SI7661ESA+T-HX/SI7661DJ-HX CMOS Voltage Converters

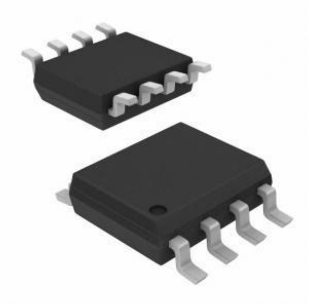
The SI7661ESA+T-HX/SI7661DJ-HX is a monolithic charge pump voltage inverter designed to convert a positive voltage in the range of +4.5V to +20V into the corresponding negative voltage of -4.5V to -20V. Compared to previous implementations of charge pump voltage inverters, the SI7661ESA+T-HX/SI7661DJ-HX offers superior performance by combining low quiescent current with high efficiency. It integrates an oscillator, control circuitry, and 4 power MOS switches on-chip, requiring only two low-cost capacitors as external components.

FEATURES

- +4.5V to +20V Supply to -4.5V to -20V Output
- Cascaded Voltage Multiplication (Vout =-n×V+)
- 99.7%Typical Open Circuit Conversion Efficiency
- Requires Only 2 External Capacitors
- Pin Compatible with the SI7661ESA+T-HX/SI7661DJ-HX

APPLICATIONS

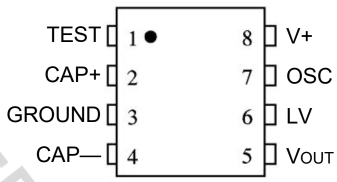
- Inexpensive Negative Supplies
- Data Acquisition Systems
- Up to -20V for Op Amps,and Other Linear Circuits
- Supply Splitter,Vout =Vs/2 RS-232 Power Supplies



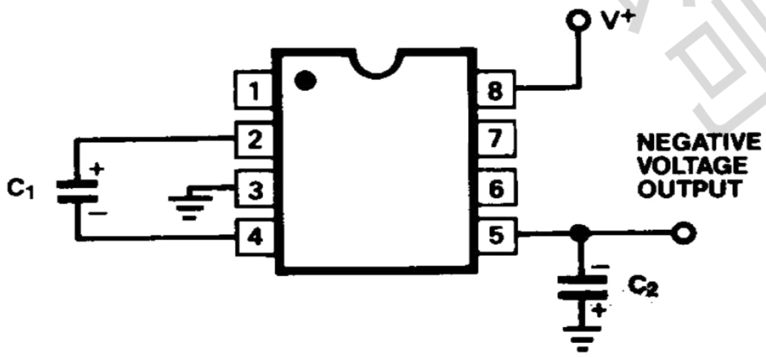
SOP-8

DIP-8

PIN ASSIGNMENT



Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

Symbol	Limit	Unit
V+TO GND	-0.3,+22	V
Oscillator Input to GND(Note 1)		
V-<12V	-0.3,V++0.3	V
V+>12V	V+-12.3,V++0.3V	V
Power Dissipation (Note 2)		
Plastic DIP	300	mW
SO	500	mW
TO-99	500	mW
CERDIP	500	mW
Operating Temperature Ranges		
Commercial	0 to +70	℃
Extended	-40 to +85	℃
Military	-55 to +125	℃
Storage Temperature	-65 to +160	℃
Lead Temperature	+300	℃

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range-Lo	V+L	RL=10k2,LV=GND	55℃<TA<+125℃	4.5		11	V
Supply Voltage Range-Hi	V+H	RL=10k2,LV=Open	40℃<T <+85℃	9		20	
			55℃< +125℃	9		16.5	
Supply Current	I+	RL=o,LV=Open	TA=+25℃		0.25	0.60	mA
			0°C<TA<+70℃		0.30	0.85	
			55℃<TA<+125C		0.40	1.0	
Output Source Resistance	Ro	Io =20mA,LV =Open	TA=+25℃		60	100	Ω
			0℃<TA<+70°C		70	120	
			55°℃<TA<+125℃		90	150	
Supply Current	I+	V+=5V, RL=oo,LV=GND	TA=+25℃		20	150	μA
			0℃<TA<+70℃		25	200	
			-55℃<TA<+125C		30	250	
Output Source Resistance	Ro	V+=5V, Io =3mA, LV =GND	TA=+25℃		125	200	Ω
			0℃<TA<+70℃		150	250	
			-55℃<TA<+125℃		200	350	
Oscillator Frequency	fosc				10		kHz
Power Efficiency	Peff	RL=2kQ	TA=+25℃	93	96		%
			Min<TA<Max	90	95		
Voltage Conversion Efficiency	VoEf	RL=∞	Min<TA<Max	97	99.9		%
Oscillator Sink or Source Current	Iosc	V+=5V(Vosc =OV to +5V)			0.5		μA
		V+=15V(Vosc=+5V to+15V)			4.0		

Notes

a. Connecting any terminal to voltages greater than V+or less than ground may cause destructive latchup.It is recommended that no input from sources operating from external supplies be applied prior to power-up of the SI7661ESA+T-HX/SI7661DJ-HX.
b. Derate linearly above +50*C by 5.5mW/℃
c.Pin 1 is a test pin and is not connected in normal use.

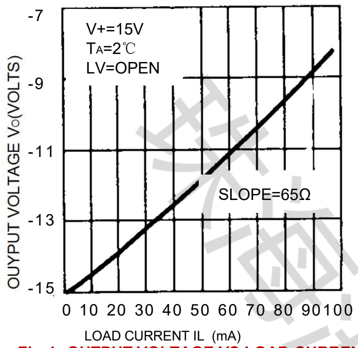


Fig 1. OUTPUT VOLTAGE VS.LOAD CURRENT

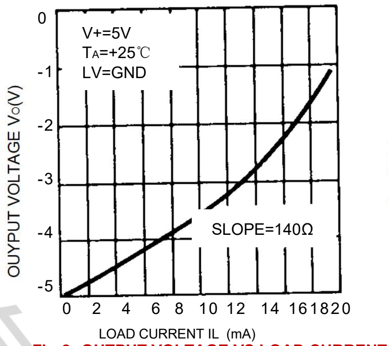


Fig 2. OUTPUT VOLTAGE VS.LOAD CURRENT

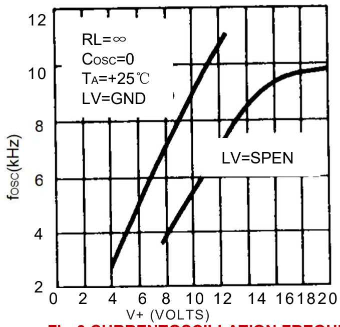


Fig 3.CURRENTOSCILLATION FREQUENCY Vs.SUPPLY VOLTAGE

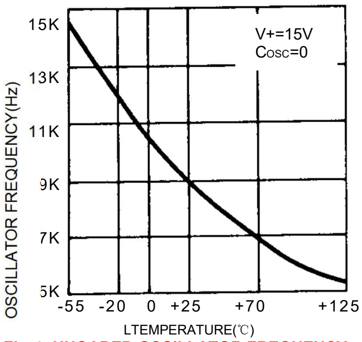


Fig 4. UNOADED OSCILLATOR FREQUENCY vs. TEMPERATURE

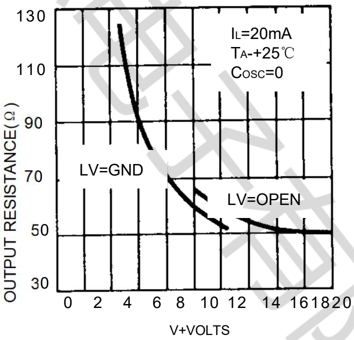


Fig 5. OUTPUT SOURCE RESLSTANCE vs. SUPPLY VOLTAGE

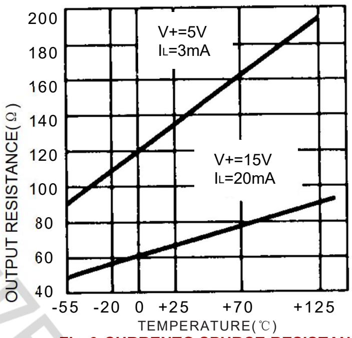


Fig 6.CURRENTO SPURCE RESISTANCE vs. TEMPERATURE

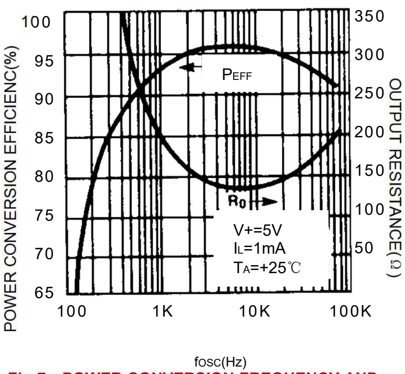


Fig 7 . POWER CONVERSION FREQUENCY AND OUTPUT RESISTANCE vs. OSCILLATOR FREQUENCY

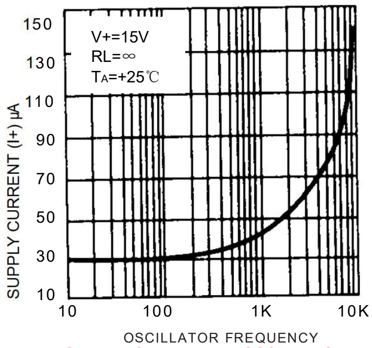


Fig 8. SUPPLY CURRENT vs. OSCILLATOR FREQUENCY

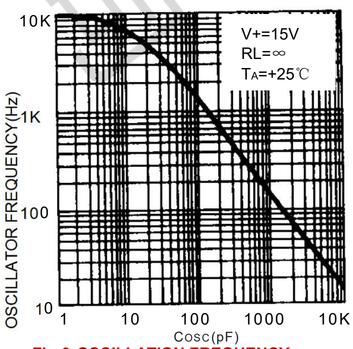


Fig 9.OSCILLATION FREQUENCY vs. EXTERNAL OSCILLATOR CAPACITANCE

Detailed Description

The SI7661ESA+T-HX/SI7661DJ-HX is a fully integrated circuit that incorporates all the necessary components to fun ction as a voltage inverter.It requires only two external capacitors, typically inexpensive 10uF polarized electrol ytic cap acitors.Figure 2 illustrates the operation of the SI7661ESA+T-HX/SI7661DJ-HX an idealized voltage inverter.

In the first half of the cycle, switches S2 and S4 are kept open, while switches S1 and S3 are closed. This allows the capacitor C1 to charge to a voltage equal to Vin. Then, in the second half of the cycle, switches S1 and S3 are opened, and switches S2 and S4 are closed. As a result, the capacitor C1 undergoes a negative shift, equivalent to Vin.

Assuming ideal switches (with zero resistance, Ron = 0) and no load on C2, the charge from C1 is then transferred to C2. This transfer ensures that the voltage on C2 is precisely the negative of Vin, i.e., -Vin.

The four switches depicted in Figure 2 are MOS power switches. Specifically, switch S1 is a P-channel switch, while switches S2, S3, and S4 are N-channel devices.

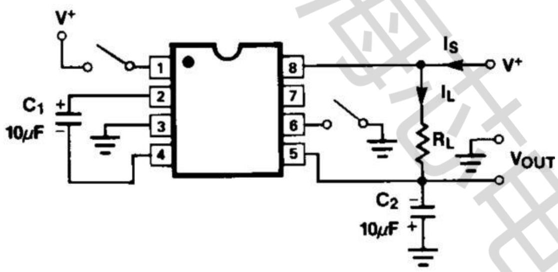


Figure 1.SI7661ESA+T-HX/SI7661DJ-HX Test Circuit

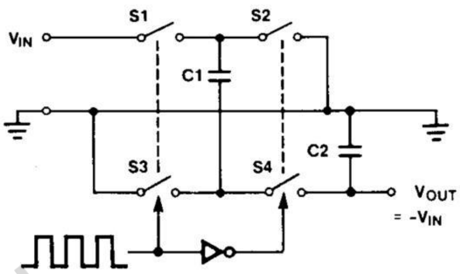


Figure 2.Idealized Negative Voltage Converter

Efficiency Considerations

In theory, a voltage multiplier can achieve nearly 100% efficiency provided certain conditions are satisfied. The SI7 661ESA+T-HX approximates the conditions necessary for efficient negative voltage multiplication when large-valued capacitors C1 and C2 are employed. These conditions include:

- The output switches exhibit virtually no offset voltage and have extremely low ON resistance.
- The power consumed by the drive circuitry is minimal.
- The impedances of the reservoir capacitor (C1) and the pump capacitor (C 2) are negligible.

The energy loss per charge pump cycle can be expressed as:

$$E = k \times C1 \times (Vin^2 - Vout^2)$$

There will be a significant voltage drop between Vin and Vout if the impedances of C1 and C2 (at the pump frequency) are comparatively high with respect to the output load R1. To minimize output ripple, it is practical to use a large value for C2. Furthermore, increasing the values of both C1 and C2 will enhance the overall efficiency of the voltage multiplier.

General Precautions

Here is a reorganized version of the text with the same meaning:

The positive terminal of capacitor C1 must be connected to Pin 2 of the SI7661ESA+T-HX/SI7661DJ-HX, while the positive terminal of capacitor C2 should be grounded.

Always ensure not to exceed the maximum specified supply voltages.

For improved efficiency, when using supply voltages less than 8 volts, connect the LV pin to Ground.

Avoid shorting Vout to V+ for extended periods of time. However, transient conditions, including during startup, are acceptable.

Applications

Changing Oscillator Frequency

Normally, the OSC pin of the SI7661ESA+T-HX/SI7661DJ-HX is left open, utilizing the nominal frequency of 10kHz (or a charge pump frequency of 5kHz). However, to lower the oscillator frequency, an external capacitor can be connected between the OSC and V+ pins (see Figure 3). A graph in the "Typical Operating Characteristics" section illustrates the relationship between the nominal frequency and the capacitor value. Reducing the oscillator frequency will enhance conversion efficiency when dealing with very low output current values. Nevertheless, a drawback of lowering the oscillator frequency is an increase in the impedance level of the pump capacitor. To compensate for this effect, the values of C1 and C2 can be increased.

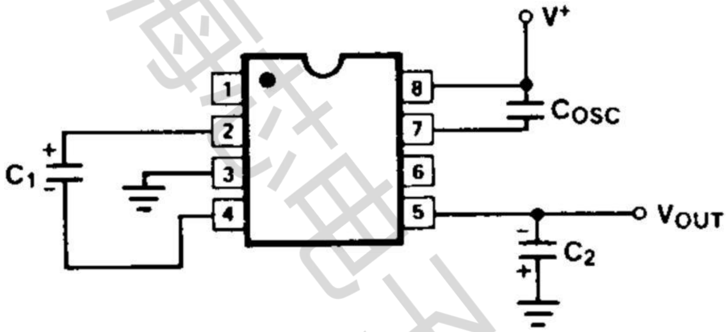


Figure 3.Lowering Oscillator Frequency

In certain applications, especially audio amplifiers, the 5kHz output ripple frequency can be undesirable. There are two methods to increase the oscillator frequency. The first approach is to overdrive the OSC pin using an external oscillator. To prevent the risk of latchup, it is recommended to insert a 1kΩ resistor in series with the OSC input (see Figure 4). If the external clock source does not pull up close to V+, then a 10kΩ pullup resistor is advisable. With this configuration, the pump frequency, and consequently, the output ripple, will be half of the external clock frequency. While driving the SI7661ESA+T-HX/SI7661DJ-HX with a higher frequency clock will slightly increase the supply current, it enables the use of smaller external capacitors and raises the ripple frequency.

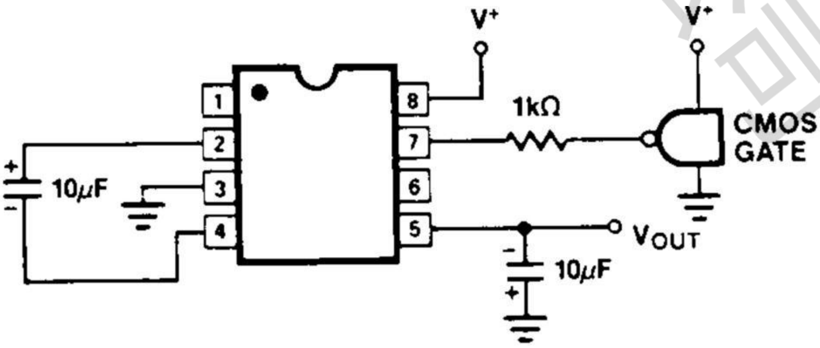
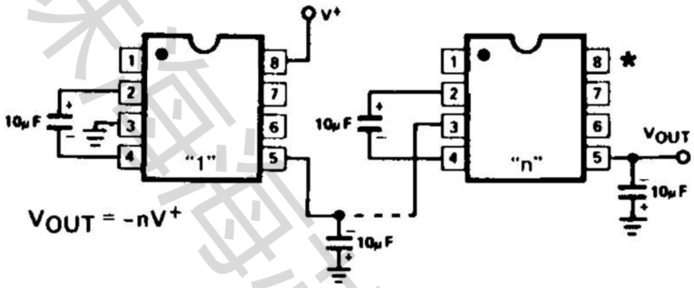


Figure 4.External Clocking

The second approach is to connect pin 1 (TEST) to V+. This effectively disconnects the internal oscillator from the OSC pin. Since there is always a minimal amount of parasitic capacitance present at the OSC pin, connecting the TEST pin to V+ allows the capacitor to oscillate at a faster rate, depending on the amount of parasitic capacitance originating from the OSC pin.

Cascading Devices

To achieve a larger negative voltage multiplication factor from the initial supply voltage, the SI7661ESA+T-HX/SI7661DJ-HX can be cascaded in a configuration as depicted in Figure 5. The resulting output resistance is approximately equivalent to the weighted sum of the individual SI7661ESA+T-HX/SI7661DJ-HX Rout values. For lighter loads, the practical limitation is up to 10 devices.The output voltage is defined by the formula Vout = -n × V+ (where n is an integer representing the number of cascaded devices).



Pin 8 tied to Pin 3 of device n-1.

Figure 5.Cascading SI7661ESA+T-HX/SI7661DJ-HX for Increased Output Voltage Negative Voltage Converter

The SI7661ESA+T-HX/SI7661DJ-HX is primarily utilized as a charge pump voltage inverter, effectively transforming a positive voltage into its corresponding negative equivalent. As depicted in the simplified circuit of Figure 6, it requires only two external components, namely C1 and C2, typically low-cost 10uF electrolytic capacitors. It is important to note that the SI7661ESA+T-HX/SI7661DJ-HX is not a voltage regulator. When powered by a +15V supply, its output source resistance approximates 60Ω.This signifies that, under light loads (less than 1mA load current), the output voltage will be -15V. However,with an increased load current of 10mA, the output voltage will slightly drop to -14.4V. The total output source impedance of the entire circuit is a combination of the SI7661ESA+T-HX/SI7661DJ-HX's output resistance and the impedance of the pump capacitor at the pumping frequency.

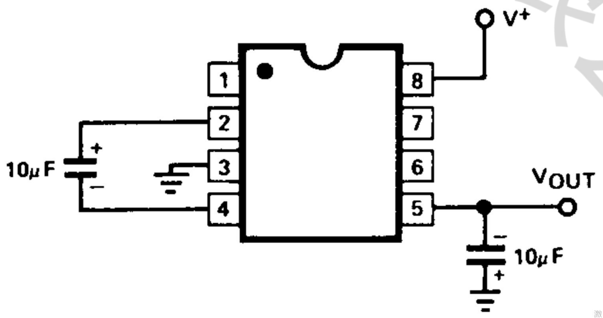


Figure 6.Negative Voltage Converter

The output ripple of the voltage inverter can be calcu-lated by noting that the output current is suppliedsolely by the reservoir capacitor during one-half ofthe charge pump cycle.This introduces an outputripple of:

VRIPPLE=k×Iour×(1/FpuMP)×(1/C2)

For the nominal Fpump of 5kHz(one-half of the nom-inal 10kHz oscillator frequency)and a 10μF C2,theoutput ripple will be approximately 10mV with a loadcurrent of 10mA.

Positlve Voltage Doubler

The SI7661ESA+T-HX/SI7661DJ-HX can double a positive voltage asshown in Figure 7.It basically uses the SI7661ESA+T-HX/SI7661DJ-HX as a power inverter.The only drawback fromthis circuit is the inevitable voltage drop across thetwo diodes.

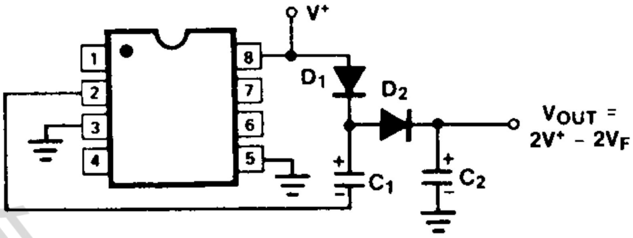
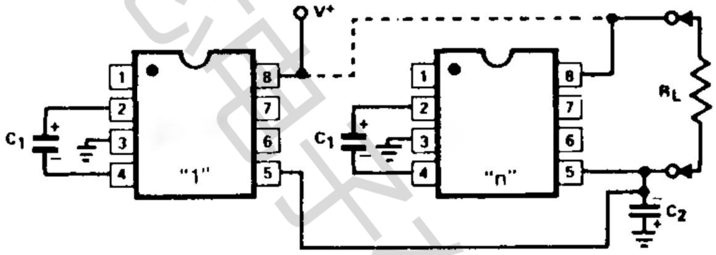


Figure 7.Positive Voltage Doubler

Paralleling Devices

Connecting multiple SI7661ESA+T-HX/SI7661DJ-HX in parallel effectively reduces the overall output resistance. As depicted in Figure 8,each individual device requires its own dedicated pump capacitor, labeled C1. However, the reservoir capacitor,denoted as 'C2', serves as a shared component for all paralleled devices. The equation for calculating the reduced output resistance resulting from this parallel configuration is also presented in Figure 8.



$$R_{OUT} = \frac{R_{OUT}(\text{of SI7661ESA+T-HX/SI7661DJ-HX})}{n(\text{number of devices})}$$

Figure 8.Paralleling SI7661ESA+T-HX/SI7661DJ-HX to Reduce Output Resistance

Combining Positive Voltage Multiplication and Negative Voltage Conversion

Figure 9 demonstrates the dual functionality of combining positive voltage multiplication and negative voltage conversion. In this circuit, capacitors C1 and C3 serve as the pump and reservoir capacitors respectively for generating the negative voltage. Meanwhile, capacitors C2 (pump capacitor) and C4 (reservoir capacitor) are utilized for the positive voltage converter. However, this circuit configuration leads to a higher source impedance of the generated power supplies, primarily due to the finite impedance of the shared charge pump driver.

Voltage Splitting

The SI7661ESA+T-HX/SI7661DJ-HX can also be employed to split a power supply or battery. As shown in Figure 10, the positive terminal of the power supply is connected to V+, while the negative terminal is connected to Vout. The midpoint of the power supply is found on Pin 3. This configuration offers a significantly lower output resistance compared to other applications, enabling higher currents to be drawn from it.

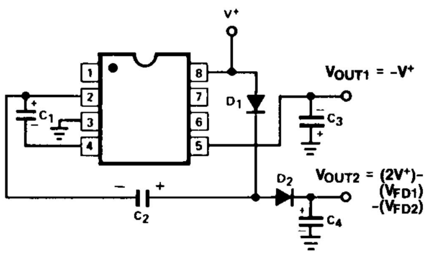


Figure 9.Combined Positive Multiplier and NegativeConverter

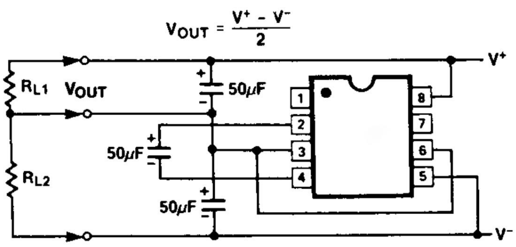
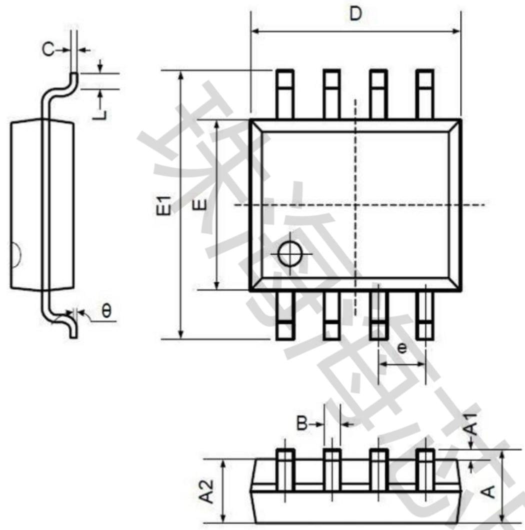


Figure 10.Splitting a Supply in Half

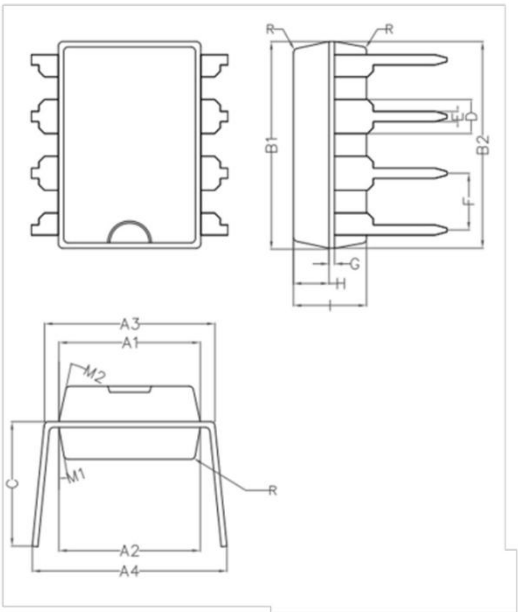
Package Information

SOP8 (Package Outline Dimensions)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

DIP8 (Package Outline Dimensions)



Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
I	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°

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