

N-Ch 100V Fast Switching MOSFETs

Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Product Summary

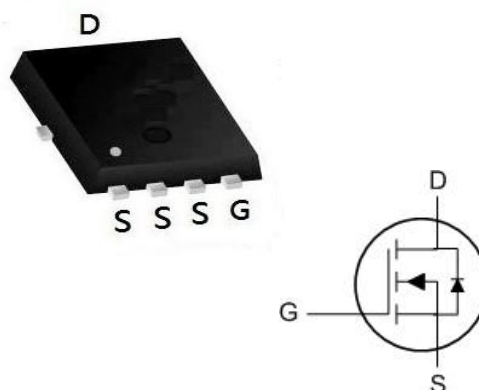


BVDSS	RDSON	ID
100V	15.6mΩ	30A

Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

PDFN3333-8L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	30	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	18	A
I_{DM}	Pulsed Drain Current ²	120	A
EAS	Single Pulse Avalanche Energy ³	39	mJ
I_{AS}	Avalanche Current	---	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation ⁴	31	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	---	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	4	$^\circ\text{C/W}$

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Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	100	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	---	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=20A$	---	15.6	20.3	m Ω
		$V_{GS}=4.5V$, $I_D=10A$	---	19	24.7	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	1.0	1.5	2.0	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	---	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=100V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=100V$, $V_{GS}=0V$, $T_J=100^\circ\text{C}$	---	---	100	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=10V$, $I_D=10A$	---	---	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	---	---	Ω
Q_g	Total Gate Charge	$V_{DS}=50V$, $V_{GS}=10V$, $I_D=5A$	---	13	---	nC
Q_{gs}	Gate-Source Charge		---	3	---	
Q_{gd}	Gate-Drain Charge		---	3.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{GS}=10V$, $V_{DD}=50V$, $R_G=3\Omega$, $I_D=5A$	---	4.5	---	ns
T_r	Rise Time		---	5	---	
$T_{d(off)}$	Turn-Off Delay Time		---	16.7	---	
T_f	Fall Time		---	8.7	---	
C_{iss}	Input Capacitance	$V_{DS}=50V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	806	---	pF
C_{oss}	Output Capacitance		---	278	---	
C_{rss}	Reverse Transfer Capacitance		---	8	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	30	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=20A$, $T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=10A$, $di/dt=100A/\mu s$, $T_J=25^\circ\text{C}$	---	39	---	nS
Q_{rr}	Reverse Recovery Charge		---	30	---	nC

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.3. The EAS data shows Max. rating. The test condition is $T_J = 25^\circ\text{C}$, $V_{DD}=50V$, $V_{GS}=10V$, $L=0.1\text{mH}$.4. The power dissipation is limited by 150°C junction temperature.5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Characteristics

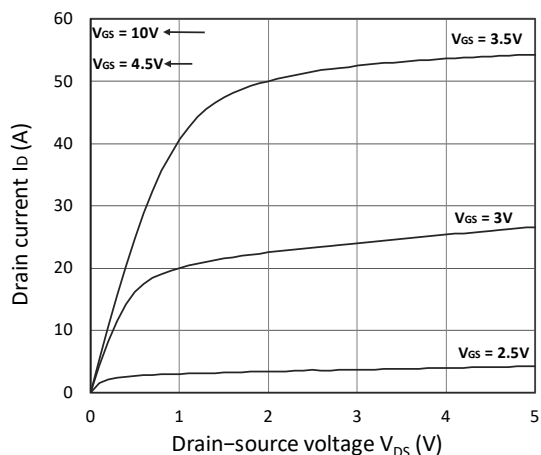


Figure 1. Output Characteristics

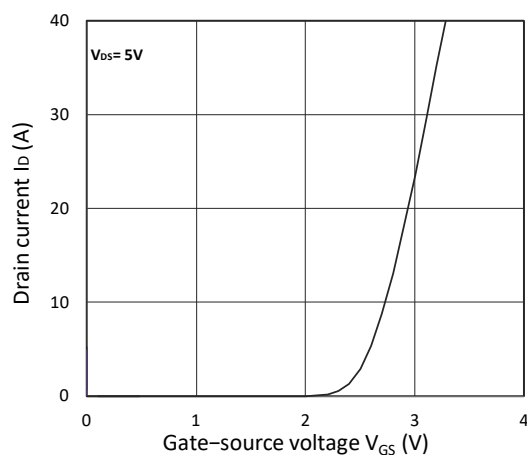


Figure 2. Transfer Characteristics

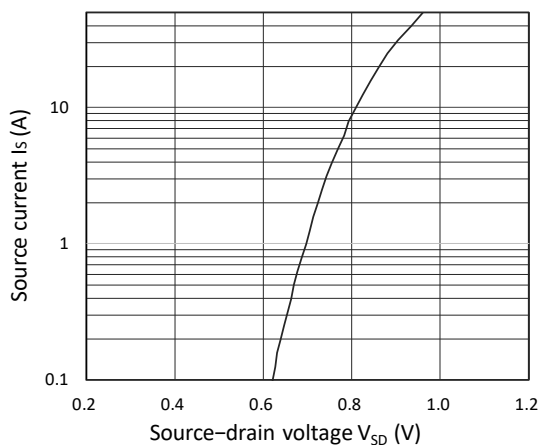


Figure 3. Forward Characteristics of Reverse

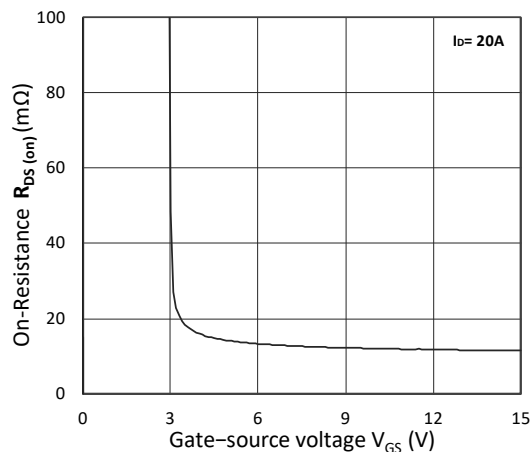


Figure 4. $R_{DS(on)}$ vs. V_{GS}

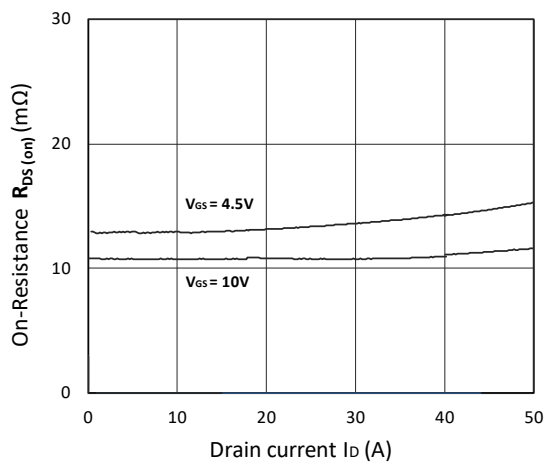


Figure 5. $R_{DS(on)}$ vs. I_D

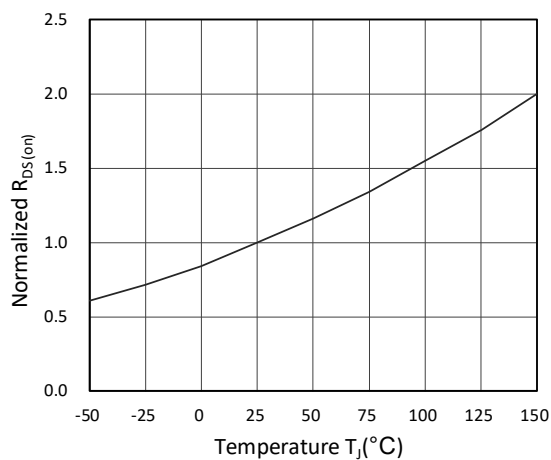


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

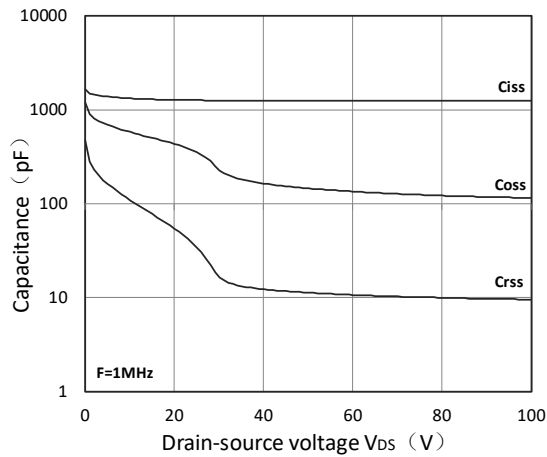


Figure 7. Capacitance Characteristics

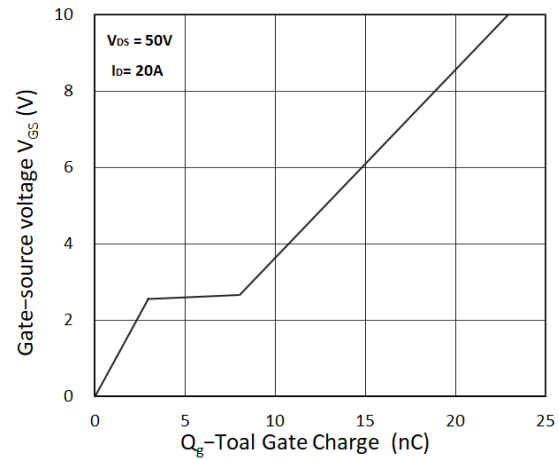


Figure 8. Gate Charge Characteristics

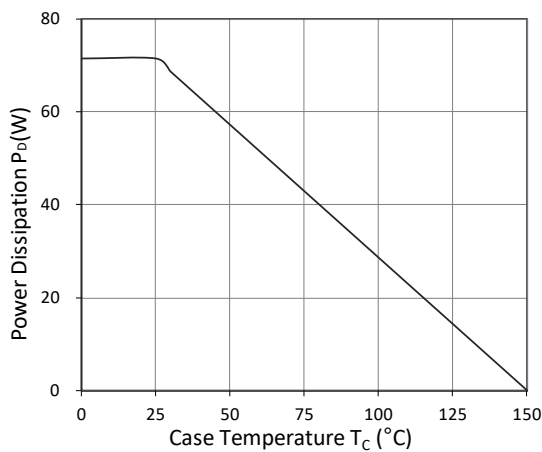


Figure 9. Power Dissipation

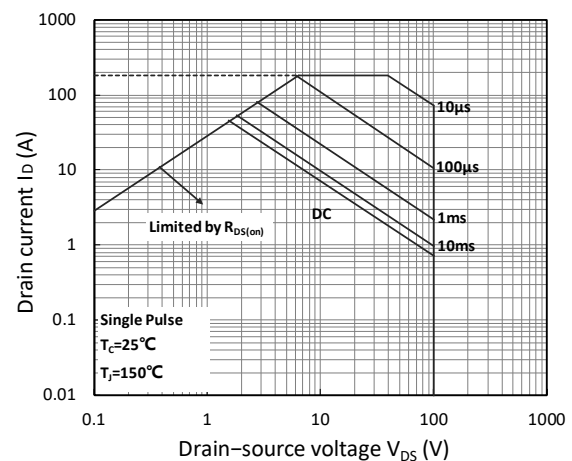


Figure 10. Safe Operating Area

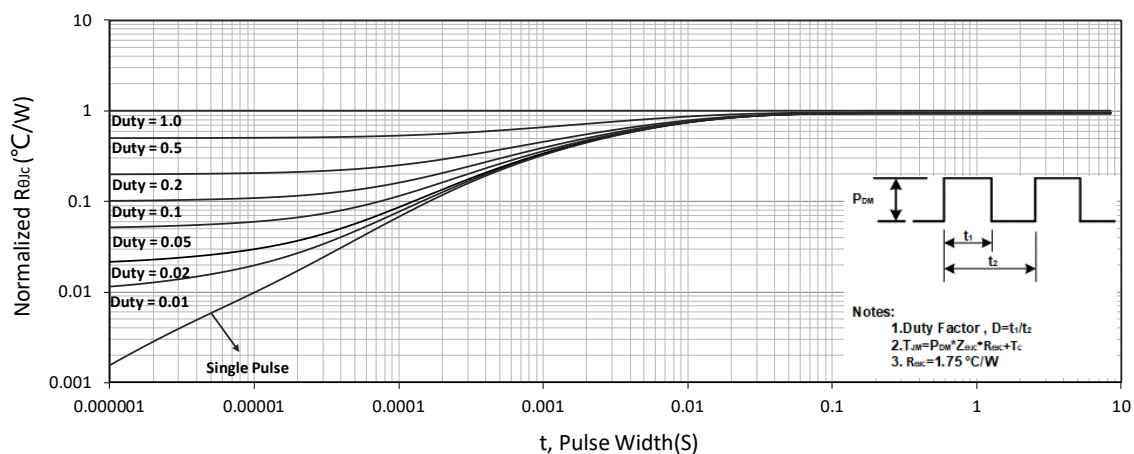
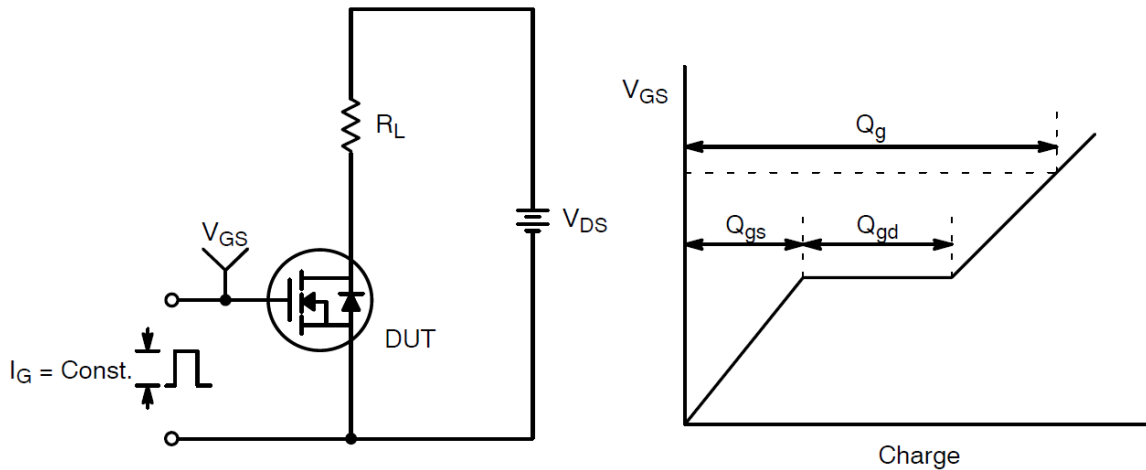
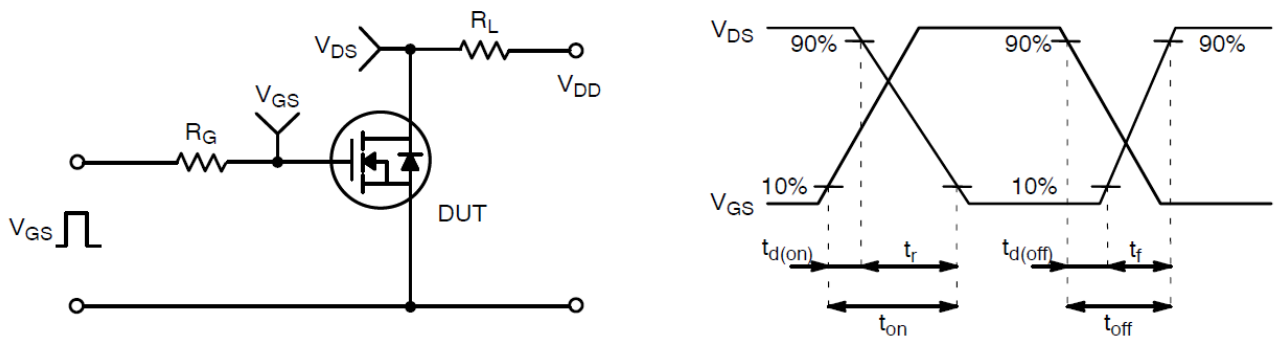


Figure 11. Normalized Maximum Transient Thermal Impedance

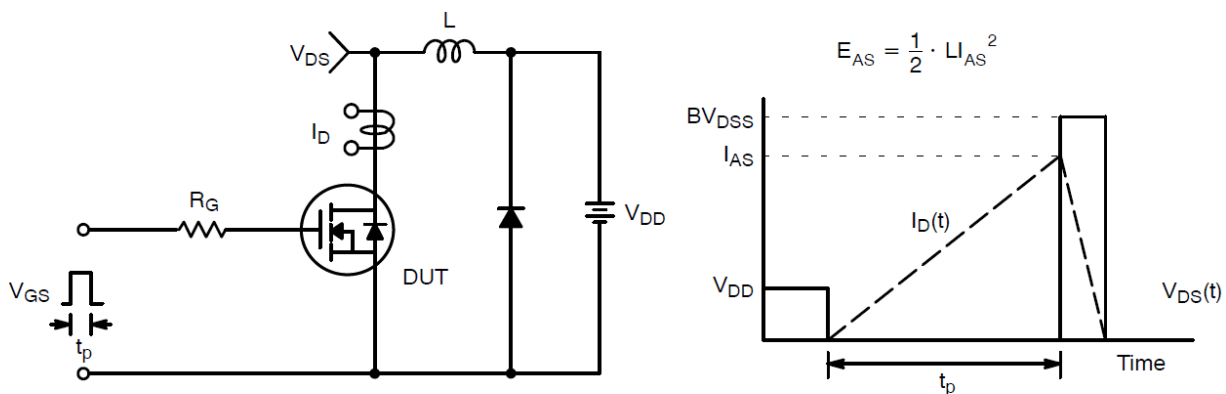
Test Circuit and Waveform:



Gate Charge Test Circuit & Waveform

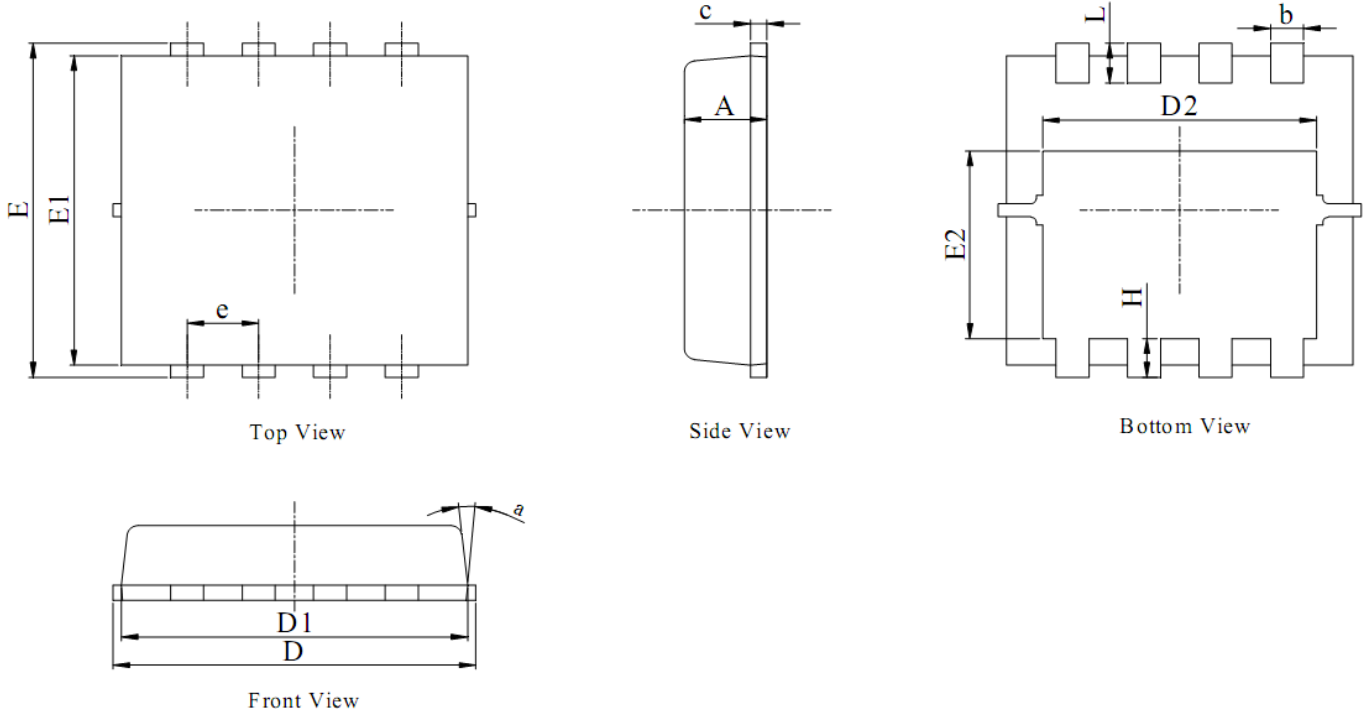


Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

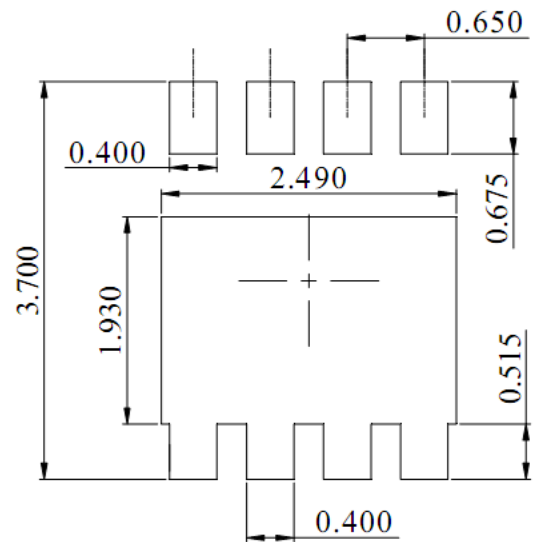
Package Mechanical Data-PDFN3333-8L-Single



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMENSIONS IN MILLIMETER (ANGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.20	0.25
D	3.00	3.15	3.25
D1	2.95	3.05	3.15
D2	2.39	2.49	2.59
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.70	1.80	1.90
e	0.65 BSC		
H	0.30	0.40	0.50
L	0.25	0.40	0.50
a	---	---	15°



DIMENSIONS:MILLIMETERS