

## Features

- Octal, 16-/12-Bit Pin-Compatible DACs
  - TPC116S8U: 16 Bits
  - TPC112S8U: 12 Bits
- Low Power Consumption (1.6 mA Typ)
- Differential Nonlinearity:  $\pm 1$  LSB (Max)
- Glitch Energy: 2 nV-s
- Power-on Reset to Zero
- Supply Range: 2.7 V to 5.5 V
- Buffered Rail-to-Rail Output Operation
- Safe Power-on Reset (POR) to Zero DAC Output
- Fast 30-MHz, 3-Wire, SPI/QSPI/MICROWIRE-Compatible Serial Interface
- Schmitt-Trigger Inputs for Direct Optocoupler Interface
- SYNC Interrupt Facility
- Available in QFN4X4-16 and TSSOP16 Package

## Applications

- Gain and Offset Adjustment
- Process Control and Servo Loops
- Programmable Voltage and Current Sources
- Programmable Attenuators
- Automatic Test Equipment

## Description

The TPC116S8U/TPC112S8U devices are pin-compatible 16-bit and 12-bit digital-to-analog converters. These devices are 8-channel, low-power, and buffered voltage-out DACs and are guaranteed monotonic by design. The devices use a precision external reference applied through the high-resistance input for rail-to-rail operation and low system power consumption.

The TPC116S8U/TPC112S8U accept a wide 2.7-V to 5.5-V supply voltage range. The parts incorporate a power-on reset circuit to ensure that the DAC output powers up to 0 V and remains there until a valid write takes place.

The on-chip precision output amplifier of the TPC116S8U/TPC112S8U allows rail-to-rail output swing to be achieved. For remote sensing applications, the inverting input of the output amplifier is available to users. The TPC116S8U/TPC112S8U use a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with SPI<sup>®</sup>, QSPI<sup>™</sup>, MICROWIRE<sup>™</sup>, and DSP interface standards.

The TPC116S8U/TPC112S8U are available in the small-sized TSSOP16 and QFN4X4-16 packages. All packages are specified over the  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  extended industrial temperature range.

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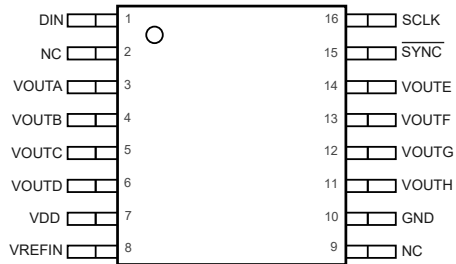
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## Revision History

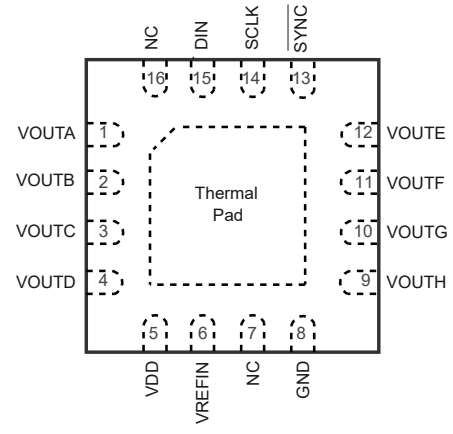
Date	Revision	Notes
2018-11-01	Rev.1.0	Initial release.
2020-03-07	Rev.1.0	Correct description typo.
2022-07-05	Rev.1.1	Correct description typo.
2023-04-21	Rev.1.2	Correct TCSA parameter typo.
2024-12-20	Rev.A.1	Updated to a new datasheet format. Updated the POD. Updated the Pin Functions table. Added the MSL value in the Order Information.

## Pin Configuration and Functions

SNC11xS8  
TSSOP16  
Top View



SNC11xS8  
QFN4X4-16  
Top View



**Table 1. Pin Functions: SNC11xS8**

Pin No.		Name	I/O	Description
TSSOP16	QFN4X4-16			
1	15	DIN	I	<ul style="list-style-type: none"> <li>Serial data input.</li> <li>Data is clocked into the 16-/24-bit input shift register on each falling edge of the serial clock input.</li> <li>Schmitt-Trigger logic input.</li> </ul>
2	16	NC	-	Not connect.
3	1	VOUTA	O	DACA output.
4	2	VOUTB	O	DACB output.
5	3	VOUTC	O	DACC output.
6	4	VOUTD	O	DACD output.
7	5	VDD	P	Power supply input, 2.7 V to 5.5 V.
8	6	VREFIN	I	Reference voltage input.
9	7	NC	-	Not connect.
10	8	GND	GND	Ground reference point for all circuitry on the part.
11	9	VOUTH	O	DACH output.
12	10	VOUTG	O	DACG output.
13	11	VOUTF	O	DACF output.
14	12	VOUTE	O	DACE output.
15	13	SYNC	I	<ul style="list-style-type: none"> <li>Level-triggered control input (active Low).</li> <li>This is the frame synchronization signal for the input data.</li> </ul>

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**Octal 12-Bit, Low-Power, High-Performance DAC**

Pin No.		Name	I/O	Description
TSSOP16	QFN4X4-16			
				<ul style="list-style-type: none"><li>When <math>\overline{\text{SYNC}}</math> goes Low, it enables the input shift register and data is transferred in on the falling edges of the following clocks.</li></ul>
16	14	SCLK	I	<ul style="list-style-type: none"><li>Serial clock input.</li><li>Data can be transferred at rates up to 30 MHz.</li><li>Schmitt-Trigger logic input.</li></ul>
	Thermal PAD	Thermal PAD	-	<ul style="list-style-type: none"><li>Connected to GND internally.</li><li>Suggest to connect it to GND.</li></ul>

## Specifications

### Absolute Maximum Ratings <sup>(1)</sup>

Parameter		Min	Max	Unit
	Supply Voltage: $V^+ - V^-$ <sup>(2)</sup>		7	V
	Input Voltage	$V^- - 0.3$	$V^+ + 0.3$	V
	Input Current: $+I_{IN}$ , $-I_{IN}$ <sup>(3)</sup>	-20	20	mA
	Output Short-Circuit Duration <sup>(4)</sup>		Indefinite	
$T_A$	Operating Temperature Range	-40	125	°C
$T_J$	Maximum Junction Temperature		150	°C
$T_{STG}$	Storage Temperature Range	-65	150	°C
$T_L$	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) The supplies must be established simultaneously, with, or before, the application of any input signals.

(3) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500 mV beyond the power supply, the input current should be limited to less than 10 mA.

(4) A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

### ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	8	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	2	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### Thermal Information

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
TSSOP16	180	35	°C/W
QFN4X4-16	34	11	°C/W

## Octal 12-Bit, Low-Power, High-Performance DAC

### Electrical Characteristics

All test conditions:  $V_{DD} = 5\text{ V}$ ,  $V_{REF} = 5\text{ V}$ ,  $C_L = 100\text{ pF}$ ,  $R_L = 10\text{ k}\Omega$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static Accuracy <sup>(1)</sup></b>						
N	Resolution	TPC112S8U	12			Bits
		TPC116S8U	16			
INL	Integral Nonlinearity	TPC112S8U (12 bits) <sup>(2)</sup>	-1	$\pm 0.25$	1	LSB
		TPC116S8U (16 bits) <sup>(2)</sup>	-16	$\pm 8$	16	
DNL	Differential Nonlinearity	TPC112S8U (12 bits) <sup>(2)</sup>	-1	$\pm 0.05$	1	LSB
		TPC116S8U (16 bits) <sup>(2)</sup>	-1	$\pm 0.5$	1	
OE	Zero Offset Error			6.5	30	mV
	Full-Scale Offset Error		-30	0	30	mV
	Offset-Error Drift			$\pm 1$		$\mu\text{V}/^\circ\text{C}$
GE	Gain Error		-0.3	$\pm 0.13$	0.3	%FS
	Gain Temperature Coefficient			$\pm 2$		ppmFS/ $^\circ\text{C}$
<b>Reference Input</b>						
$V_{REF}$	Reference-Input Voltage Range		0.5		$V_{DD}$	V
$R_{REF}$	Reference-Input Impedance			333		k $\Omega$
<b>DAC Output</b>						
	Output Voltage Range	No load (typical)			$V_{REF}$	V
		10-k $\Omega$ load	0.2		$V_{REF} - 0.1$	
	DC Output Impedance			0.1		$\Omega$
$C_L$	Capacitive Load <sup>(3)</sup>	Series resistance = 0 $\Omega$			0.1	nF
		Series resistance = 1 k $\Omega$			15	$\mu\text{F}$
$R_L$	Resistive Load <sup>(3)</sup>		5			k $\Omega$
	Short-Circuit Current	$V_{DD} = 5.5\text{ V}$		35		mA
	Power-up Time	From power-down mode		25		$\mu\text{s}$
<b>Digital Inputs (SCLK, DIN, SYNC)</b>						
$V_{IH}$	Input High Voltage	$V_{DD} = 5\text{ V}$	2			V
		$V_{DD} = 3.3\text{ V}$	1.5			V
$V_{IL}$	Input Low Voltage	$V_{DD} = 5\text{ V}$			0.6	V
		$V_{DD} = 3.3\text{ V}$			0.4	V
$I_{IN}$	Input Leakage Current	$V_{IN} = 0\text{ V}$ or $V_{DD}$		$\pm 5$	$\pm 10$	$\mu\text{A}$
$C_{IN}$	Input Capacitance			1		pF

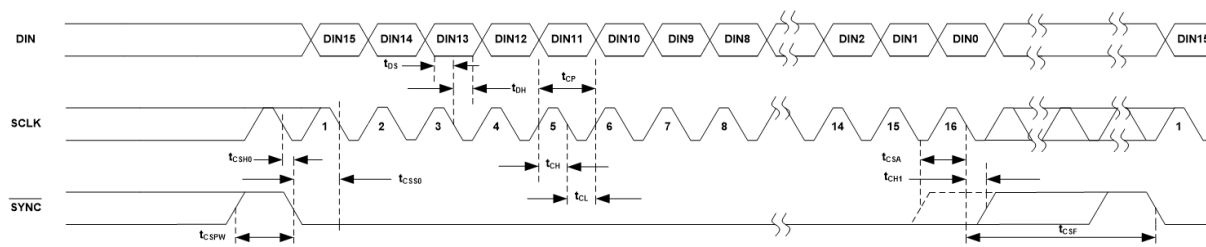
**Octal 12-Bit, Low-Power, High-Performance DAC**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>HYS</sub>	Hysteresis Voltage			0.15		V
<b>Dynamic Performance <sup>(3)</sup></b>						
SR	Voltage-Output Slew Rate	Positive and negative		1		V/μs
BW	Voltage-Output Settling Time	1/4 scale to 3/4 scale, to ≤ 0.5 LSB, 12 bits		14		μs
	Reference -3-dB Bandwidth	Hex code = 800 (TPC112S8U), Hex code = 8000 (TPC116S8U)		100		kHz
	Digital Feedthrough	Code = 0, all digital inputs from 0 V to V <sub>DD</sub> , SCLK < 50 MHz		0.5		nV·s
	DAC Glitch Impulse	Major code transition		2		nV·s
	Output Noise	10 kHz		90		nV/√Hz
	Integrated Output Noise	0.1 Hz to 10 Hz		25		μV <sub>P-P</sub>
<b>Power Requirements</b>						
V <sub>DD</sub>	Supply Voltage		2.7		5.5	V
I <sub>DD</sub>	Supply Current	V <sub>DD</sub> = 5 V, no load; all digital inputs at 0 V or V <sub>DD</sub> , supply current only; excludes reference input current, midscale		0.8	1.5	mA
		V <sub>DD</sub> = 3.3 V, no load; all digital inputs at 0 V or V <sub>DD</sub> , supply current only; excludes reference input current, midscale		0.5	1	mA
	Power-down Supply Current	No load, all digital inputs at 0 V or V <sub>DD</sub>			500	μA

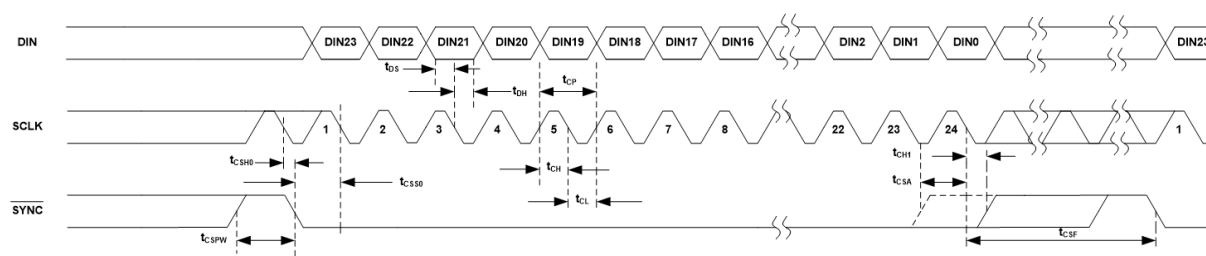
- (1) Linearity is tested within 20 mV of GND and V<sub>DD</sub>.  
(2) Gain and offset is tested within 100 mV of GND and V<sub>DD</sub>.  
(3) All timing specifications are measured with V<sub>IL</sub> = V<sub>GND</sub>, V<sub>IH</sub> = V<sub>DD</sub>.



## Serial Write Operation



**Figure 1. 16-Bit Serial-Interface Timing Diagram (TPC112S8U)**



**Figure 2. 24-Bit Serial-Interface Timing Diagram (TPC116S8U)**

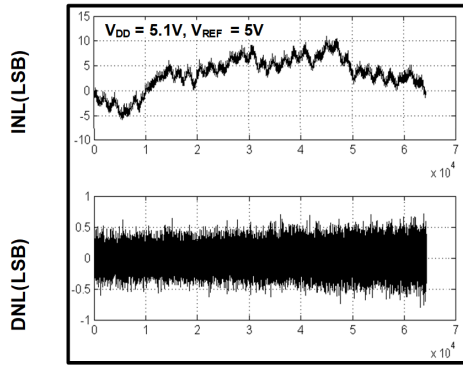
**Table 2. Timing Characteristics (Figures 1, 2)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{SCLK}$	Serial Clock Frequency		0		30	MHz
$t_{CH}$	SCLK Pulse-Width High		8			ns
$t_{CL}$	SCLK Pulse-Width Low		8			ns
$t_{CSS0}$	$\overline{SYNC}$ Fall to SCLK Fall Setup Time		8			ns
$t_{CSH0}$	$\overline{SYNC}$ Fall to SCLK Fall Hold Time		0			ns
$t_{CSH1}$	$\overline{SYNC}$ Rise to SCLK Fall Hold Time		0			ns
$t_{CSA}$	$\overline{SYNC}$ Rise to SCLK Fall		12			ns
$t_{CSF}$	SCLK Fall to $\overline{SYNC}$ Fall		100			ns
$t_{DS}$	DIN to SCLK Fall Setup Time		5			ns
$t_{DH}$	DIN to SCLK Fall Hold Time		4.5			ns
$t_{CSPW}$	$\overline{SYNC}$ Pulse-Width High		20			ns
$t_{CLPW}$	$\overline{SYNC}$ Pulse-Width Low		20			ns
$t_{CSC}$	$\overline{SYNC}$ Rise to $\overline{SYNC}$ Fall		20			ns

(1) Parameters are provided by lab bench tests and design simulations.

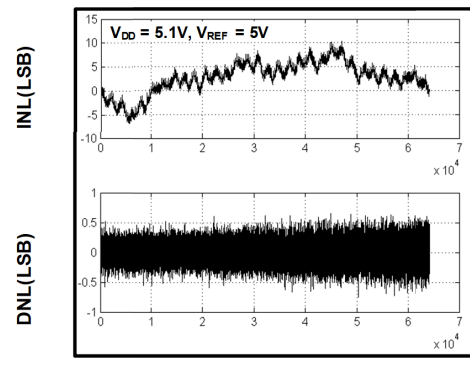
## Typical Performance Characteristics

All test conditions:  $V_S = 5\text{ V}$  at  $T_A = +25^\circ\text{C}$ , unless otherwise noted.



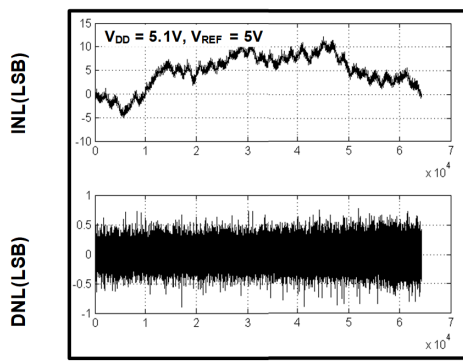
Digital Input Code

**Figure 3. INL and DNL vs. Digital Input Code (+25°C TPC116S8U)**



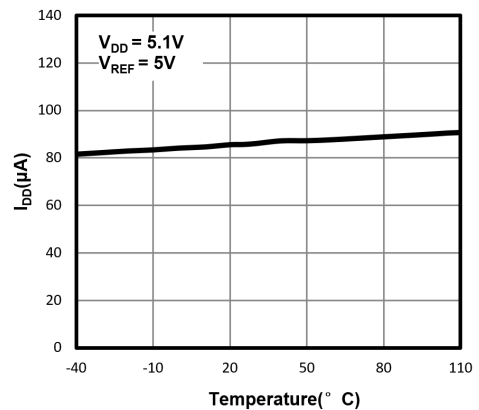
Digital Input Code

**Figure 4. INL and DNL vs. Digital Input Code (-40°C TPC116S8U)**

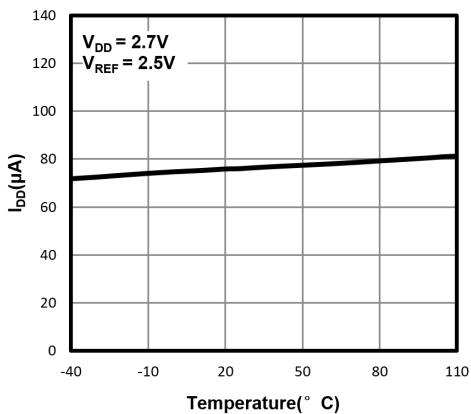


Digital Input Code

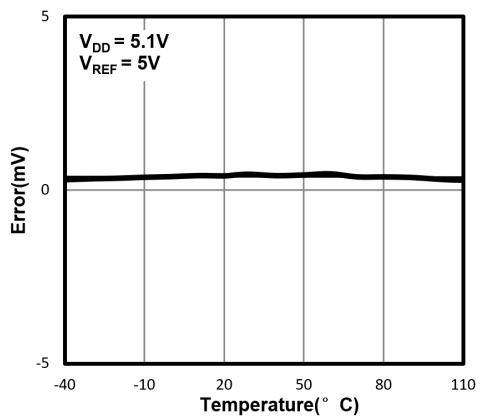
**Figure 5. INL and DNL vs. Digital Input Code (+105°C TPC116S8U)**



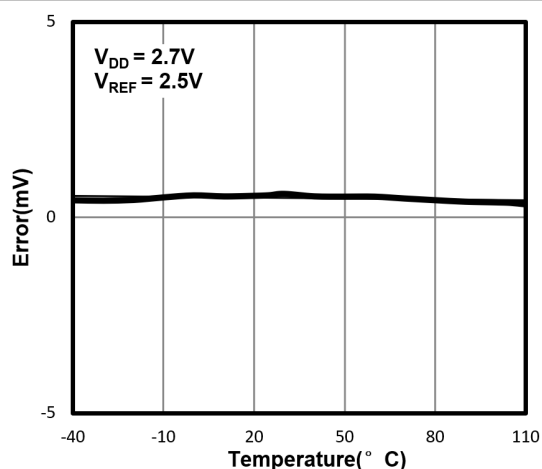
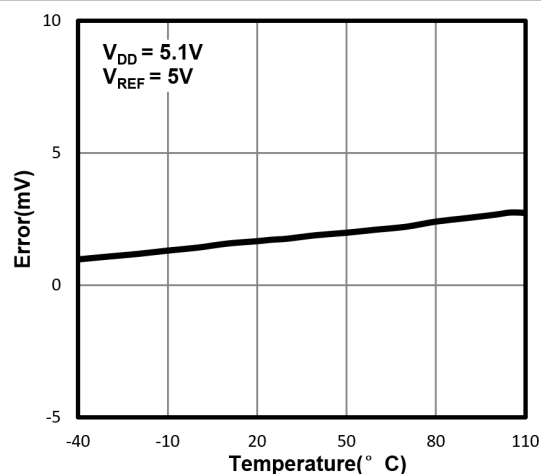
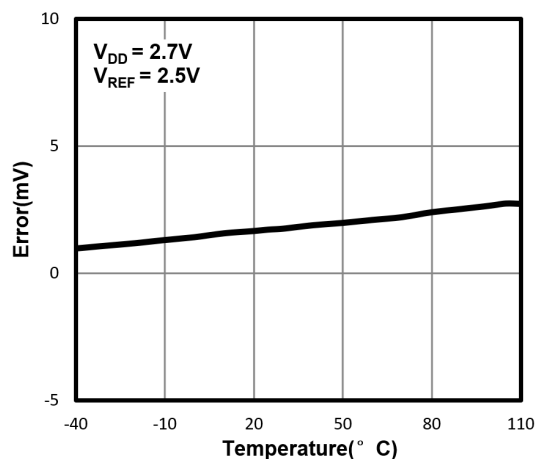
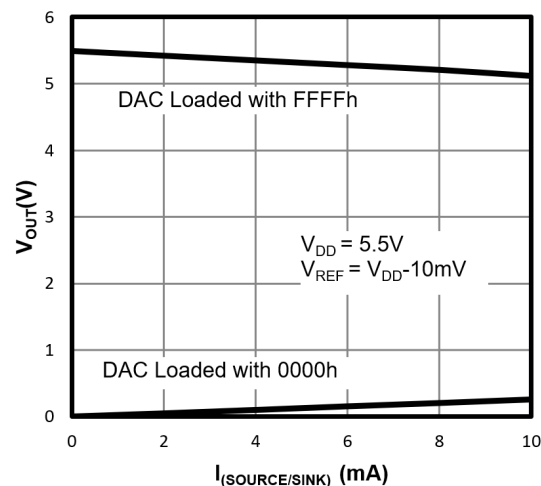
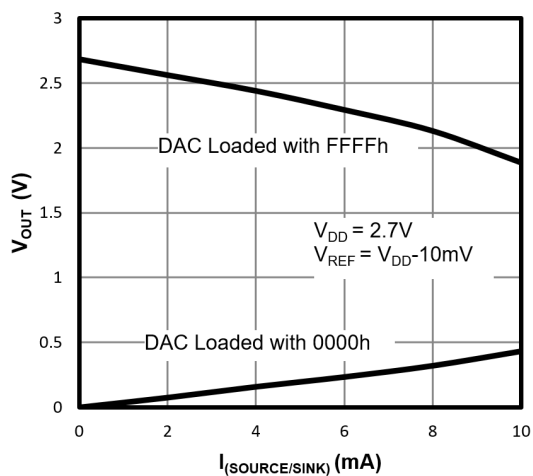
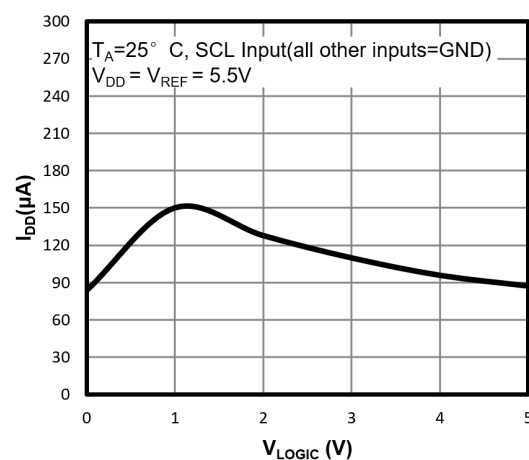
**Figure 6. Power-Supply Current vs. Temperature (TPC116S8U)**

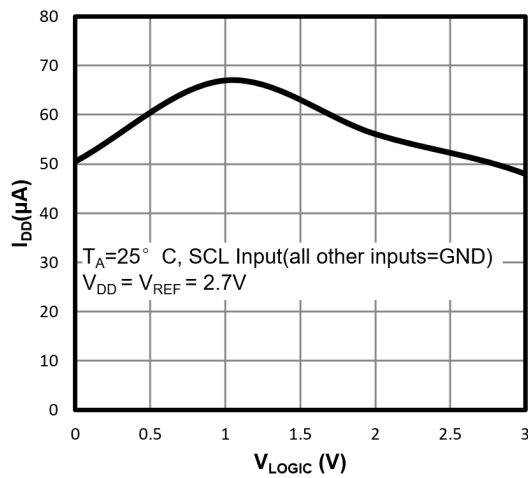


**Figure 7. Power-Supply Current vs. Temperature (TPC116S8U)**

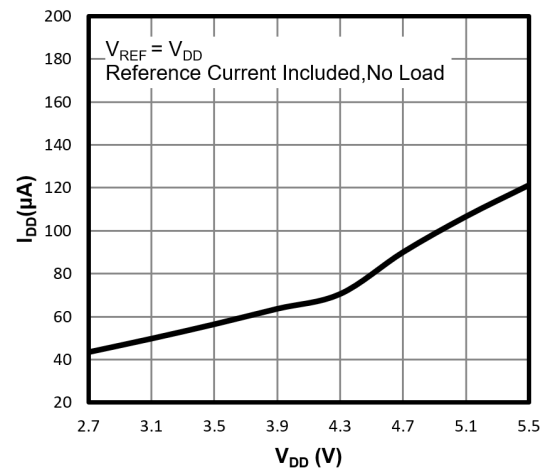


**Figure 8. Zero-Scale Error vs. Temperature (TPC116S8U)**

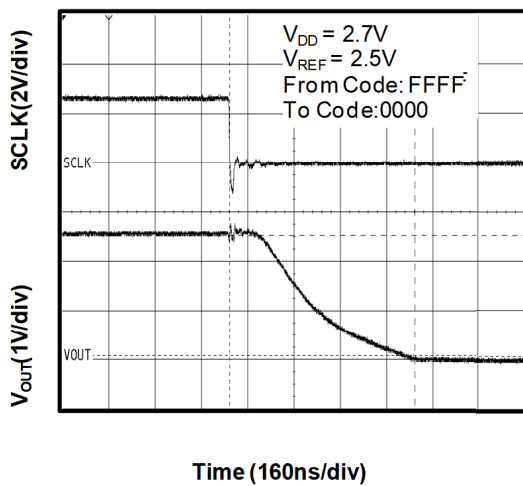

**Figure 9. Zero-Scale Error vs. Temperature (TPC116S8U)**

**Figure 10. Full-Scale Error vs. Temperature (TPC116S8U)**

**Figure 11. Full-Scale Error vs. Temperature (TPC116S8U)**

**Figure 12. Source and Sink Current Capability (TPC116S8U)**

**Figure 13. Source and Sink Current Capability (TPC116S8U)**

**Figure 14. Supply Current vs. Logic Input Voltage (TPC116S8U)**



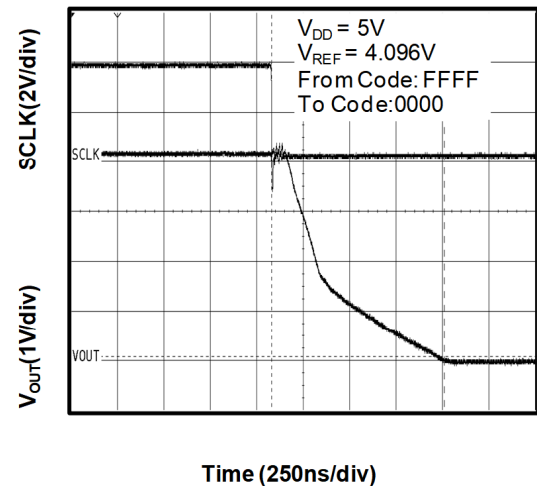
**Figure 15. Supply Current vs. Logic Input Voltage (TPC116S8U)**



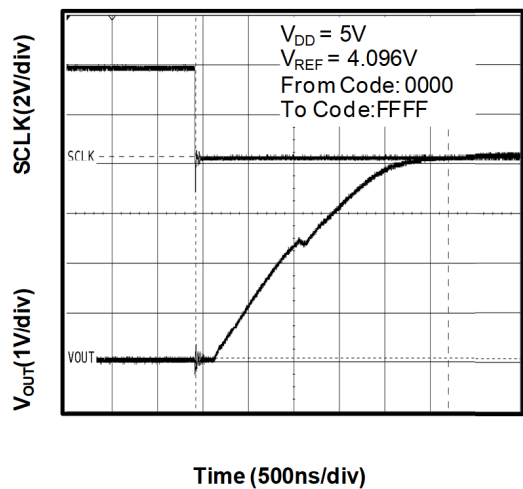
**Figure 16. Supply Current vs. Supply Voltage (TPC116S8U)**



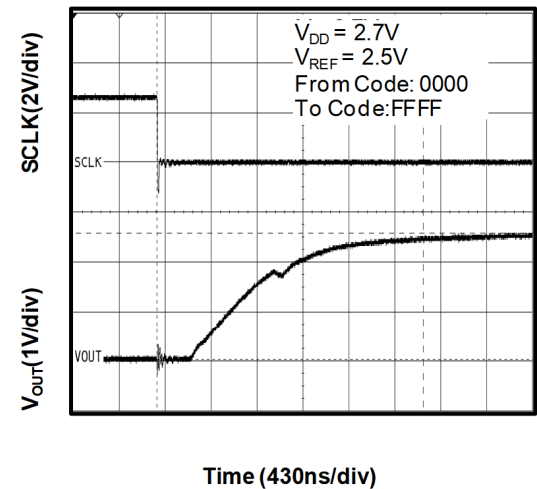
**Figure 17. Full-Scale Settling Time (2.7-V Falling Edge)**



**Figure 18. Full-Scale Settling Time (5-V Falling Edge)**



**Figure 19. Full-Scale Settling Time (5-V Rising Edge)**



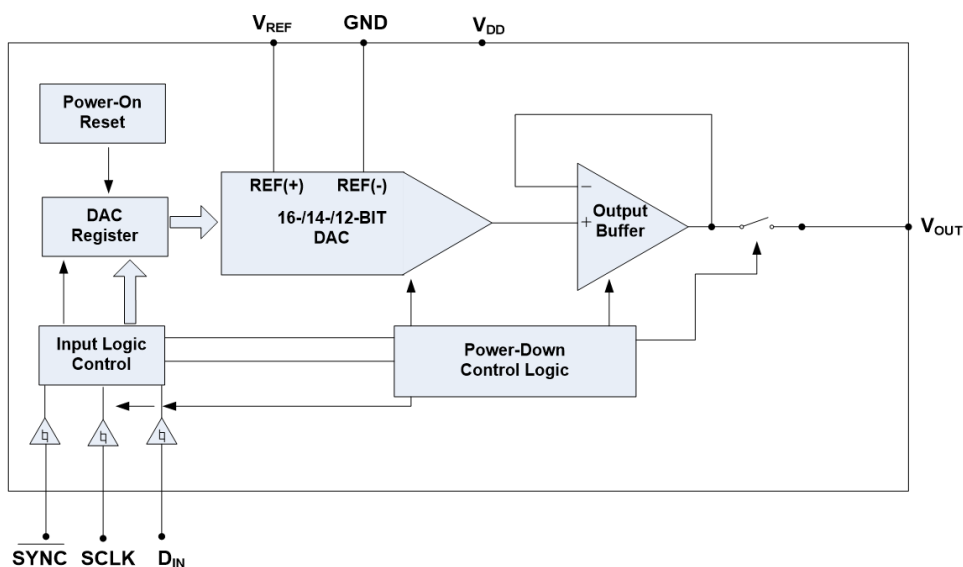
**Figure 20. Full-Scale Settling Time (2.7-V Rising Edge)**

## Detailed Description

### Overview

The TPC116S8U/TPC112S8U are pin-compatible and software-compatible 12-bit and 16-bit DACs. The TPC116S8U/TPC112S8U are 8-channel, low-power, high-reference input resistance, and buffered voltage-output DACs. The TPC116S8U/TPC112S8U minimize the digital noise feedthrough from their inputs to outputs by powering down the SCLK and DIN input buffers after the completion of each data frame. The data frames are 16 bits for the TPC112S8U and 24 bits for the TPC116S8U. During power-up, the TPC116S8U/TPC112S8U reset the DAC output to zero, providing additional safety for applications that drive valves or other transducers which need to be off during power-up. The TPC116S8U/TPC112S8U contain a segmented resistor string-type DAC, a serial-in/parallel-out shift register, a DAC register, a power-on-reset (POR) circuit, and control logic. On the falling edge of the clock (SCLK) pulse, the serial input (DIN) data is shifted into the device, MSB first.

### Functional Block Diagram



**Figure 21. Block Diagram of One DAC**

## Application and Implementation

### Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## Application Information

### DAC Reference (REF)

The external reference input features a typical input impedance of 333 k $\Omega$  and accepts an input voltage from 2 V to  $V_{DD}$ . Connect an external voltage supply between REF and GND to apply an external reference.

### Serial Interface

The TPC116S8U/TPC112S8U 3-wire serial interface is compatible with MICROWIRE, SPI, QSPI, and DSP. The interface provides three inputs: SCLK,  $\overline{\text{SYNC}}$ , and DIN. The chip-select input ( $\overline{\text{SYNC}}$ ) frames the serial data loading at DIN. Following a chip-select input high-to-low transition, the data is shifted synchronously and latched into the input register on each falling edge of the serial-clock input (SCLK). Each serial word is 16 bits for the TPC112S8U and 24 bits for the TPC116S8U. The first 3 bits are the control bits followed by 1 power-down bit as well as 12 data bits (MSB first) for the TPC112S8U and 22 data bits (MSB first) for the TPC116S8U as shown in Table 3 and Table 4. The serial input register transfers its contents to the input registers after loading 16/24 bits of data and updates the DAC output immediately after the data is received on the 16-/24-bit falling edge of the clock. To initiate a new data transfer,  $\overline{\text{SYNC}}$  is driven high and kept for a minimum of 20 ns before the next write sequence. The SCLK can be either high or low between  $\overline{\text{SYNC}}$  write pulses. Figure 1 and Figure 2 show the timing diagrams for the complete 3-wire serial interface transmission. The DAC code of the TPC116S8U is unipolar binary with  $V_{OUT} = (\text{code}/65,536) \times V_{REF}$ , and that of the TPC112S8U is with  $V_{OUT} = (\text{code}/4,096) \times V_{REF}$ .

**Table 3. Operating Mode Truth Table (TPC112S8U)**

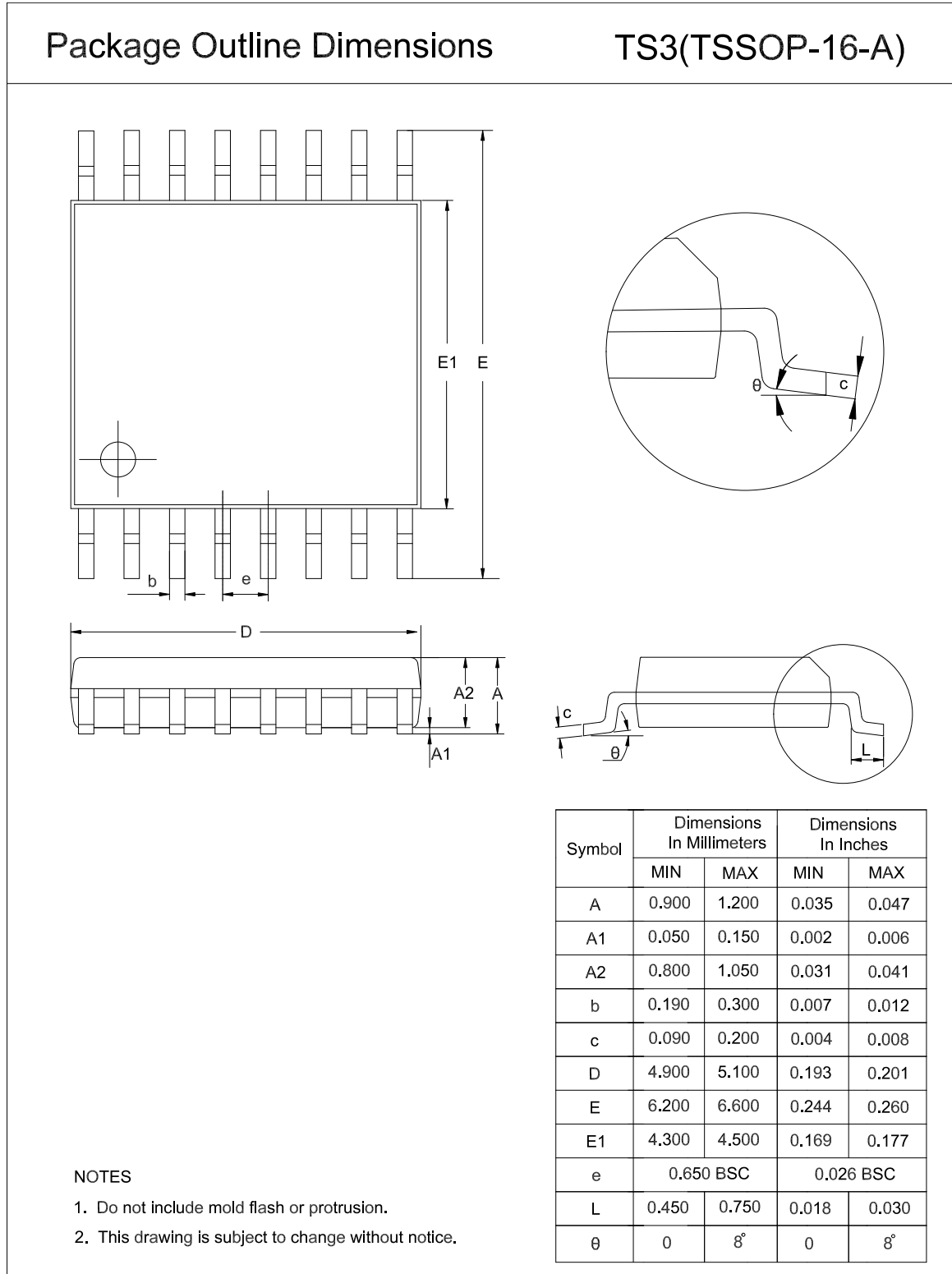
16-Bit Word					Function
A2	A1	A0	PD	DAC Data Bit	
D15	D14	D13	D12	D11 ~ D0	
0	0	0	0	X	Update DAC A Data
0	0	1	0	X	Update DAC B Data
0	1	0	0	X	Update DAC C Data
0	1	1	0	X	Update DAC D Data
1	0	0	0	X	Update DAC E Data
1	0	1	0	X	Update DAC F Data
1	1	0	0	X	Update DAC G Data
1	1	1	0	X	Update DAC H Data
X	X	X	1	X	Power down (Output High Z)

**Octal 12-Bit, Low-Power, High-Performance DAC**
**Table 4. Operating Mode Truth Table (TPC116S8U)**

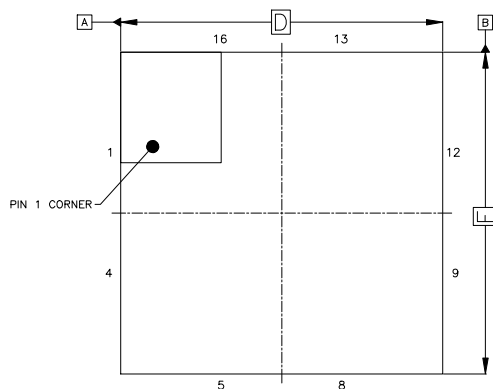
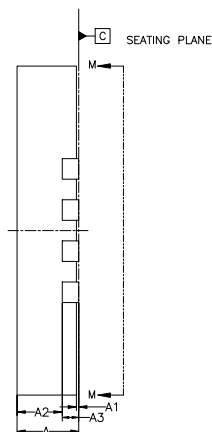
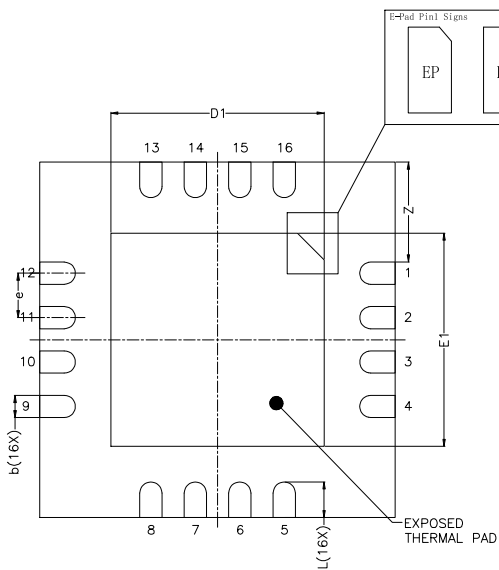
24-Bit Word									Function
MSB ( No content)				A2	A1	A0	PD	DAC Data Bit	
D23	D22	D21	D20	D19	D18	D17	D16	D15 ~ D0	
X	X	X	X	0	0	0	0	X	Update DAC A Data
X	X	X	X	0	0	1	0	X	Update DAC B Data
X	X	X	X	0	1	0	0	X	Update DAC C Data
X	X	X	X	0	1	1	0	X	Update DAC D Data
X	X	X	X	1	0	0	0	X	Update DAC E Data
X	X	X	X	1	0	1	0	X	Update DAC F Data
X	X	X	X	1	1	0	0	X	Update DAC G Data
X	X	X	X	1	1	1	0	X	Update DAC H Data
X	X	X	X	X	X	X	1	X	Power down (Output High Z)

## Package Outline Dimensions

### TSSOP16





**QFN4X4-16**
**Package Outline Dimensions**
**QFP(QFN4X4-16-B)**

**TOP VIEW**

**SIDE VIEW**

**BOTTOM VIEW**
**NOTES**

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.500	0.600	0.020	0.024
A3	0.203 REF		0.008 REF	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
e	0.500 BSC		0.020 BSC	
b	0.200	0.300	0.008	0.012
L	0.350	0.450	0.013	0.017
D1	2.300	2.500	0.091	0.098
E1	2.300	2.500	0.091	0.098
Z	1.125 BSC		0.044 BSC	

## Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC112S8U-TR	-40 to 125°C	TSSOP16	112S8U	1	Tape and Reel, 3,000	Green
TPC112S8U-QR	-40 to 125°C	QFN4X4-16	112S8U	1	Tape and Reel, 3,000	Green
TPC116S8U-TR <sup>(1)</sup>	-40 to 125°C	TSSOP16	116S8U	1	Tape and Reel, 3,000	Green
TPC116S8U-QR <sup>(1)</sup>	-40 to 125°C	QFN4X4-16	116S8U	1	Tape and Reel, 3,000	Green

(1) Samples could be provided in 3 months if needed.

**Green:** 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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