

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

Product Summary



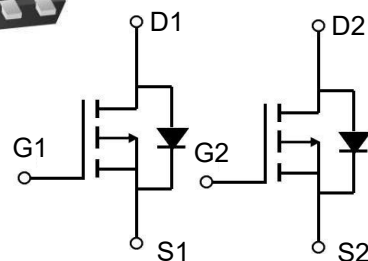
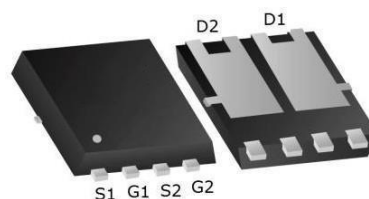
BVDSS	RDSON	ID
-30V	10.3mΩ	-40A

Description

The XR40K03D is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The XR40K03D meet the RoHS and Gree Product requirement 100% EAS guaranteed with full function reliability approved.

PDFN3333-8L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	-40	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	-25	A
I_{DM}	Pulsed Drain Current ²	-120	A
EAS	Single Pulse Avalanche Energy ³	45	mJ
I_{AS}	Avalanche Current	-30	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation ⁴	29.7	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	4.2	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	---	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-1A	---	10.3	13.5	mΩ
		V _{GS} =-4.5V, I _D =-1A	---	15	20	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1	-1.6	-2.5	V
$\Delta V_{GS(th)}$	V _{GS(th)} Temperature Coefficient		---	---	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-30V, V _{GS} =0V, T _J =25°C	---	---	-1	uA
		V _{DS} =-30V, V _{GS} =0V, T _J =100°C	---	---	-5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-15A	---	15	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	11	---	Ω
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V, I _D =-15A	---	30	---	nC
Q _{gs}	Gate-Source Charge		---	5.5	---	
Q _{gd}	Gate-Drain Charge		---	8	---	
T _{d(on)}	Turn-On Delay Time	V _{GS} =-10V, V _{DS} =-15V, I _D =-15A, R _{GEN} =2.5Ω	---	10	---	ns
T _r	Rise Time		---	15	---	
T _{d(off)}	Turn-Off Delay Time		---	110	---	
T _f	Fall Time		---	70	---	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	1450	---	pF
C _{oss}	Output Capacitance		---	177	---	
C _{rss}	Reverse Transfer Capacitance		---	147	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	-40	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-30A, T _J =25°C	---	---	-1.2	V

Note :

1. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C.
2. The EAS data shows Max. rating . The test condition is V_{DD}= -25V, V_{GS}= -10V, L= 0.1mH, I_{AS}= -30A.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 20Z copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Characteristics

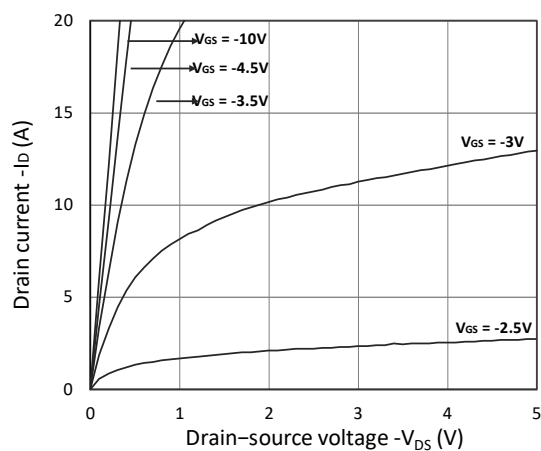


Figure 1. Output Characteristics

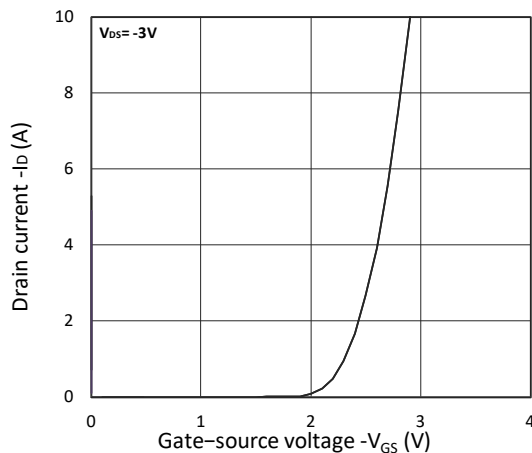


Figure 2. Transfer Characteristics

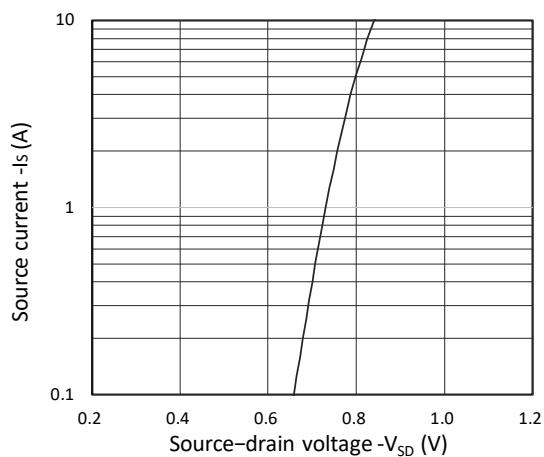


Figure 3. Forward Characteristics of Reverse

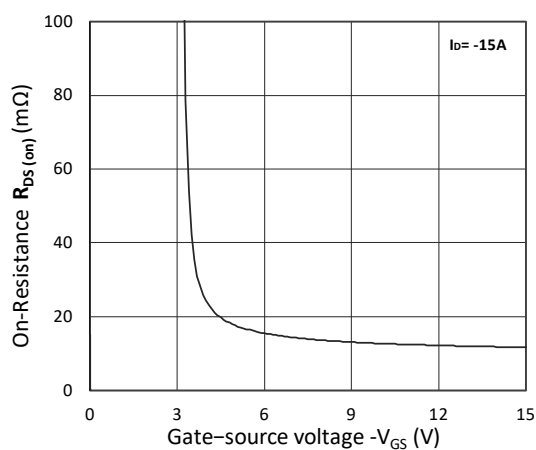


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

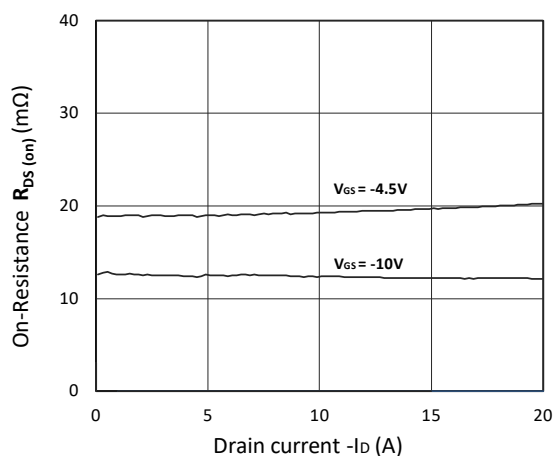


Figure 5. $R_{DS(ON)}$ vs. I_D

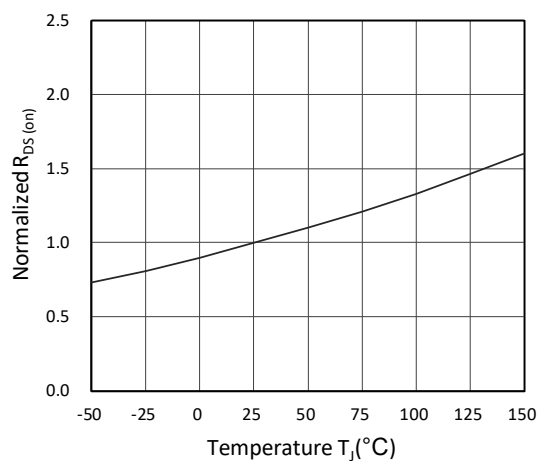


Figure 6. Normalized $R_{DS(ON)}$ vs. Temperature

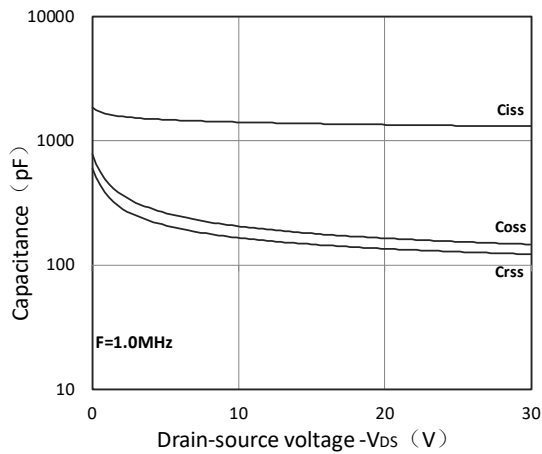


Figure 7. Capacitance Characteristics

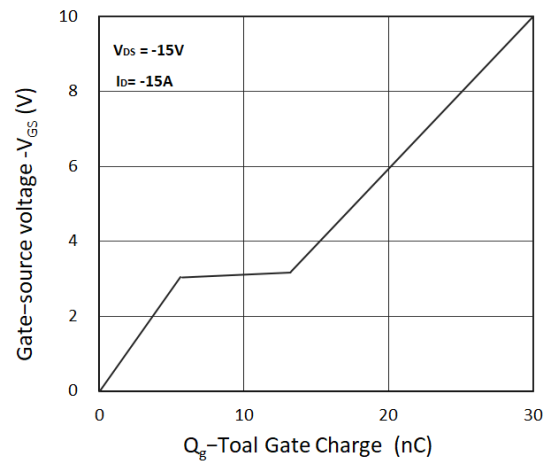


Figure 8. Gate Charge Characteristics

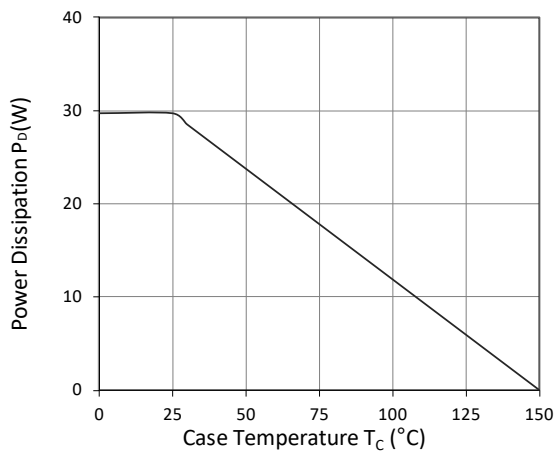


Figure 9. Power Dissipation

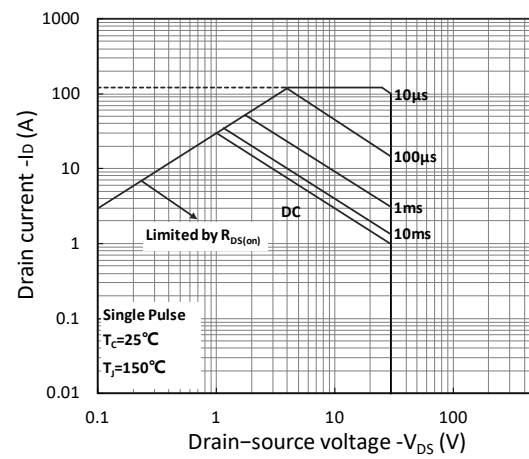


Figure 10. Safe Operating Area

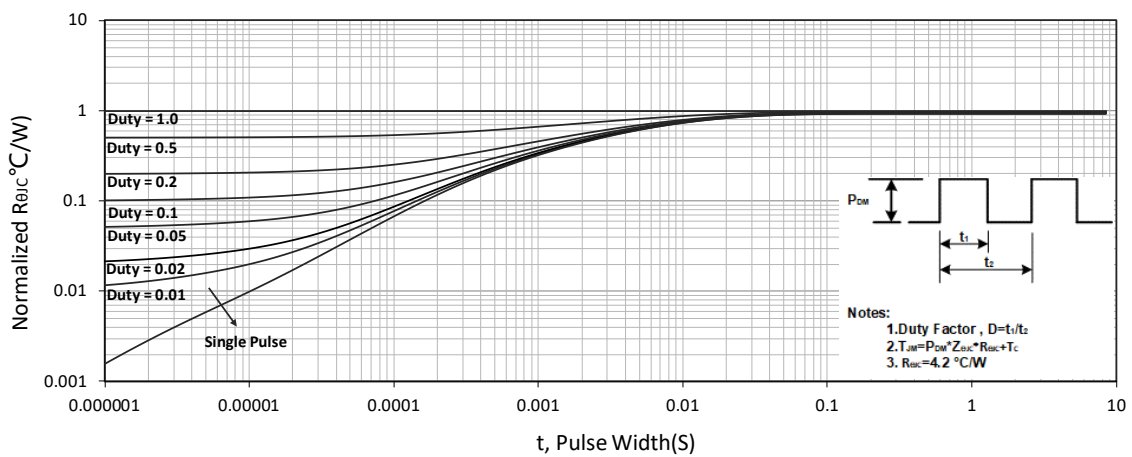


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

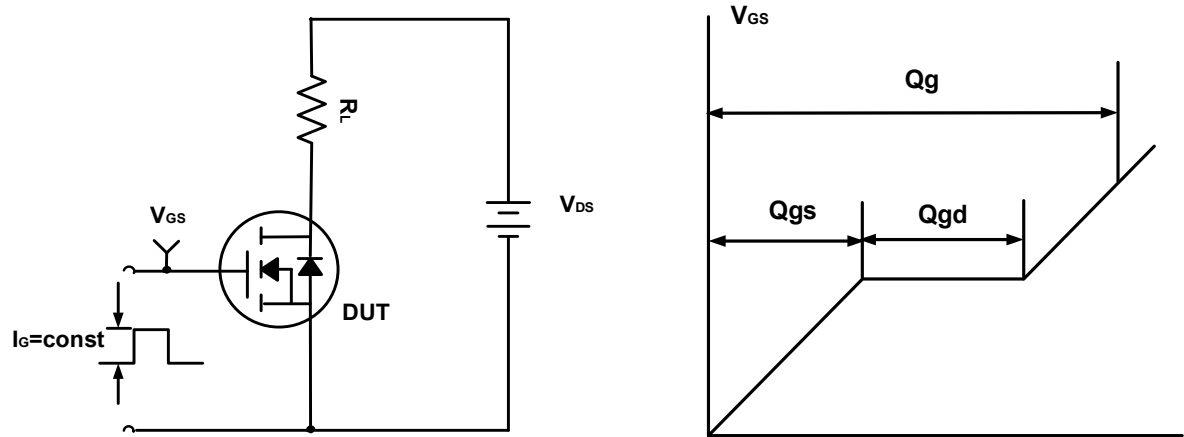


Figure A. Gate Charge Test Circuit & Waveforms

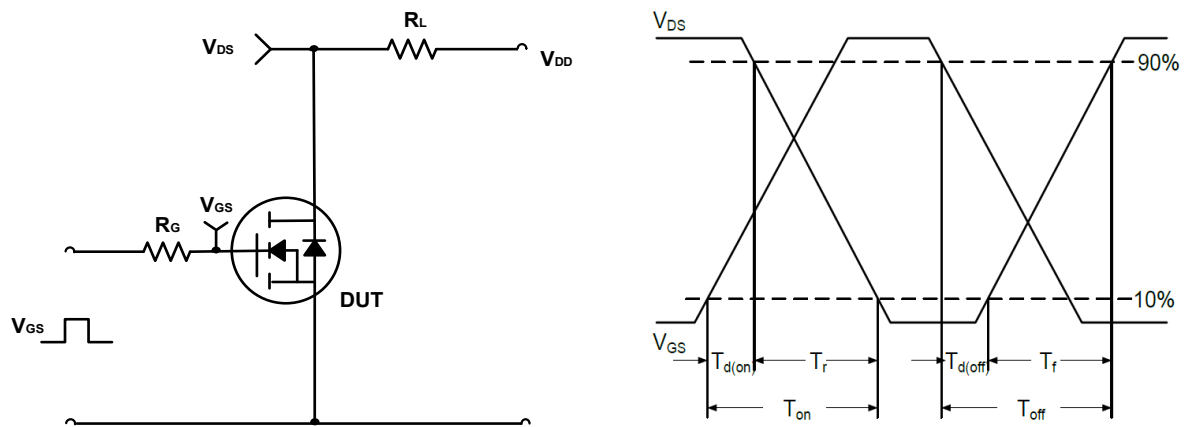


Figure B. Switching Test Circuit & Waveforms

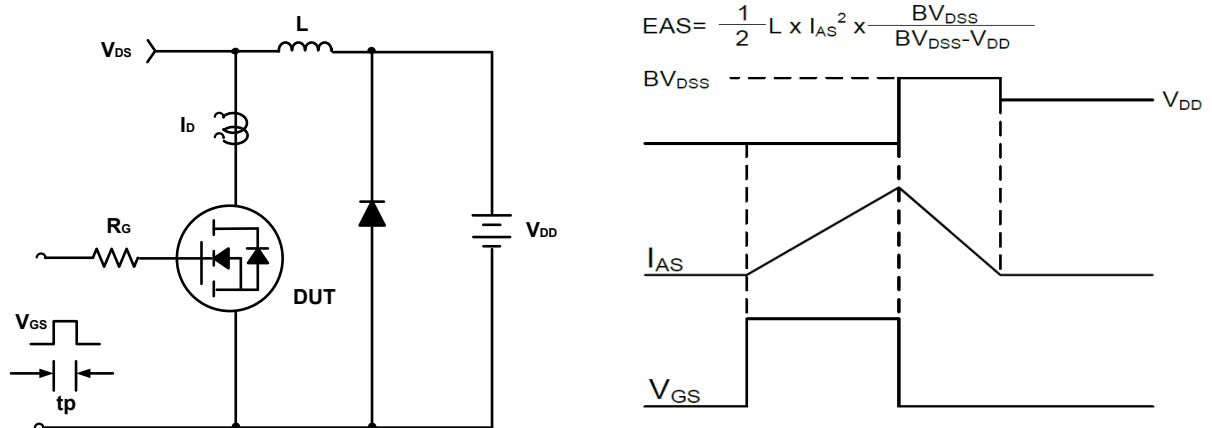
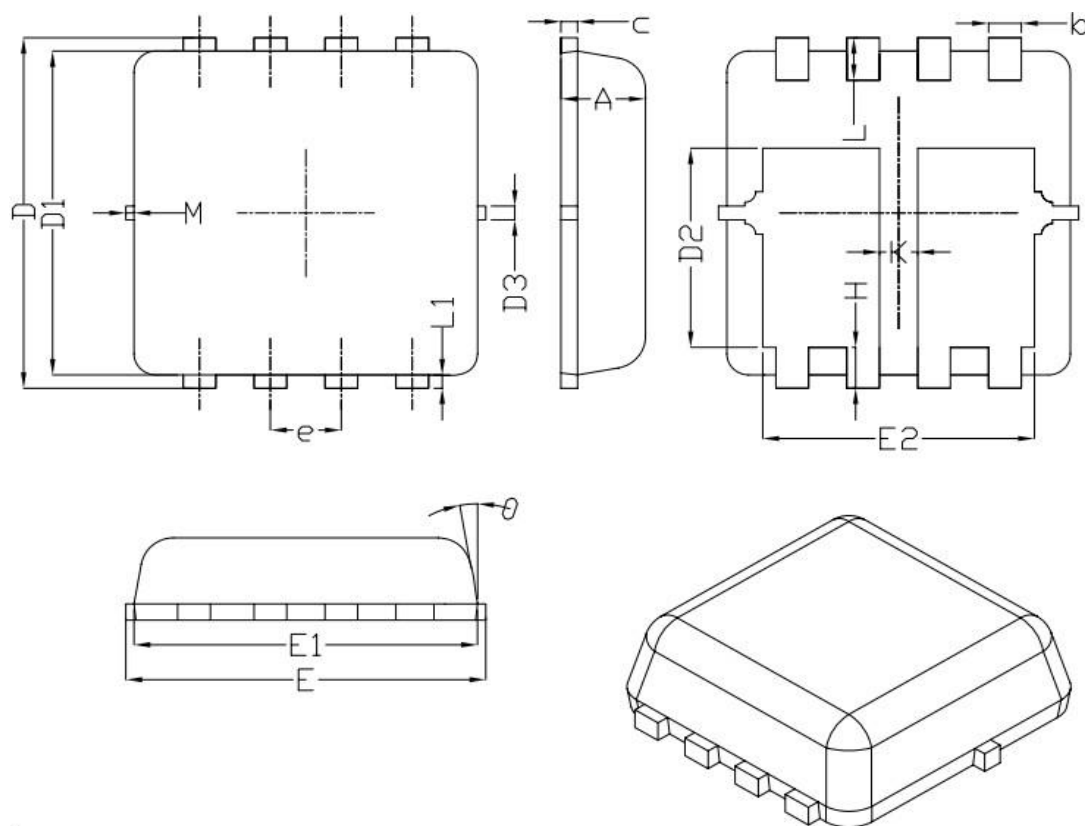


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Dual PDFN3333-8L Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	--
K	0.30	--	--
θ	--	10°	12°
M	*	*	0.15
* Not Specified			

Notes:

1. Refer to JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion.