NXS0506GU-Q100

SD 3.0-compatible memory card integrated auto-direction control and level translator with EMI filter and ESD protection

Rev. 2.1 — 31 July 2024 Product data sheet

1. General description

The NXS0506GU-Q100 is an SD 3.0-compatible bidirectional dual supply level translator with auto-direction control. It is designed to interface between a memory card operating at 1.7 V to 3.6 V signal levels and a host with a nominal supply voltage of 1.1 V to 1.95 V. The device supports SD 3.0: SDR104, SDR50, DDR50, SDR25, SDR12 and SD 2.0 High-Speed (50 MHz) and Default-Speed (25 MHz) modes. The device has a built-in EMI filter and robust ESD protection (IEC 61000-4-2, level 4).

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 2) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 2)
  - Specified from -40 °C to +85 °C and from -40 °C to +105 °C
- Supports up to 208 MHz clock rate
- SD 3.0 specification-compatible voltage translation to support: SDR104, SDR50, DDR50, SDR25, SDR12, High-Speed and Default-Speed modes
- 1.1 V to 1.95 V host side interface voltage support
- Auto-direction sensing
- Low power consumption
- Integrated pull-up resistors: no external resistors required
- Integrated EMI filters suppress higher harmonics of digital I/Os
- Level shifting buffers keep ESD stress away from the host (zero-clamping concept)
- 16-terminal XQFN16 package; pitch 0.4 mm
- Latch-up performance exceeds 100 mA per JESD78 Class II.A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
  - IEC61000-4-2, level 4, contact discharge on all memory card-side pins exceeds 8000 V
  - IEC61000-4-2, level 4, air discharge on all memory card-side pins exceeds 15000 V

3. Applications

- Smartphone
- Mobile handsets
- Digital cameras
- Tablet PCs
- Laptop computers
- SD, MMC or microSD card readers

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NXS0506GU-Q100	-40 °C to +105 °C	XQFN16	plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 × 2.60 × 0.50 mm	SOT1161-1

5. Marking

Table 2. Marking codes

Type number	Marking code
NXS0506GU-Q100	m5

6. Block diagram

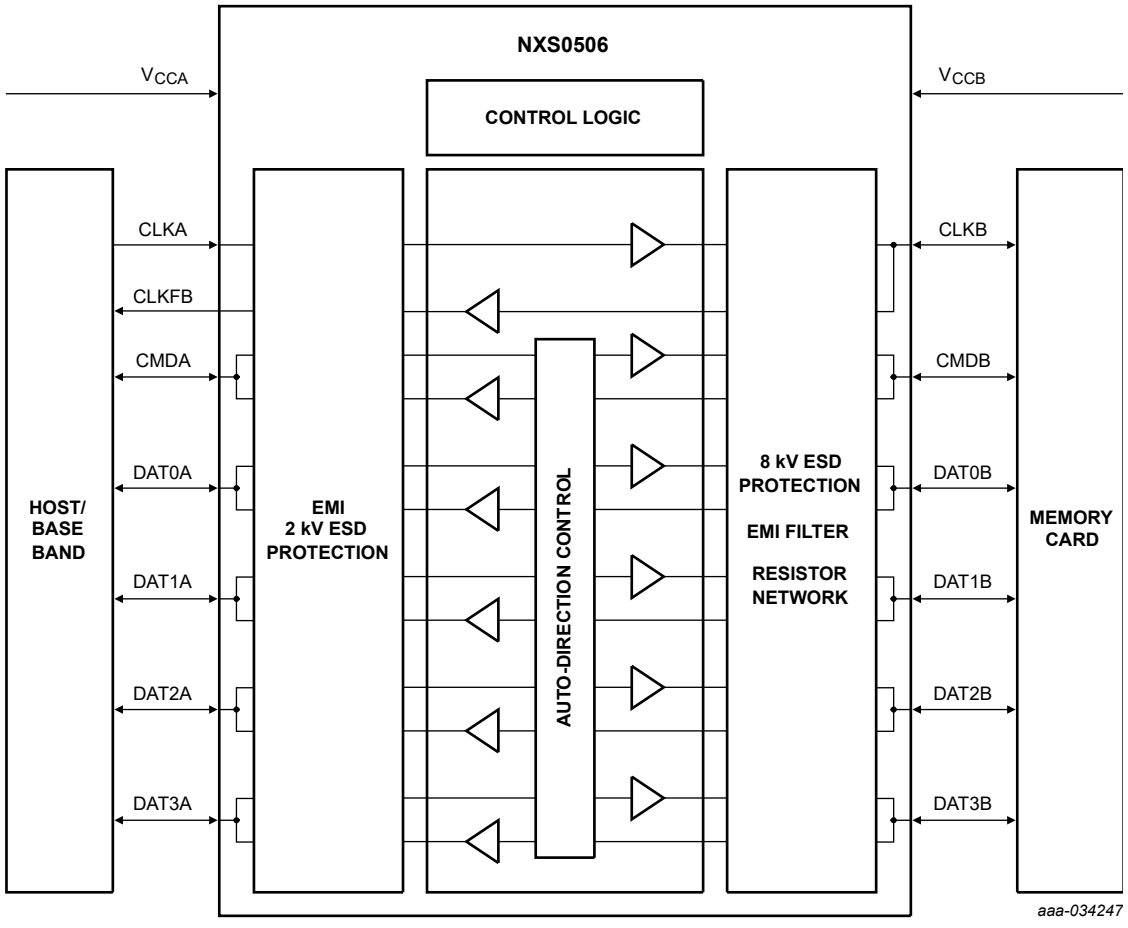
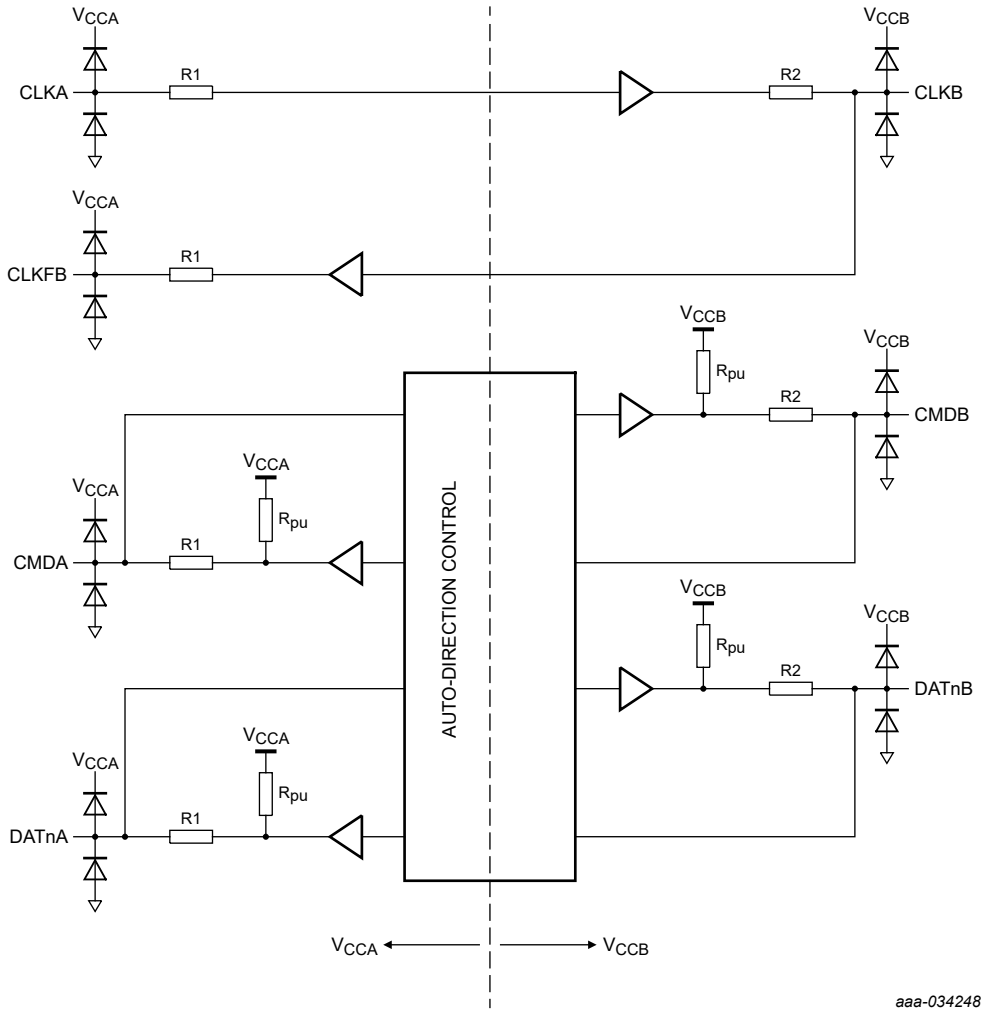


Fig. 1. Block diagram

7. Functional diagram

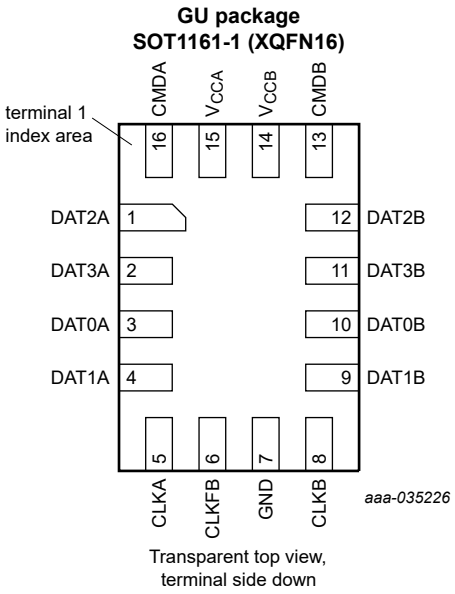


Only one data input/output channel (DATnA/DATnB) shown.

Fig. 2. Functional diagram

8. Pinning information

8.1. Pinning



8.2. Pin description

Table 3. Pin description

Symbol[1]	Pin	Description
DAT2A	1	data 2 input or output on host side
DAT3A	2	data 3 input or output on host side
DAT0A	3	data 0 input or output on host side
DAT1A	4	data 1 input or output on host side
V_{CCA}	15	supply voltage A (host side)
CMDA	16	command input or output on host side
CLKFB	6	clock feedback signal on host side, this pin can be left floating
CLKA	5	clock signal input on host side
V_{CCB}	14	supply voltage B (memory card side)
CMDB	13	command input or output on memory card side
GND	7	supply ground
CLKB	8	clock signal input on memory card side
DAT2B	12	data 2 input or output on memory card side
DAT3B	11	data 3 input or output on memory card side
DAT0B	10	data 0 input or output on memory card side
DAT1B	9	data 1 input or output on memory card side

[1] The pin names relate particularly to SD memory cards, but also apply to microSD and MMC memory cards. See Section 9.6 for options to swap identical channels.

9. Functional description

9.1. Level translator

The bidirectional level translator shifts the data between the I/O supply levels of the host and the memory card. Auto direction sensing circuitry determines if a command and data signals are transferred from the memory card to the host (card read mode) or from the host to the memory card (card write mode). The voltage translator has to support several clock and data transfer rates at the signaling levels specified in the SD 3.0 standard specification.

Table 4. Supported modes

Bus speed mode	Signal level (V)	Clock rate (MHz)	Data rate (MB/s)
Default-Speed	3.3	25	12.5
High-Speed	3.3	50	25
SDR12	1.8	25	12.5
SDR25	1.8	50	25
SDR50	1.8	100	50
SDR104	1.8	208	104
DDR50	1.8	50	50

9.2. Enable and direction control

The device contains an auto-enable feature. If V_{CCB} rises above 1.5 V, the level translator logic is enabled automatically. As soon as V_{CCB} drops below 0.65 V, the memory card side drivers and the level translator logic are disabled. All pins on the host side, excluding CLKA are configured as inputs with a 70 kΩ resistor pulled up to V_{CCA}.

The device features an auto correction control for all data channels except CLK. For these pins the direction of data flow is sensed by the direction control logic and the output drivers are controlled accordingly. There is no need for the host interface to indicate the direction of data flow.

9.3. Feedback clock channel

The clock is transmitted from the host to the memory card side. The voltage translator and the Printed-Circuit Board (PCB) tracks introduce some amount of delay. It reduces timing margin for data read back from memory card, especially at higher data rates. Therefore, a feedback path is provided to compensate the delay. The reasoning behind this approach is the fact that the clock is always delivered by the host, while the data in the timing critical read mode comes from the card.

9.4. EMI filter

All input/output driver stages are equipped with EMI filters to reduce interference towards sensitive mobile communication.

9.5. ESD protection

The device has robust ESD protections on all memory card pins. The architecture prevents any stress for the host: the voltage translator discharges any stress to supply ground.

9.6. Pin and channel naming

The channel/pin naming as shown in Fig. 2 and in Section 8 aims at using NXS0506GU-Q100 for SD-card interfaces. The sequence of the channels is chosen to easily connect to SD-card connectors. As the internal design of channels DAT0 (pins DAT0A and DAT0B), DAT1 (pins DAT1A and DAT1B), DAT2 (pins DAT2A and DAT2B), DAT3 (pins DAT3A and DAT3B) and CMD (pins CMDA and CMDB) is identical, these channels can be exchanged. Swapping channels in the above mentioned group can help ease PCB layout issues. E.g. DAT0 can be swapped with DAT1 or DAT3 with CMD without impact on functionality of NXS0506GU-Q100.

10. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage	4 ms transient; on pin V_{CCA}		-0.5	4.6	V
		4 ms transient; on pin V_{CCB}		-0.5	4.6	V
I_{IK}	input clamping current	V_I < -0.3 V or V_I > V_{CC} +0.3 V	[1]	-	±20	mA
V_I	input voltage	4 ms transient at I/O pins		-0.5	4.6	V
I_{OK}	output clamping current	V_O < -0.3 V or V_O > V_{CCA} +0.3 V	[1]	-	±20	mA
		V_O < -0.3 V or V_O > V_{CCB} +0.3 V	[1]	-	±50	mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to +105 °C		-	250	mW
T_{stg}	storage temperature			-55	+150	°C
$I_{lu(IO)}$	input/output latch-up current	JESD78F: -0.5V_{CC} < V_I < 1.5V_{CC}; T_j < 125 °C		-100	100	mA

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

11. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	on pin V_{CCA}	[1]	1.1	-	1.95	V
		on pin V_{CCB}	[1]	1.7	-	3.6	V
V_I	input voltage	host side		-0.3	-	V_{CCA} + 0.3	V
		memory card side	[2]	-0.3	-	V_{CCB} + 0.3	V
T_{amb}	ambient temperature			-40	+25	+105	°C

[1] $V_{CCB} \geq V_{CCA}$
[2] The voltage must not exceed 3.6 V.

Table 7. Integrated resistors

Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +105 °C		Unit
				Min	Typ[1]	Max	Min	Max	
R_{pu}	pull-up resistance			42	70	100	42	100	kΩ
R_s	series resistance	host side; R1	[2]	-	22.5	-	-	-	Ω
		card side; R2	[2]	-	15	-	-	-	Ω

[1] Typical values are measured at T_{amb} = 25 °C.
[2] Guaranteed by design and characterization.

12. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V) unless otherwise specified.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +105 °C		Unit
			Min	Typ[1]	Max	Min	Max	
Automatic enable feature: V_{CCB}								
V_{en}	device enable voltage level	V_{CCA} ≥ 1.0 V; V_{CCB} rising edge	0.9	1.2	1.5	0.9	1.5	V
V_{dis}	device disable voltage level	V_{CCA} ≥ 1.0 V; V_{CCB} falling edge	0.65	1.0	1.3	0.65	1.3	V
Host-side input signals: CMDA, DAT0A to DAT3A and CLKA								
V_{IH}	HIGH-level input voltage	1.1 V ≤ V_{CCA} ≤ 1.95 V	0.65V_{CCA}	-	V_{CCA} + 0.3	0.65V_{CCA}	V_{CCA} + 0.3	V
V_{IL}	LOW-level input voltage	1.1 V ≤ V_{CCA} ≤ 1.95 V	-0.3	-	0.35V_{CCA}	-0.3	0.35V_{CCA}	V
I_I	input leakage current	CLKA; V_{CCA} = 1.95 V; V_I = 0 V to 1.95 V	-	-	1	-	1	µA
Host-side output signals: CMDA and DAT0A to DAT3A								
V_{OH}	HIGH-level output voltage	I_O = -2 µA; V_I = V_{IH} (card side); 1.1 V ≤ V_{CCA} ≤ 1.95 V	0.8V_{CCA}	-	V_{CCA} + 0.3	0.8V_{CCA}	V_{CCA} + 0.3	V
V_{OL}	LOW-level output voltage	I_O = 2 mA; V_I = V_{IL} (card side); 1.1 V ≤ V_{CCA} ≤ 1.95 V	-0.3	-	0.15V_{CCA}	-0.3	0.15V_{CCA}	V
Host-side output signals: CLKFB								
V_{OH}	HIGH-level output voltage	I_O = -2 mA; V_I = V_{IH} (host side); 1.1 V ≤ V_{CCA} ≤ 1.95 V	0.8V_{CCA}	-	V_{CCA} + 0.3	0.8V_{CCA}	V_{CCA} + 0.3	V
V_{OL}	LOW-level output voltage	I_O = 2 mA; V_I = V_{IL} (host side); 1.1 V ≤ V_{CCA} ≤ 1.95 V	-0.3	-	0.15V_{CCA}	-0.3	0.15V_{CCA}	V
Card-side input signals: CMDB and DAT0B to DAT3B								
V_{IH}	HIGH-level input voltage	1.7 V ≤ V_{CCB} ≤ 3.6 V	0.625V_{CCB}	-	V_{CCB} + 0.3	0.625V_{CCB}	V_{CCB} + 0.3	V
V_{IL}	LOW-level input voltage	1.7 V ≤ V_{CCB} ≤ 1.95 V	-0.3	-	0.35V_{CCB}	-0.3	0.35V_{CCB}	V
		2.7 V ≤ V_{CCB} ≤ 3.6 V	-0.3	-	0.30V_{CCB}	-0.3	0.30V_{CCB}	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +105 °C		Unit
			Min	Typ[1]	Max	Min	Max	
Card-side output signal: CMDB, DAT0B to DAT3B and CLKB								
V_{OH}	HIGH-level output voltage	CLKB; V_{CCB} = 1.7 V; I_O = -2 mA; $V_I = V_{IH}$ (host side)	$0.85V_{CCB}$	-	2.0	$0.85V_{CCB}$	2.0	V
		CLKB; V_{CCB} = 2.7 V; I_O = -4 mA; $V_I = V_{IH}$ (host side)	$0.85V_{CCB}$	-	V_{CCB} + 0.3	$0.85V_{CCB}$	V_{CCB} + 0.3	V
		CMDB, DATnB; V_{CCB} = 1.7 V; I_O = -2 µA; $V_I = V_{IH}$ (host side)	$0.85V_{CCB}$	-	2.0	$0.85V_{CCB}$	2.0	V
V_{OL}	Low-level output voltage	I_O = 2 mA; $V_I = V_{IL}$ (host side); V_{CCB} = 1.7 V	-0.3	-	$0.125V_{CCB}$	-0.3	$0.125V_{CCB}$	V
		I_O = 4 mA; $V_I = V_{IL}$ (host side); V_{CCB} = 2.7 V	-0.3	-	$0.125V_{CCB}$	-0.3	$0.125V_{CCB}$	V
Current consumption								
I_{CC}	supply current	host side; all inputs = HIGH; $V_I = V_{CCA}$; V_{CCA} = 1.95 V; V_{CCB} = 3.6 V	-	-	4	-	10	µA
		card side; all inputs = HIGH; $V_I = V_{CCA}$; V_{CCA} = 1.7 V; V_{CCB} = 1.7 V	-	-	7	-	15	µA
		card side; all inputs = HIGH; $V_I = V_{CCA}$; V_{CCA} = 1.95 V; V_{CCB} = 3.6 V	-	-	20	-	50	µA

[1] Typical values are measured at T_{amb} = 25 °C.

13. Dynamic characteristics

13.1. Level translator

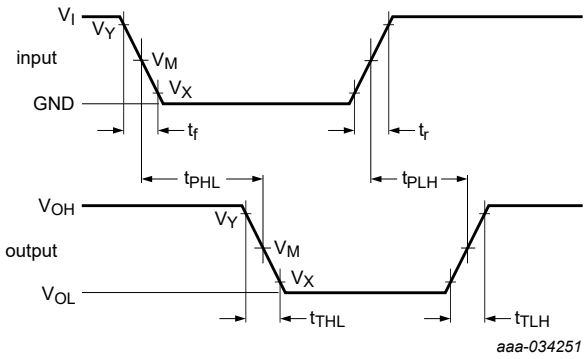
Table 9. Level translator dynamic characteristics

At recommended operating conditions; For waveform and test circuit see Fig. 3 and Fig. 4.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +105 °C		Unit
			Min	Typ[1]	Max	Min	Max	
Host-side output transition times								
t_t	transition time	V_{CCA} = 1.2 V to 1.8 V; output transition time between $V_X = 0.35V_{CCA}$ and $V_Y = 0.65V_{CCA}$ [2]	-	0.3	1.0	-	1.0	ns
Host-side input rise and fall times								
t_r, t_f	rise and fall time	V_{CCA} = 1.2 V to 1.8 V; input rise and fall time between $V_X = 0.35V_{CCA}$ and $V_Y = 0.65V_{CCA}$	-	0.4	1.0	-	1.0	ns
Card-side output transition times								
t_t	transition time	V_{CCB} = 1.8 V; output transition time between V_X = 0.45 V and V_Y = 1.4 V [2]	0.4	0.88	1.32	-	1.32	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +105 °C		Unit
			Min	Typ[1]	Max	Min	Max	
Card-side input rise and fall times								
t_r	rise time	V_{CCB} = 1.8 V; input rise time between 0.58 V and 1.27 V	0.2	0.5	0.96	-	0.96	ns
t_f	fall time	V_{CCB} = 1.8 V; input fall time between 0.58 V and 1.27 V	0.2	0.45	0.96	-	0.96	ns
Host-side to card-side propagation delay; DATnA to DATnB, CMDA to CMDB and CLKA to CLKB								
t_{pd}	propagation delay	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V [3]	-	3.1	5.4	-	5.4	ns
		V_{CCA} = 1.2 V; V_{CCB} = 3.3 V [3]	-	2.2	4.0	-	4.0	ns
		V_{CCA} = 1.8 V; V_{CCB} = 1.8 V [3]	-	2.7	4.8	-	4.8	ns
		V_{CCA} = 1.8 V; V_{CCB} = 3.3 V [3]	-	1.7	3.1	-	3.1	ns
$t_{sk(o)}$	output skew time	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V	-	-	200	-	250	ps
		V_{CCA} = 1.2 V; V_{CCB} = 3.3 V	-	-	200	-	250	ps
		V_{CCA} = 1.8 V; V_{CCB} = 1.8 V	-	-	200	-	250	ps
		V_{CCA} = 1.8 V; V_{CCB} = 3.3 V	-	-	200	-	250	ps
Card-side to host-side propagation delay; DATnB to DATnA and CMDB to CMDA								
t_{pd}	propagation delay	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V [3]	-	2.7	4.6	-	4.6	ns
		V_{CCA} = 1.2 V; V_{CCB} = 3.3 V [3]	-	1.7	3.0	-	3.0	ns
		V_{CCA} = 1.8 V; V_{CCB} = 1.8 V [3]	-	2.7	4.6	-	4.6	ns
		V_{CCA} = 1.8 V; V_{CCB} = 3.3 V [3]	-	1.6	2.7	-	2.7	ns
$t_{sk(o)}$	output skew time	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V	-	-	200	-	250	ps
		V_{CCA} = 1.2 V; V_{CCB} = 3.3 V	-	-	200	-	250	ps
		V_{CCA} = 1.8 V; V_{CCB} = 1.8 V	-	-	200	-	250	ps
		V_{CCA} = 1.8 V; V_{CCB} = 3.3 V	-	-	200	-	250	ps
Host-side to host-side propagation delay; CLKA to CLKFB								
t_{pd}	propagation delay	V_{CCA} = 1.2 V; V_{CCB} = 1.8 V [3]	-	5.8	10	-	10	ns
		V_{CCA} = 1.2 V; V_{CCB} = 3.3 V [3]	-	3.9	7.0	-	7.0	ns
		V_{CCA} = 1.8 V; V_{CCB} = 1.8 V [3]	-	5.4	9.4	-	9.4	ns
		V_{CCA} = 1.8 V; V_{CCB} = 3.3 V [3]	-	3.3	5.8	-	5.8	ns
Bus signal equivalent capacitance								
$C_{I/O}$	input/output capacitance	V_I = 0 V; f_i = 1 MHz; V_{CCA} = 1.8 V; host side [4]	-	5.0	-	-	-	pF
		V_I = 0 V; f_i = 1 MHz; V_{CCB} = 1.8 V; card side [4]	-	12.0	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] t_{pd} is the same as t_{PLH} and t_{PHL}.
[4] EMI filter line capacitance from I/O driver to pin; $C_{I/O}$ is guaranteed by design.



Measurement points are given in Table 10.

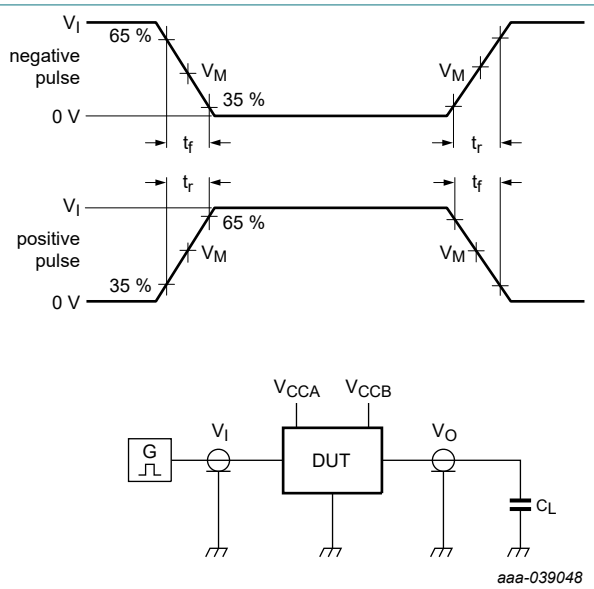
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 3. The input to output propagation delays, input rise and fall times and output transition times

Table 10. Measurement points

Supply voltage		Input		Output
V_{CCA}	V_{CCB}	V_I [1]	V_M [1]	V_M [2]
1.1 V to 1.95 V	1.7 V to 3.6 V	V_{CCI}	$0.5V_{CCI}$	$0.5V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{CCO} is the supply voltage associated with the output.



Test data is given in Table 11.

All input pulses are supplied by generators having the following characteristics:

PRR ≤ 10 MHz, Z_O = 50 Ω, input edges (t_r, t_f) are defined in Section 13.

Definitions test circuit:

C_L = Load capacitance including jig and probe capacitance;

Fig. 4. Test circuit for measuring switching time

Table 11. Test data

Supply voltage		Input	Load	
V_{CCA}	V_{CCB}	V_I [1]	C_L (host side)	C_L (card side)
1.1 V to 1.95 V	1.7 V to 3.6 V	V_{CCI}	10 pF	15 pF

[1] V_{CCI} is the supply voltage associated with the input.

14. Application information

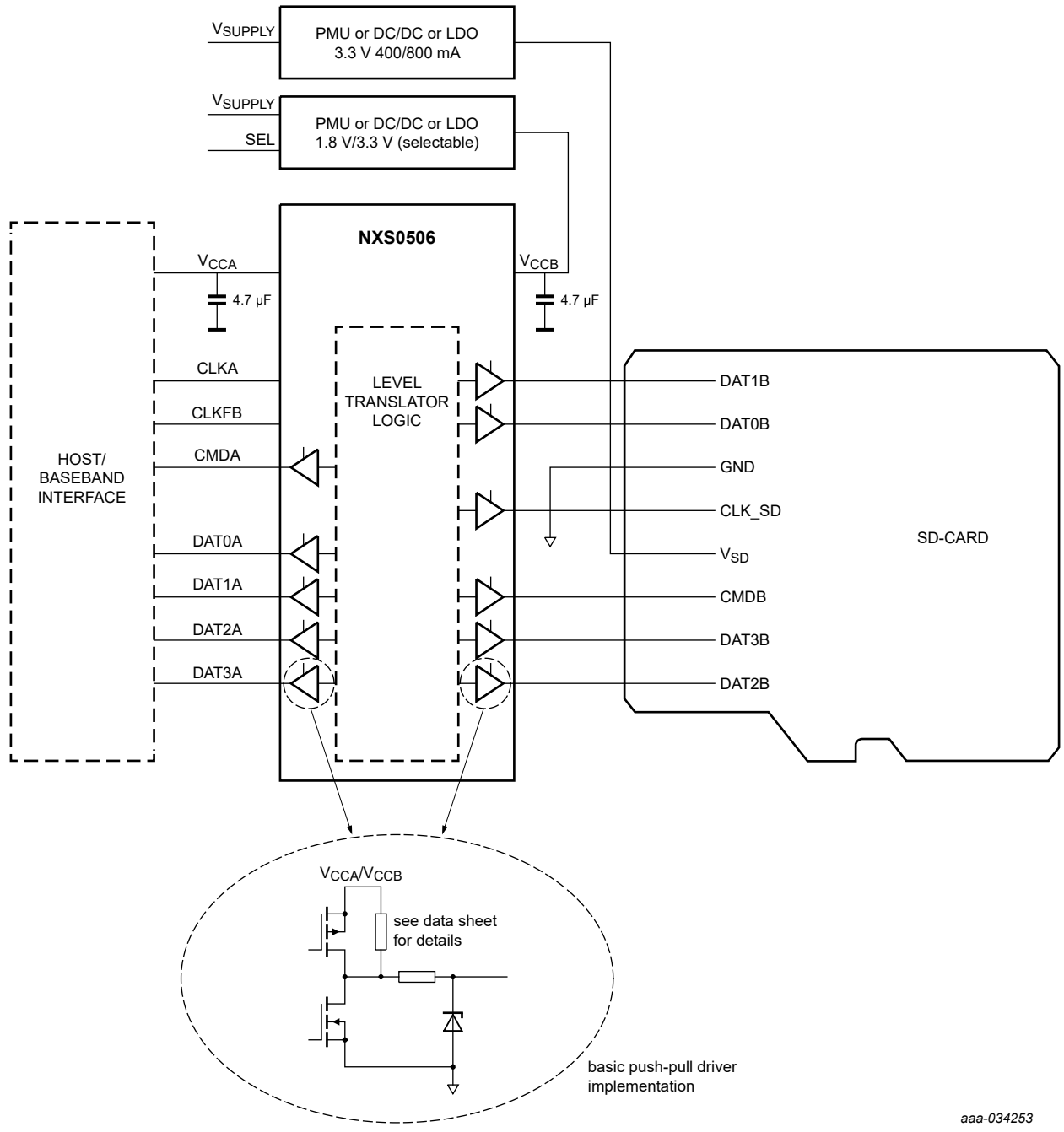


Fig. 5. Application diagram

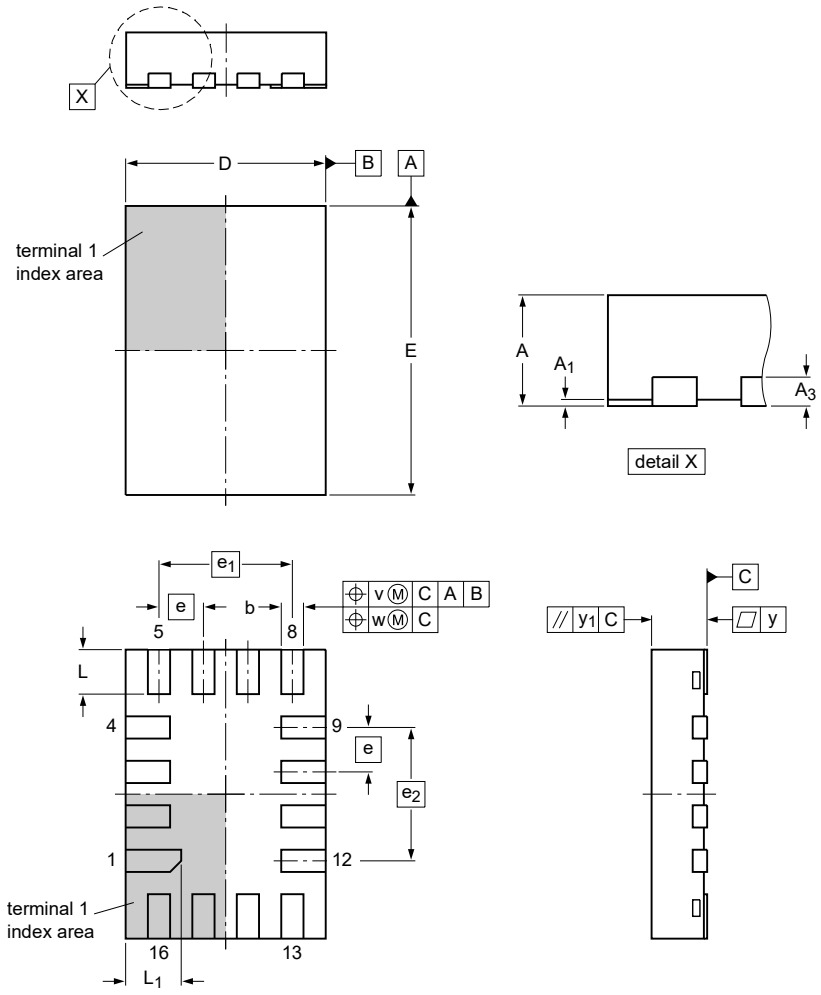
14.1. PCB design guidelines

The translator can operate with frequencies up to 208 MHz so the PCB connections between host and translator and translator and card can start to act as transmission lines, affecting the signal integrity.

For PCB connections below 8 cm (t_r = 0.4 ns) no degradation of the signal integrity is to be expected. For longer connections it's important to take pre-cautions and check the signal integrity during the development phase of the PCB. If the CLKFB is used to synchronize the data that is read from the card, it is important to place the translator as close as possible to the card connector.

15. Package outline

XQFN16: plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 x 2.60 x 0.50 mm **SOT1161-1**



Dimensions

Unit[1]		A	A_1	A_3	b	D	E	e	e_1	e_2	L	L_1	v	w	y	y_1
	max	0.5	0.05		0.25	1.9	2.7				0.45	0.55				
mm	nom			0.127	0.20	1.8	2.6	0.4	1.2	1.2	0.40	0.50	0.1	0.05	0.05	0.05
	min		0.00		0.15	1.7	2.5				0.35	0.45				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1161-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1161-1	- - -	- - -	- - -			~~09-12-28~~ 09-12-29

Fig. 6. Package outline SOT1161-1 (XQFN16)

16. Abbreviations

Table 12. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
DUT	Device Under Test
EMI	Electro Magnetic Interface
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
FR4	Flame Retard 4
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
LDO	Low-Dropout
MMC	MultiMedia Card
NSMD	Non-Solder Mask PCB Design
OSP	Organic Solderability Preservation
PCB	Printed-Circuit Board
PMU	Project Management Unit
PRR	Pulse Rate Repetition
RoHS	Restriction of Hazardous Substances
SD	Secure Digital

17. Revision history

Table 13. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NXS0506GU_Q100 v.2.1	20240731	Product data sheet	-	NXS0506GU_Q100 v.2
NXS0506GU_Q100 v.2	20240202	Product data sheet	-	NXS0506GU_Q100 v.1
Modifications:	• Fig. 2 updated. • Table 5: input and output clamping current added.			
NXS0506GU_Q100 v.1	20231030	Product data sheet	-	-

18. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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