

## PDFN5060 Plastic-Encapsulate MOSFETS

### Features

- $V_{DS}=100V$
- $I_D=100A$
- $R_{DS(on)}@V_{GS}=10V < 5.7m\Omega$
- $R_{DS(on)}@V_{GS}=4.5V < 8m\Omega$
- High density cell design for ultra low Rdson
- Advanced Split Gate Trench Technology
- Fast Switching Speedze

**Drain-source Voltage**

100 V

**Drain Current**

100 Ampere

### Applications

- DC-DC Converters
- Motor Control
- Portable equipment application

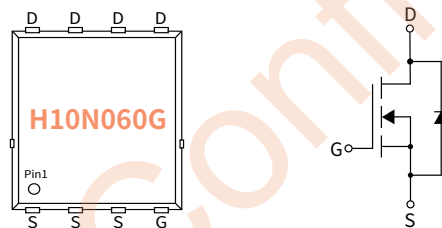
### Mechanical Data

- Case: PDFN5060  
Molding compound meets UL 94V-0 flammability rating, RoHS-compliant,halogen-free
- Terminals: Solder plated, solderable per MIL-STD-750,Method 2026

PDFN5060



### Function Diagram



### Ordering Information

PACKAGE	PACKAGE CODE	UNIT WEIGHT(g)	REEL(pcs)	BOX(pcs)	CARTON(pcs)	DELIVERY MODE
PDFN5060	R3	0.09	5000	10000	80000	13"

### Maximum Ratings (Ta=25°C Unless otherwise specified)

PARAMETER	SYMBOL	UNIT	VALUE
Drain-source Voltage	$V_{DS}$	V	100
Gate-source Voltage	$V_{GS}$	V	$\pm 20$
Drain Current	$I_D$	A	100
Pulsed Drain Current <sup>(1)</sup>	$I_{DM}$	A	400
Total Power Dissipation	$P_D$	W	150
Single pulse avalanche energy <sup>(2)</sup>	EAS	mJ	182
Junction temperature	$T_J$	°C	-55 ~+150
Storage temperature	$T_{stg}$	°C	-55 ~+150
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	°C / W	0.83

## ● Static Parameter Characteristics (T<sub>j</sub>=25°C Unless otherwise specified)

PARAMETER	SYMBOL	Condition	UNIT	Min	Typ	Max
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	V	100	—	—
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V	μA	—	—	1.0
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V	nA	—	—	±100
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	V	1.0	1.8	2.5
Static Drain-Source On-Resistance <sup>(3)</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =30A	mΩ	—	4.5	5.7
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =10A		—	6	8

## ● Dynamic Parameters

PARAMETER	SYMBOL	Condition	UNIT	Min	Typ	Max
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, f=1MHZ	pF	—	3168	—
Output Capacitance	C <sub>oss</sub>			—	1125	—
Reverse Transfer Capacitance	C <sub>rss</sub>			—	38	—

## ● Switching Parameters

PARAMETER	SYMBOL	Condition	UNIT	Min	Typ	Max
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =50V, I <sub>D</sub> =50A, R <sub>GEN</sub> =3Ω	nS	—	12.1	—
Turn-on Rise Time	t <sub>r</sub>		nS	—	17.4	—
Turn-off Delay Time	t <sub>D(off)</sub>		nS	—	47	—
Turn-off fall Time	t <sub>f</sub>		nS	—	32	—
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =50V, I <sub>D</sub> =50A V <sub>GS</sub> =10V	nC	—	45	—
Gate-Source Charge	Q <sub>gs</sub>		nC	—	10.3	—
Gate-Drain Charge	Q <sub>gd</sub>		nC	—	9.1	—

## ● Drian-Source Diode Characteristics

PARAMETER	SYMBOL	Condition	UNIT	Min	Typ	Max
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =100A, V <sub>GS</sub> =0V	V	—	—	1.2
Maximum Body-Diode Continuous Current	I <sub>S</sub>	—	A	—	—	100
Reverse Recovery time	t <sub>rr</sub>	I <sub>SD</sub> =100A di/dt=100A/us	nS	—	32	—
Reverse Recovery Charge	Q <sub>rr</sub>		nC	—	146	—

Note :

(1) Repetitive Rating: Pulse width limited by maximum junction temperature.

(2) EAS condition : T<sub>j</sub>=25°C ,V<sub>DD</sub>=50V,V<sub>G</sub>=10V,L=0.5mH,I<sub>AS</sub>=27A,R<sub>G</sub>=25Ω.

(3) Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

● Ratings And Characteristics Curves (Ta=25°C Unless otherwise specified)

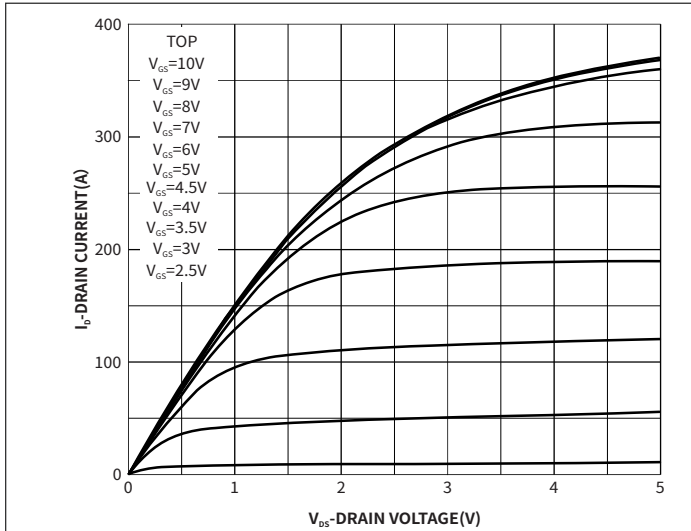


Fig.1 Output Characteristics

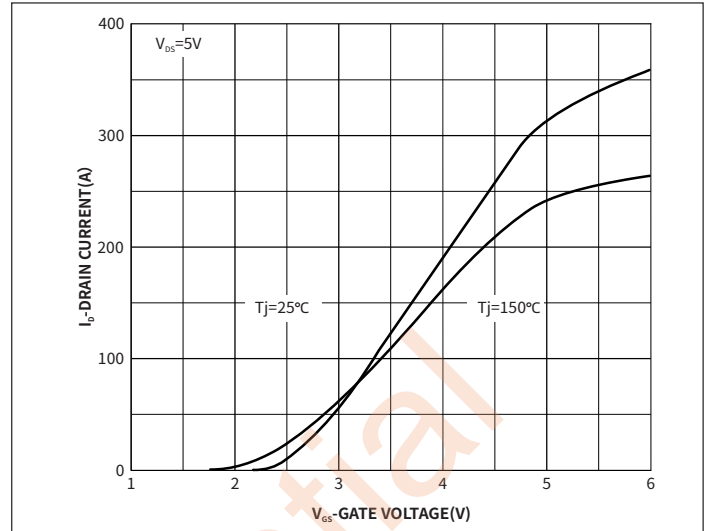


Fig.2 Transfer Characteristics

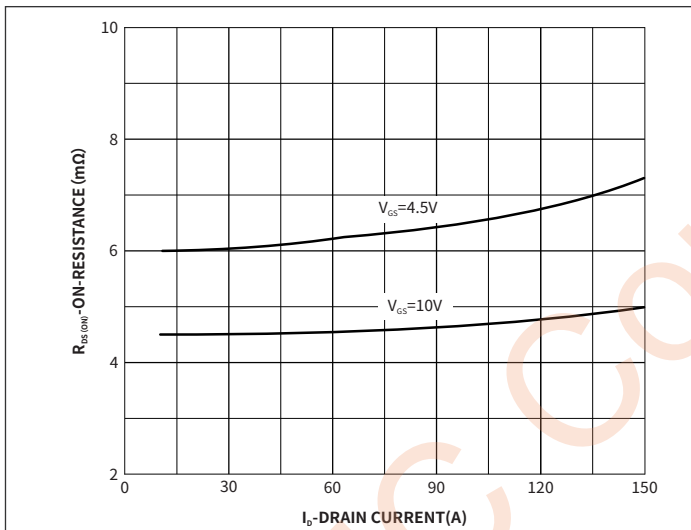


Fig.3 On-Resistance vs. Drain Current and Gate Voltage

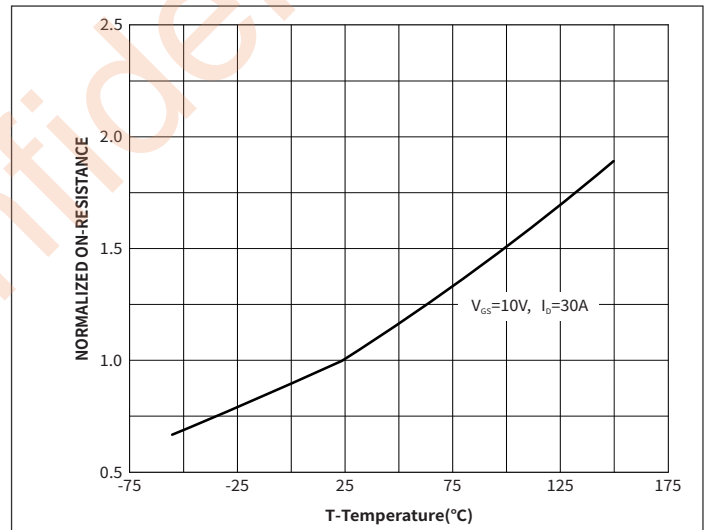


Fig.4 On-Resistance vs. Junction Temperature

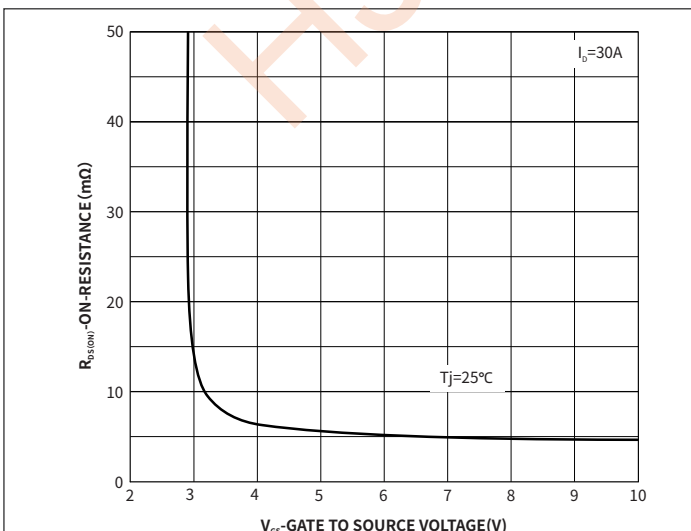


Fig.5 On-Resistance vs. Gate to Source Voltage

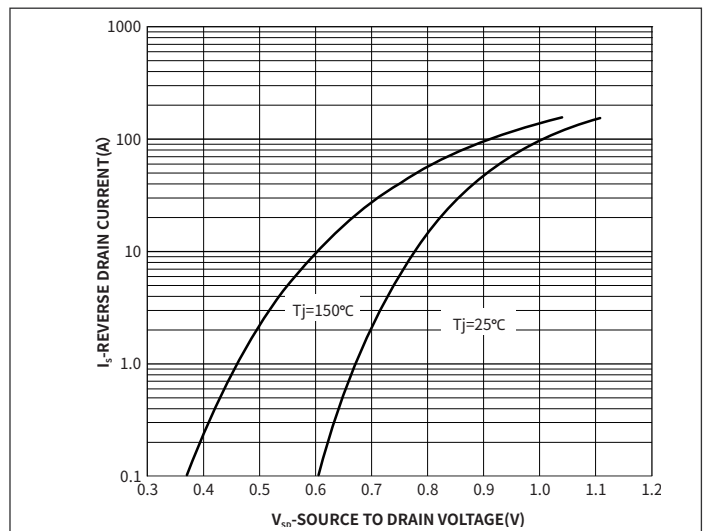
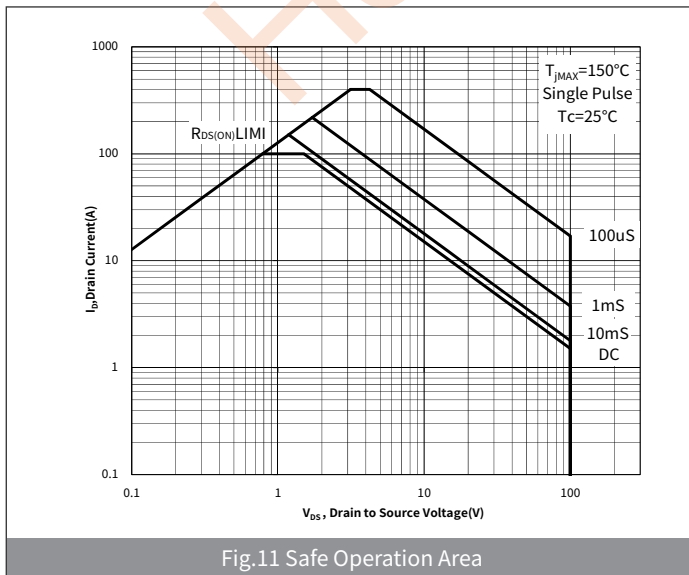
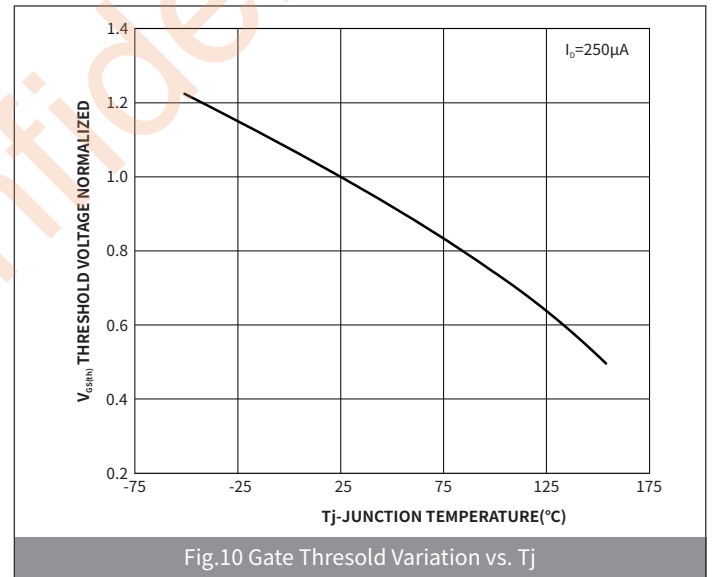
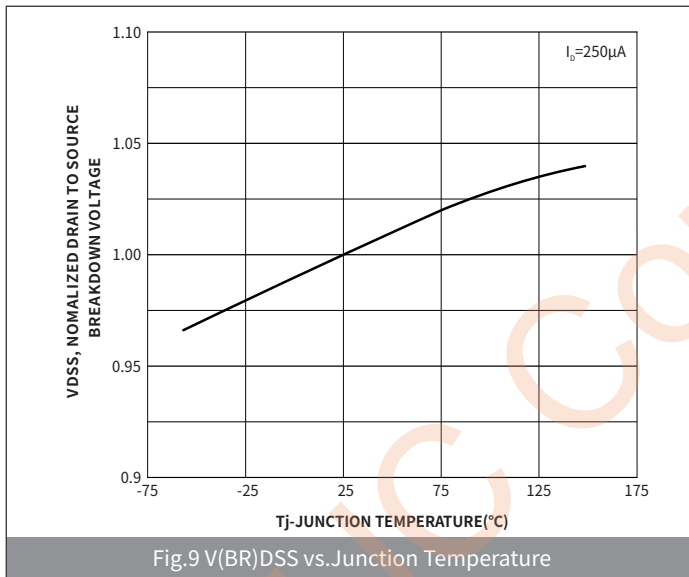
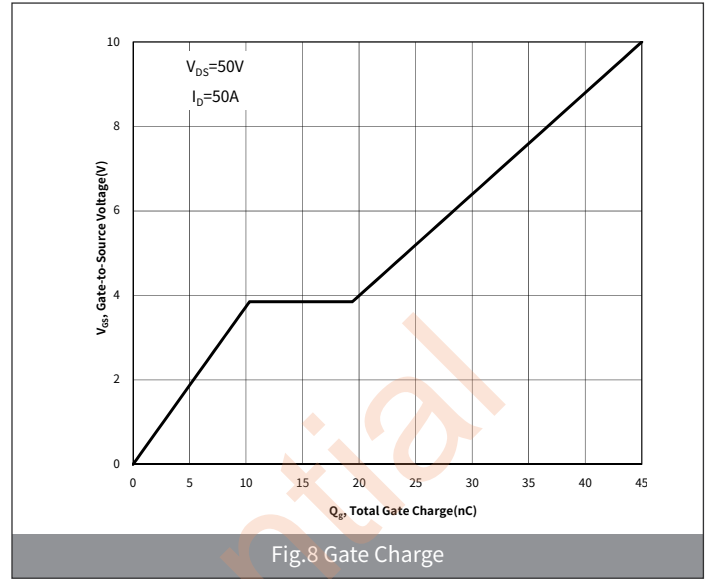
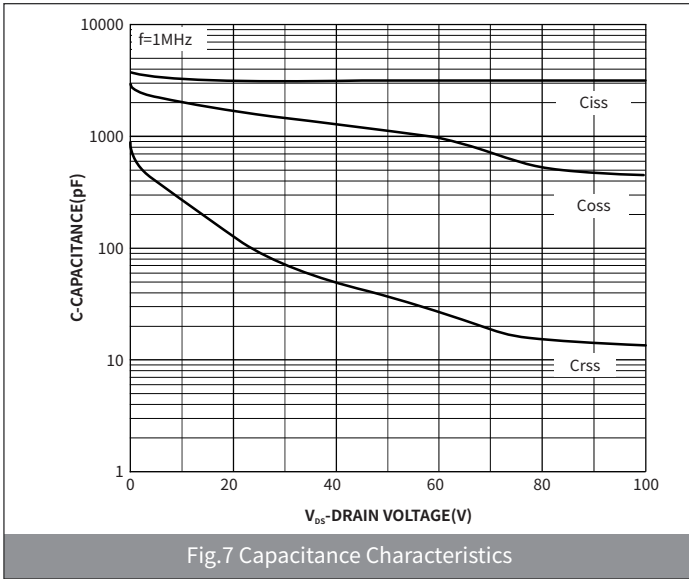
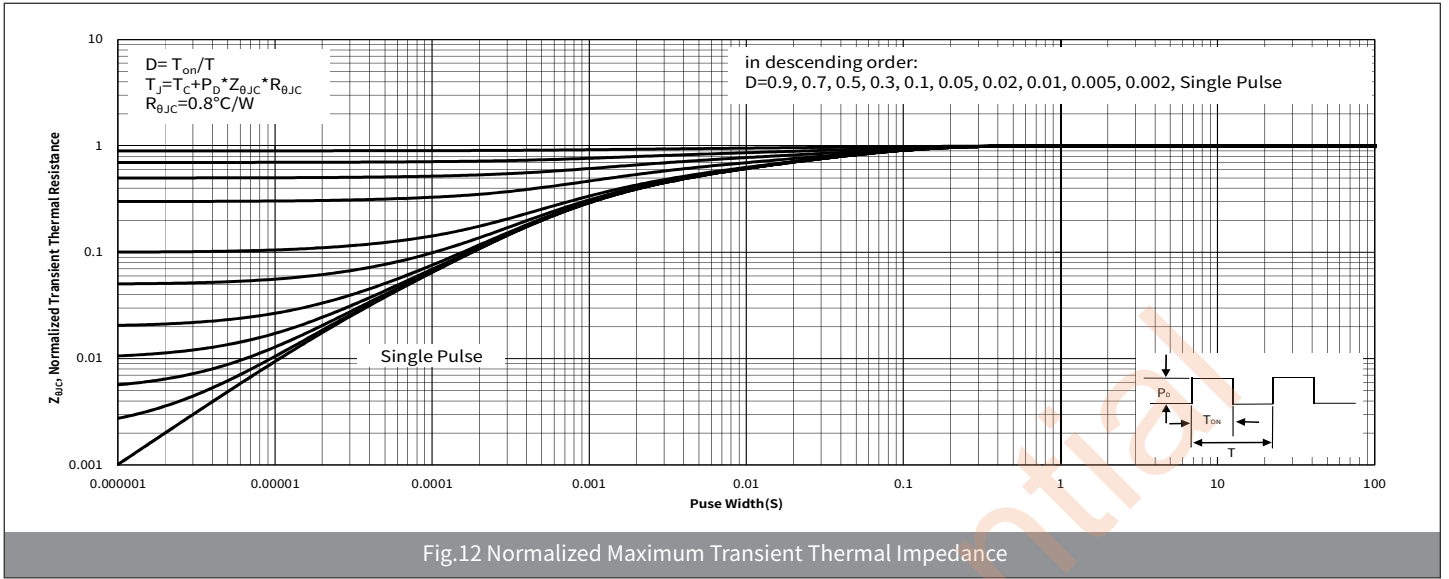


Fig.6 Typical Body-Diode Forward Characteristics

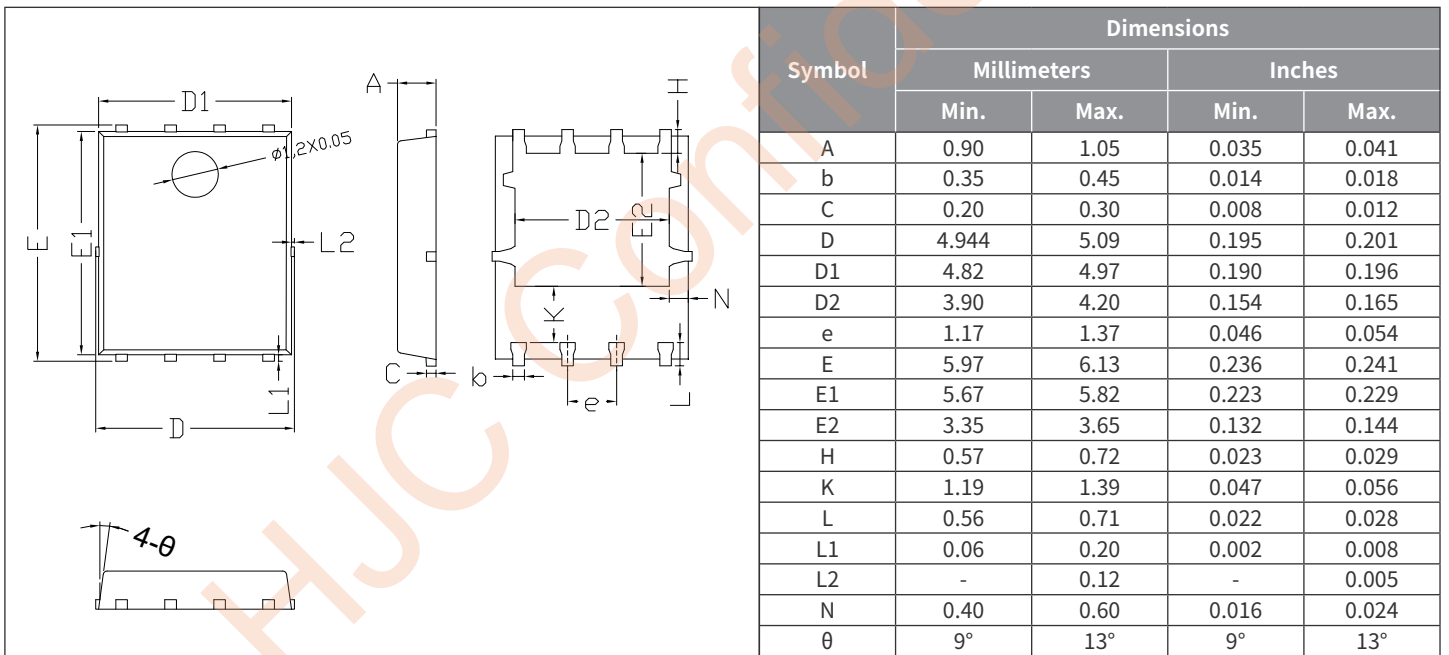
● Ratings And Characteristics Curves (Ta=25°C Unless otherwise specified)



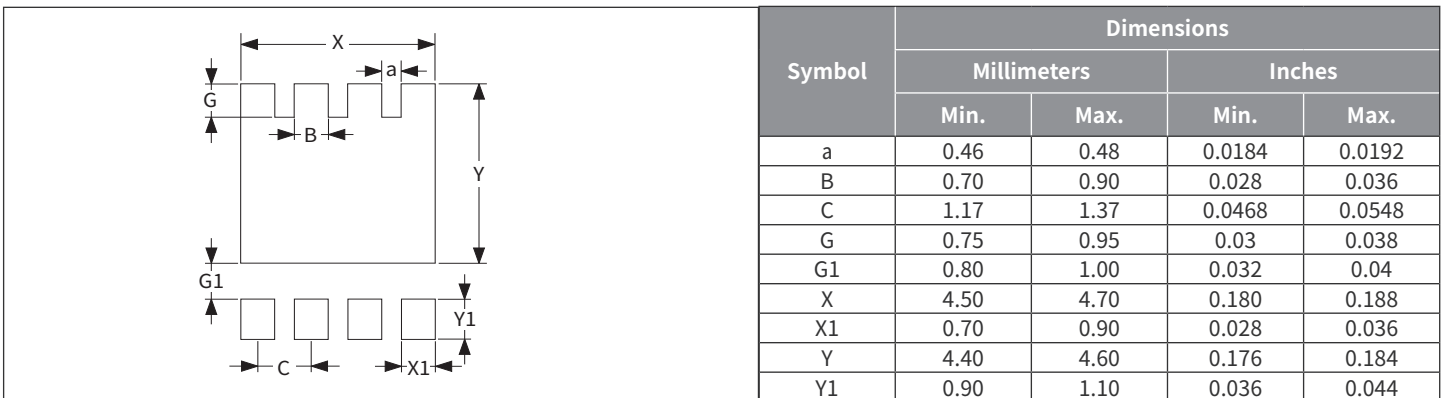
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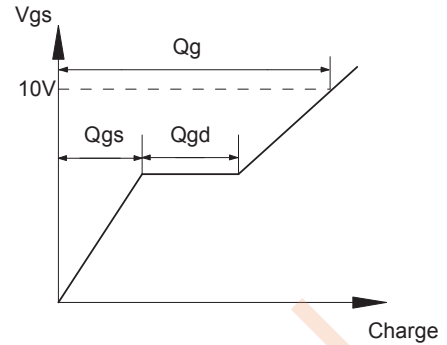
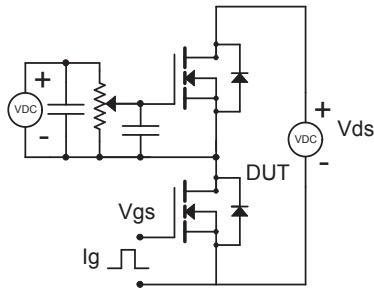
● Package Outline Dimensions (PDFN5060)



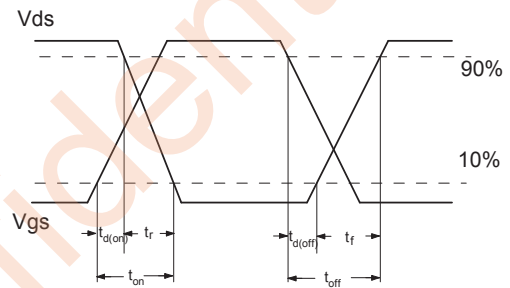
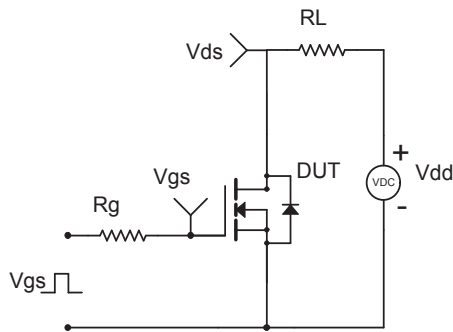
● Suggested Pad Layout



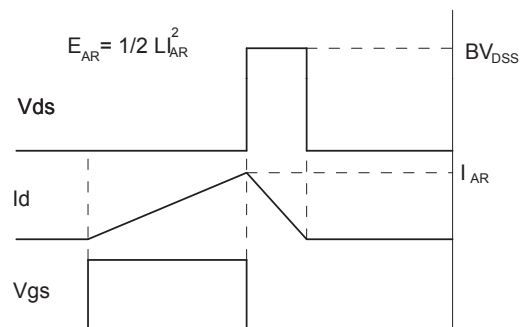
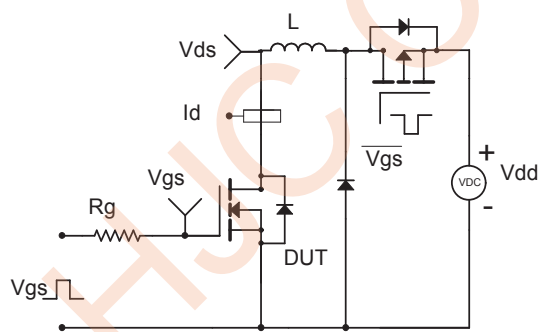
### 1. Gate Charge Test Circuit & Waveforms



### 2. Resistive Switching Test Circuit & Waveforms



### 3. Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



### 4. Diode Recovery Test Circuit & Waveforms

