

N-Channel 80V MOSFET

E080N020CL1

V_{DS} (V)	$R_{DS(on),max}$ (m Ω)	I_D (A)
80V	20 @ $V_{GS} = 10V$	35

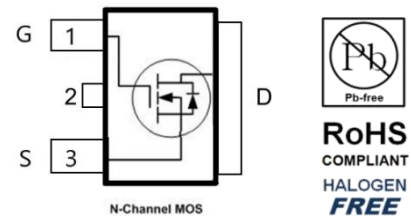
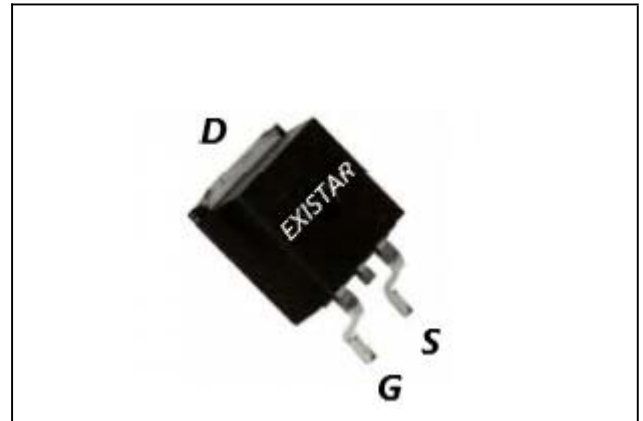
Features

- Low $R_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Applications

- DC/DC conversion
- Power switch
- PD charger
- Moto driver

TO-252



Package And Ordering Information

Ordering code	Package	Marking
E080N020CL1	TO-252	E080N020CL1

Ordering Information

Package	Units/ Reel	Reels/ Inner Box	Units/ Inner Box
TO-252	2500	1	2500

Key Performance Parameters

Parameter	Value	Unit
V _{DS} , min @ T _j (max)	80	V
I _D , pulse	140	A
R _{DS(ON)} , max @ V _{GS} =10V	20	mΩ
Q _g	13	nC

Absolute Maximum Ratings at T_j=25°C Unless Otherwise Noted

Parameter		Symbol	Limit	Unit
Drain-source voltage		V _{DS}	80	V
Gate-source voltage		V _{GS}	±20	
Continuous drain current	T _C =25°C	I _D	35	A
	T _C =100°C		-	
Pulsed drain current		I _{D,pulse}	140	
Avalanche energy, single pulse		E _{AS}	22	mJ
Power dissipation	T _C =25°C	P _D	35	W
	T _A =25°C		-	
Operating junction and storage temperature range		T _J , T _{stg}	-55 To 175	°C

Thermal Characteristics

Parameter		Symbol	Max.	Unit
Thermal resistance, junction-to-case	Steady state	R _{θJC}	4.3	°C/W
Thermal resistance, junction-to-ambient	Steady state	R _{θJA}	62	

Electrical Characteristics at T_j=25°C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Static						
Drain to source breakdown voltage	V _{(BR)DSS}	80			V	V _{GS} = 0, I _D = 250 μA
Gate-source threshold voltage	V _{GS(th)}	1.3	1.8	2.0	V	V _{DS} = V _{GS} , I _D = 250 μA
Gate-body leakage	I _{GSS}			±100	nA	V _{DS} = 0 V, V _{GS} = ±20 V
Zero gate voltage drain current	I _{DSS}			1	μA	V _{DS} = 80 V, V _{GS} = 0 V
Drain-source on-resistance	R _{DS(on)}		13.6	20	mΩ	V _{GS} = 10 V, I _D = 12 A
Drain-source on-resistance	R _{DS(on)}		19	25	mΩ	V _{GS} = 4.5 V, I _D = 9 A
Forward transconductance	g _{fs}		-		S	V _{DS} = 5 V, I _D = 30 A

Gate resistance	Rg		1.5		Ω	f=1MHz
Gate Charge						
Total gate charge	Qg		13		nC	VDS = 40 V, ID = 20 A, VGS = 10 V
Gate-source charge	Qgs		2.4			
Gate-drain charge	Qgd		2.5			
Dynamic						
Turn-on delay time	td(on)		7		ns	VDS = 40 V, ID =20 A, VGS = 10 V, RGEN = 2 Ω
Rise time	tr		4			
Turn-off delay time	td(off)		17			
Fall time	tf		2.6			
Input capacitance	Ciss		894		pF	VDS =25 V, VGS = 0 V, f = 100kHz
Output capacitance	Coss		337			
Reverse transfer capacitance	Crss		24			
Body Diode						
Diode forward voltage	VSD			1.3	V	VGS = 0 V, IS = 20 A
Reverse recovery time	trr		40		ns	VR= 40 V, IS =20 A, di/dt = 100 A/μs
Reverse recovery charge	Qrr		35		nC	

Electrical Characteristics Diagrams

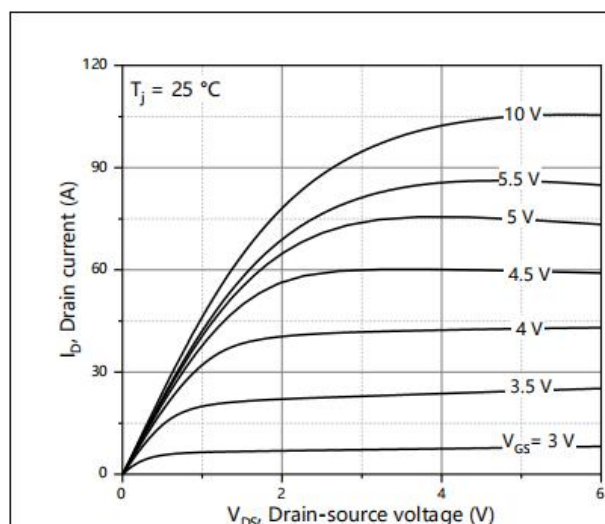


Figure 1. Typ. output characteristics

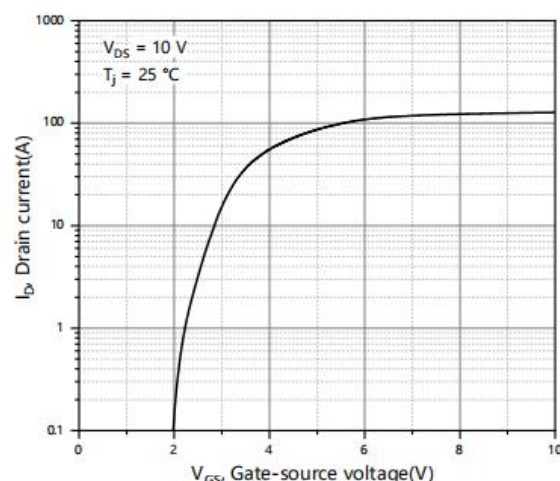


Figure 2. Typ. transfer characteristics

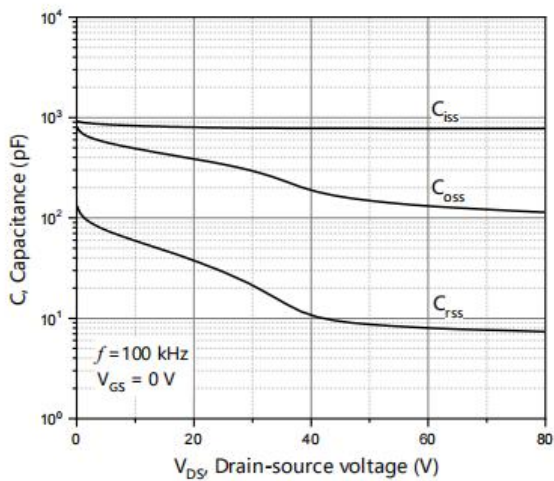


Figure 3. Typ. capacitances

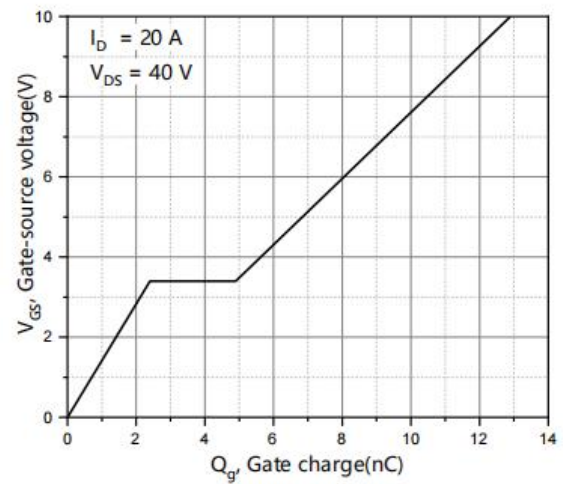


Figure 4. Typ. gate charge

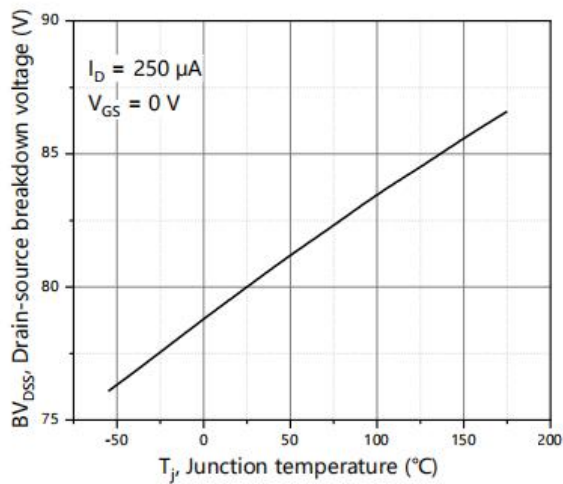


Figure 5. Drain-source breakdown voltage

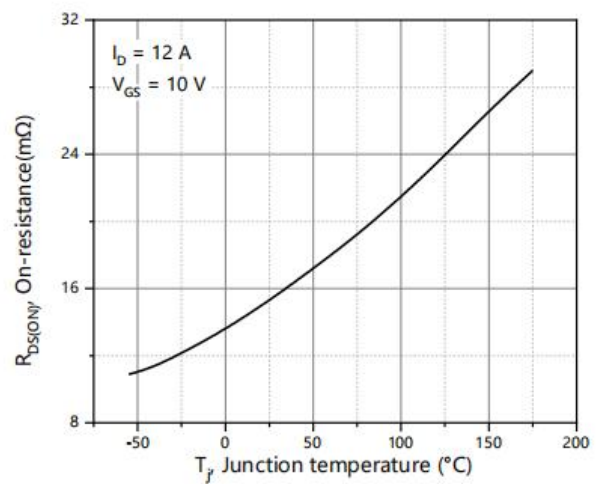


Figure 6. Drain-source on-state resistance

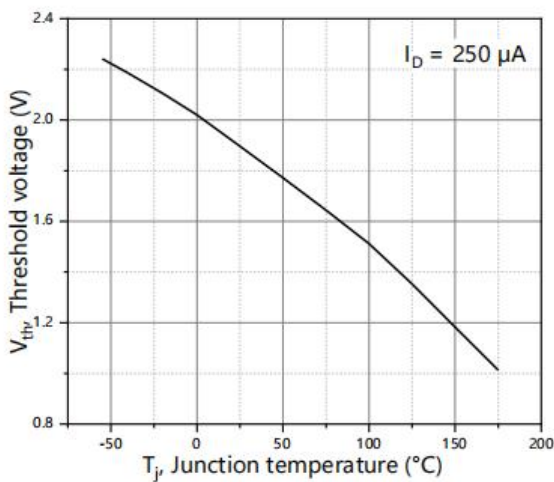


Figure 7. Threshold voltage

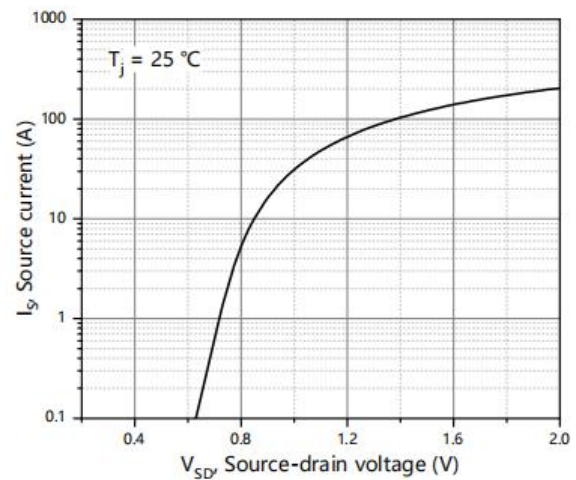


Figure 8. Forward characteristic of body diode

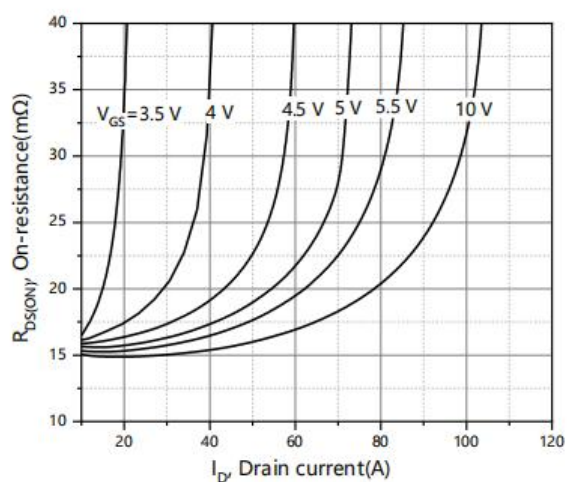


Figure 9. Drain-source on-state resistance

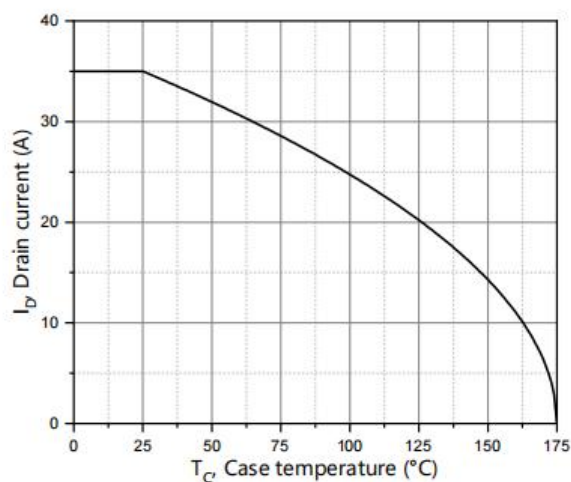


Figure 10. Drain current

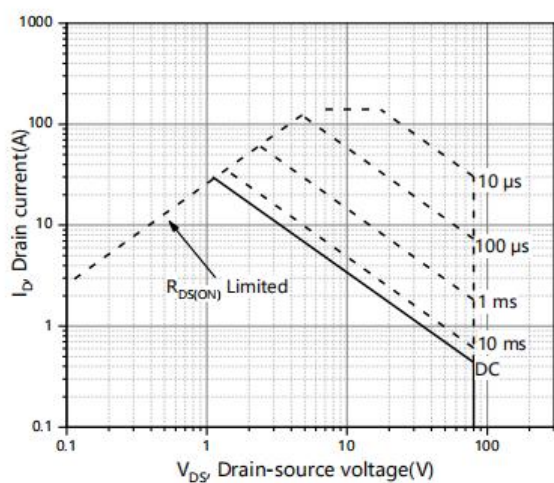


Figure 11. Safe operation area $T_C=25^{\circ}C$

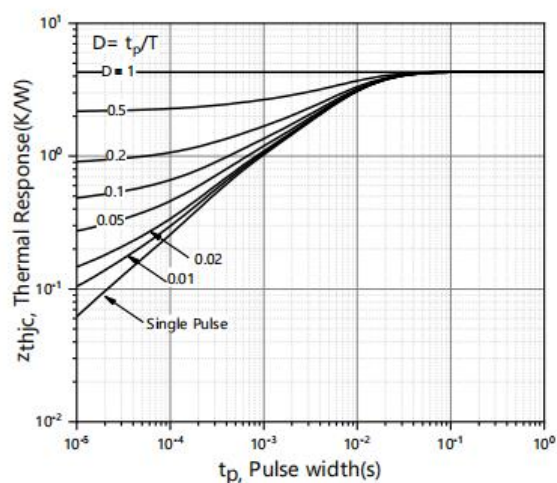


Figure 12. Max. transient thermal impedance

Test circuits and waveforms

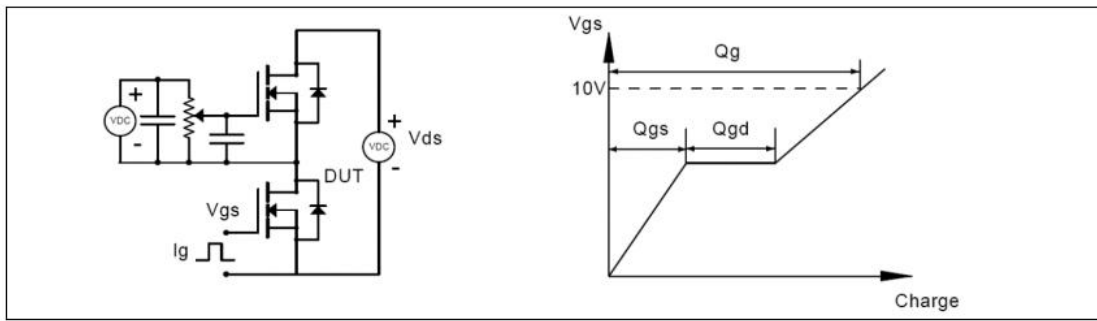


Figure 1. Gate charge test circuit & waveform

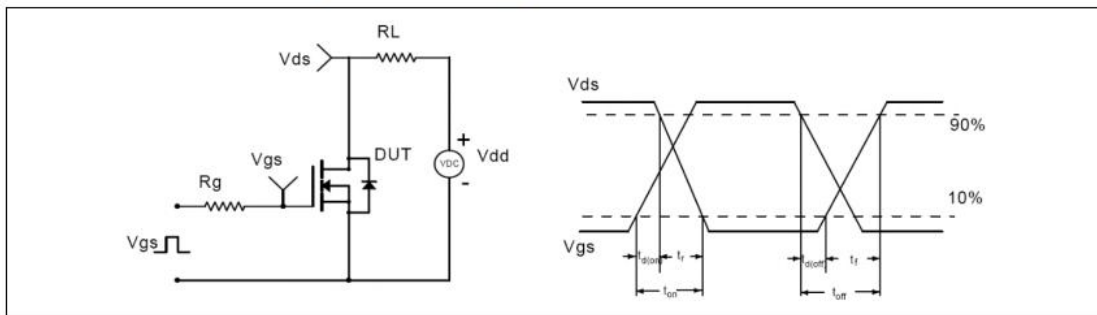


Figure 2. Switching time test circuit & waveforms

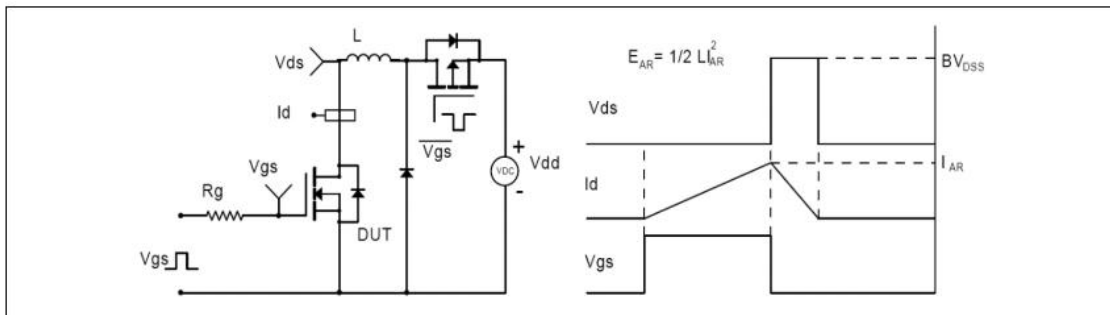


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

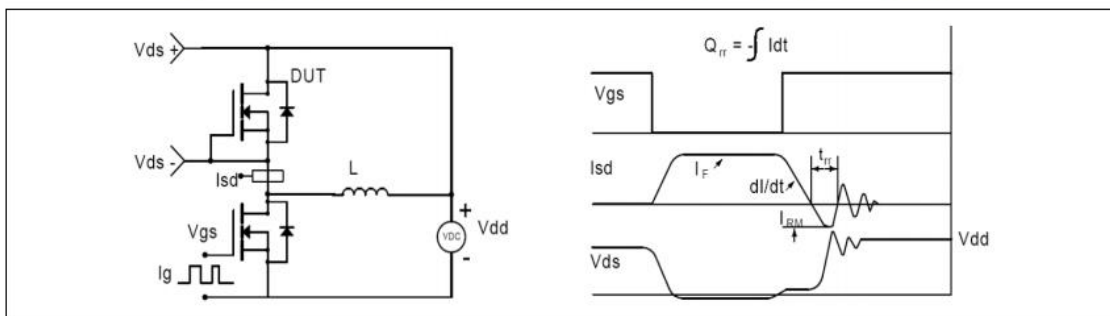
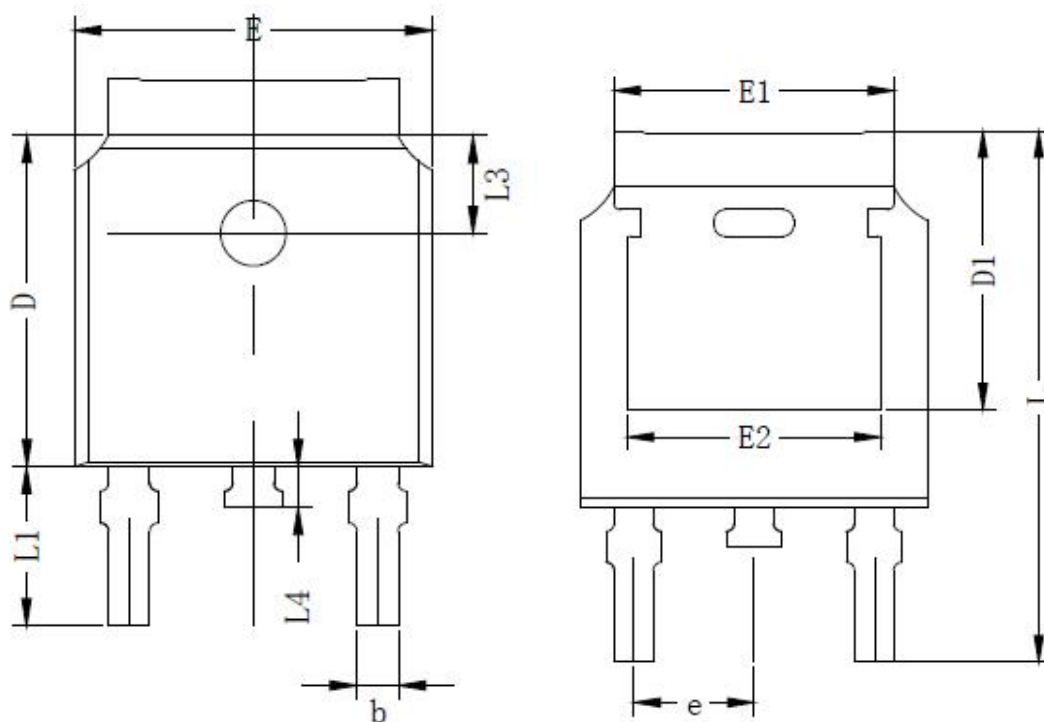


Figure 4. Diode reverse recovery test circuit & waveforms

Package Outline Dimensions



SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0.97	1.07	1.17
A2	0.00	—	0.12
b	0.66	0.76	0.86
c	0.45	0.51	0.60
D	5.90	6.10	6.30
D1	5.10	5.30	5.45
E	6.40	6.60	6.80
E1	5.10	5.33	5.45
E2	4.63	4.83	5.03
L	9.90	10.10	10.30
L1	2.74	2.94	3.14
L2	1.40	1.50	1.70
L3	1.65	1.80	1.95
L4	0.60	0.80	1.00
e	2.286BSC		
θ	5°	7°	10°
θ 1	0°	—	3°

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