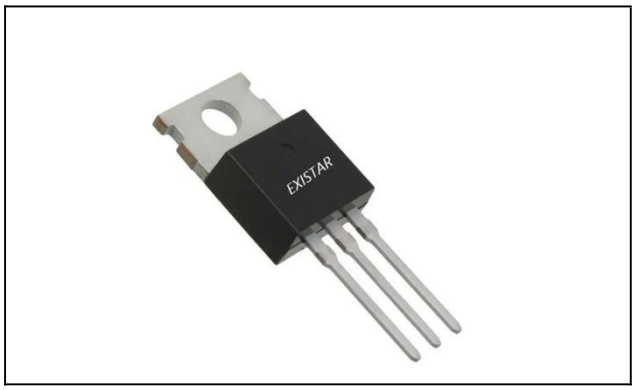
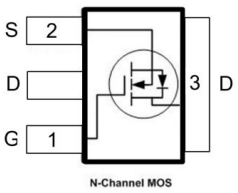
N-Channel 100V MOSFET

E100N4P5AH1

V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
100V	4.5 @ V_{GS} = 10V	170

TO-220





Pb-free
RoHS
COMPLIANT
HALOGEN
FREE

Features

- Low $R_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Applications

- DC/DC conversion
- Power switch
- PD charger
- Moto driver

Package And Ordering Information

Ordering code	Package	Marking
E100N4P5AH1	TO-220	E100N4P5AH1

Ordering Information

Package	Units/ Tube	Tubes/ Inner Box	Units/ Inner Box
TO-220	50	20	1000

Key Performance Parameters

Parameter	Value	Unit
VDS, min @ Tj(max)	100	V
ID, pulse	675	A
RDS(ON), max @ VGS=10V	4.5	mΩ
Qg	91	nC

Absolute Maximum Ratings at Tj=25°C Unless Otherwise Noted

Parameter		Symbol	Limit	Unit
Drain-source voltage		V_{DS}	100	V
Gate-source voltage		V_{GS}	±20	
Continuous drain current	T_C=25°C	I_D	170	A
	T_C=100°C		120	
Pulsed drain current		$I_{D,pulse}$	675	
Avalanche energy, single pulse		E_{AS}	484	mJ
Power dissipation	T_C=25°C	P_D	250	W
	T_A=25°C		-	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to 175	℃

Thermal Characteristics

Parameter		Symbol	Max.	Unit
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	0.6	°C/W
Thermal resistance, junction-to-ambient	Steady state	$R_{\theta JA}$	60	

Electrical Characteristics at Tj=25°C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Static						
Drain to source breakdown voltage	$V_{(BR)DSS}$	100			V	V_{GS} = 0, I_D = 250 μA
Gate-source threshold voltage	$V_{GS(th)}$	2.2	2.7	3.2	V	V_{DS} = V_{GS}, I_D = 250 μA
Gate-body leakage	I_{GSS}			±100	nA	V_{DS} = 0 V, V_{GS} = ±20 V
Zero gate voltage drain current	I_{DSS}			1	μA	V_{DS} = 100 V, V_{GS} = 0 V
Drain-source on-resistance	$R_{DS(on)}$		3.6	4.5	mΩ	V_{GS} = 10 V, I_D = 40 A
Forward transconductance	gfs		-		S	V_{DS} = 5 V, I_D = 30 A
Gate resistance	Rg		1.8		Ω	f=1MHz

Gate Charge						
Total gate charge	Qg		91		nC	V_{DS} = 50 V, I_D = 40 A, V_{GS} = 10 V
Gate-source charge	Qgs		25			
Gate-drain charge	Qgd		25			
Dynamic						
Turn-on delay time	$t_{d(on)}$		21		ns	V_{DS} = 50 V, I_D =40 A, V_{GS} = 10 V, R_{GEN} = 3 Ω
Rise time	t_r		69			
Turn-off delay time	$t_{d(off)}$		57			
Fall time	t_f		70			
Input capacitance	C_{iss}		5440		pF	V_{DS} =50 V, V_{GS} = 0 V, f = 1MHz
Output capacitance	C_{oss}		1035			
Reverse transfer capacitance	C_{rss}		35			
Body Diode						
Diode forward voltage	V_{SD}		0.8	1.2	V	V_{GS} = 0 V, I_F = 40 A
Reverse recovery time	t_{rr}		59		ns	V_{GS}= 0 V, I_S =40 A, di/dt = 100 A/μs
Reverse recovery charge	Q_{rr}		71		nC	

Electrical Characteristics Diagrams

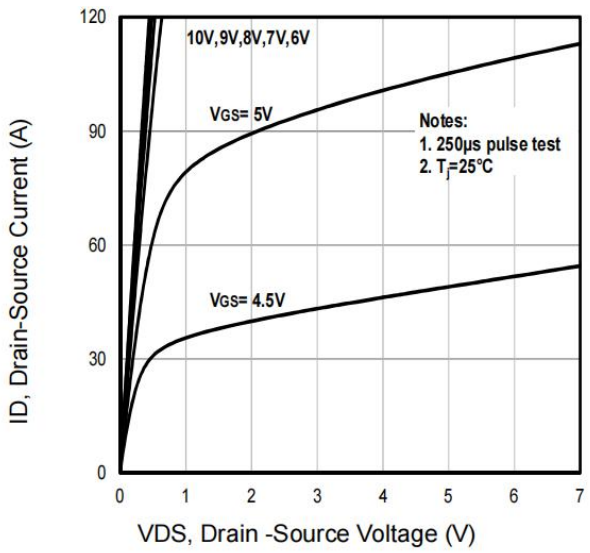


Fig1. Typical Output Characteristics

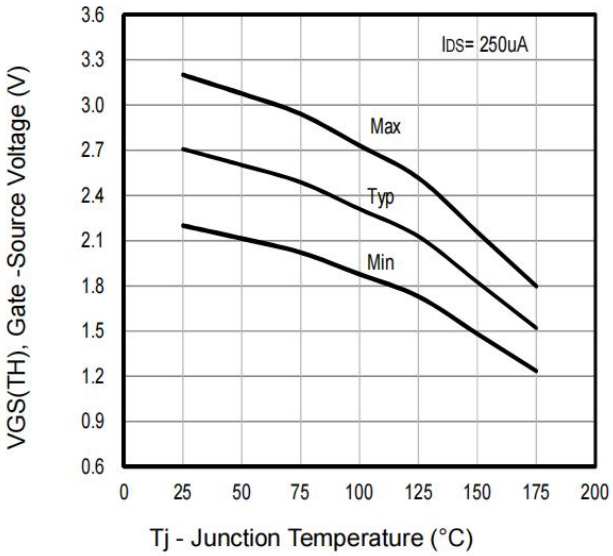


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

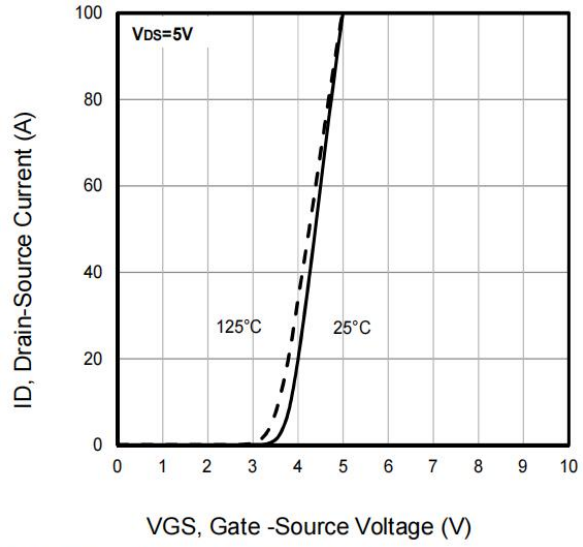


Fig3. Typical Transfer Characteristics

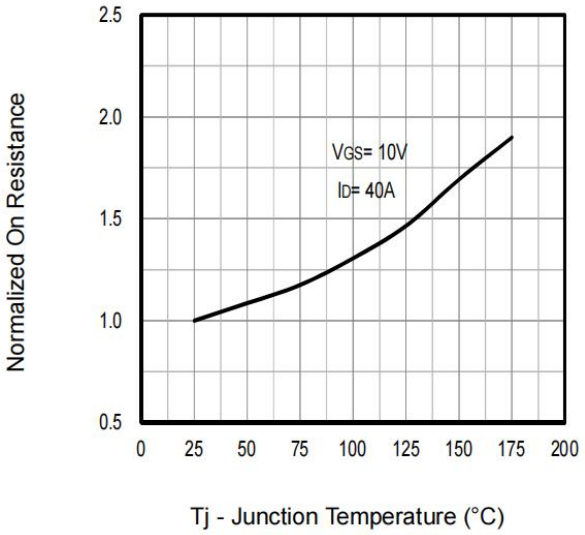


Fig4. Typical Normalized On-Resistance Vs. Tj

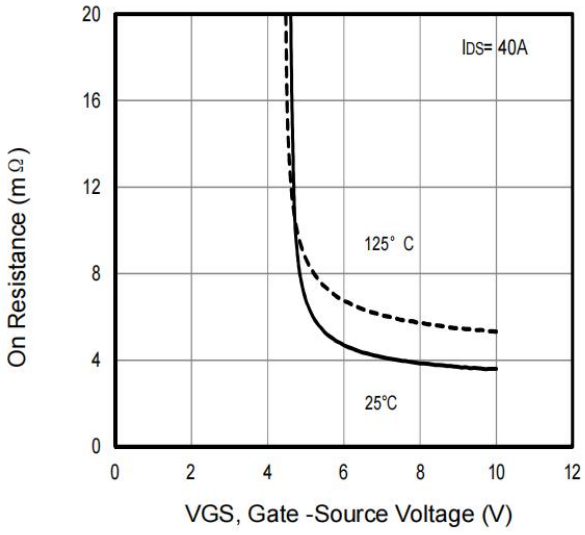


Fig5. Typical On Resistance Vs Gate -Source Voltage

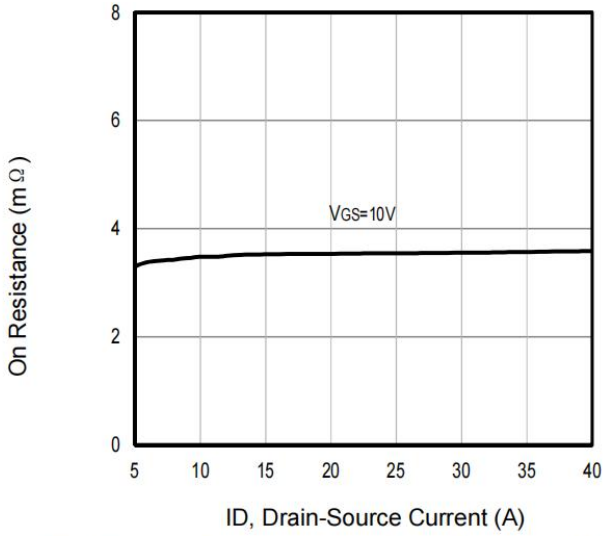


Fig6. Typical On Resistance Vs Drain Current and Gate

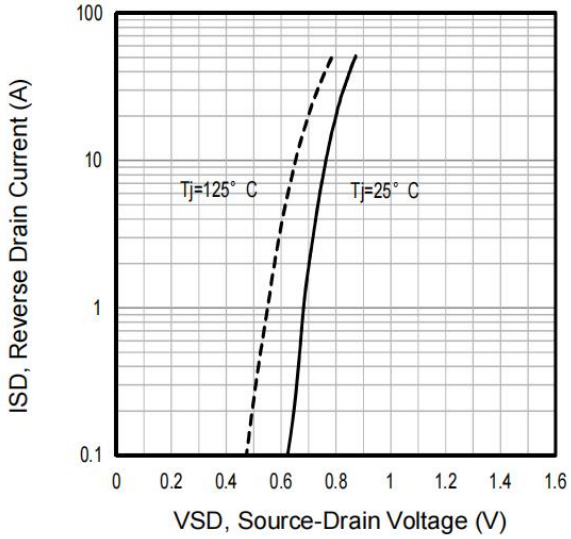


Fig7. Typical Source-Drain Diode Forward Voltage

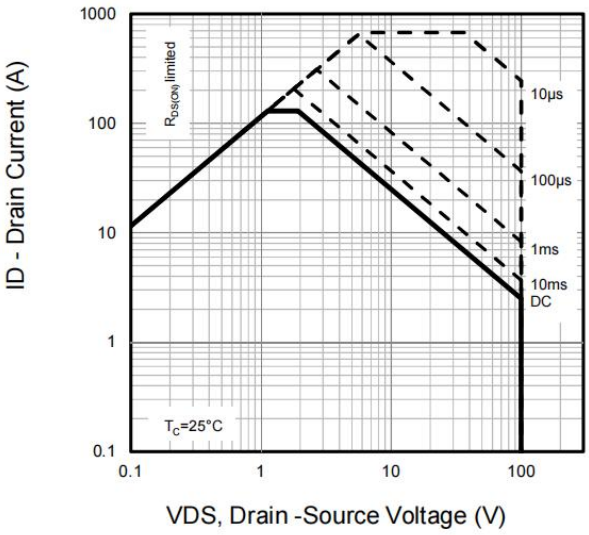


Fig8. Maximum Safe Operating Area

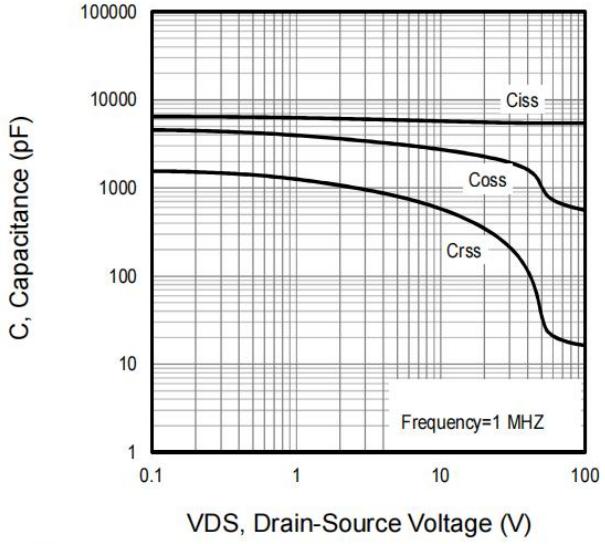


Fig9. Typical Capacitance Vs. Drain-Source Voltage

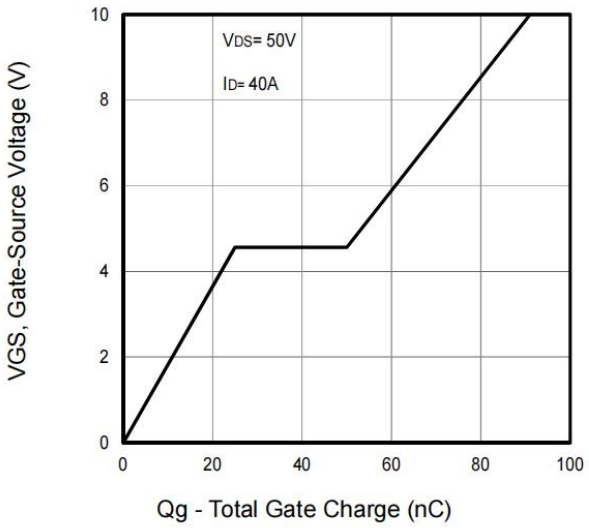


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

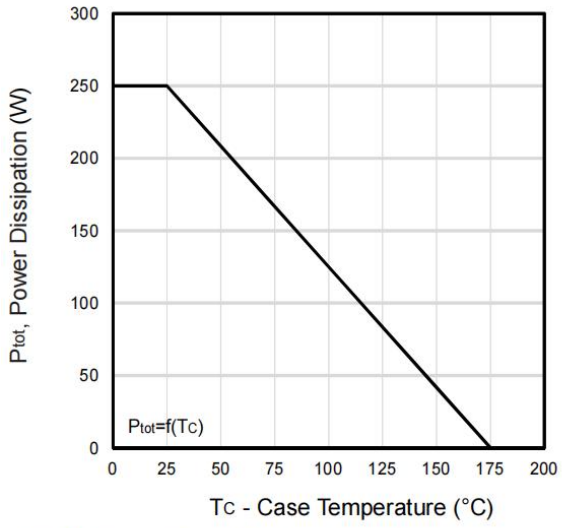


Fig11. Power Dissipation Vs. Case Temperature

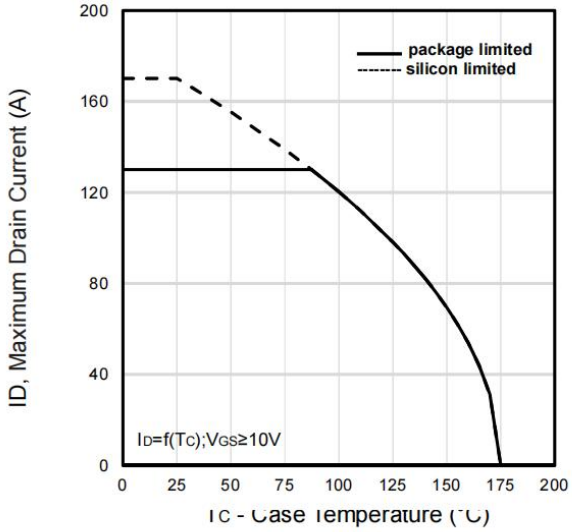


Fig12. Maximum Drain Current Vs. Case Temperature

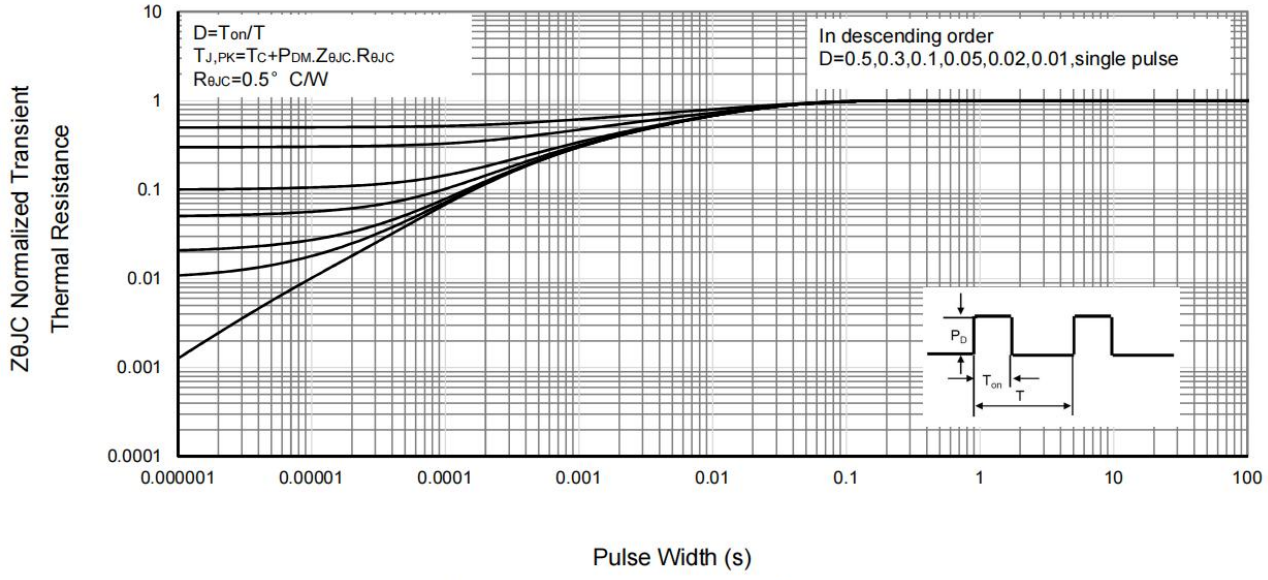


Fig13 . Normalized Maximum Transient Thermal Impedance

Test circuits and waveforms

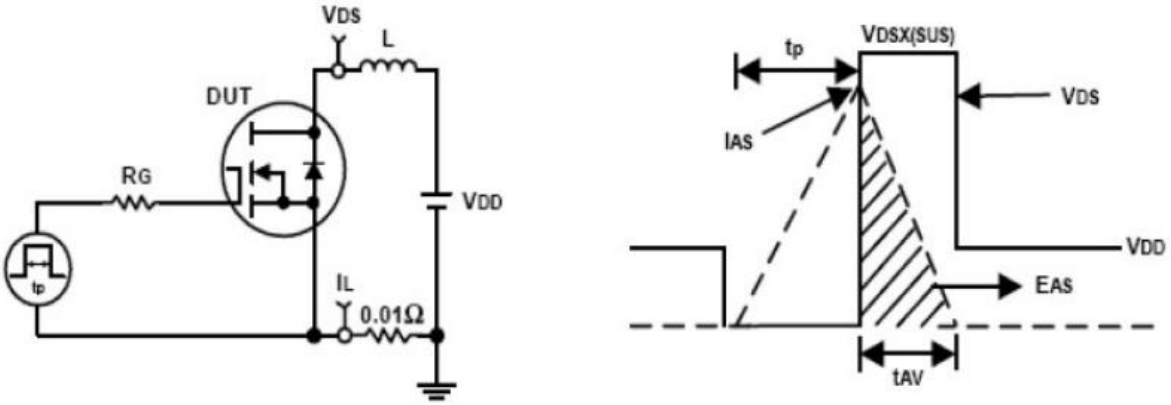


Fig14. Unclamped Inductive Test Circuit and waveforms

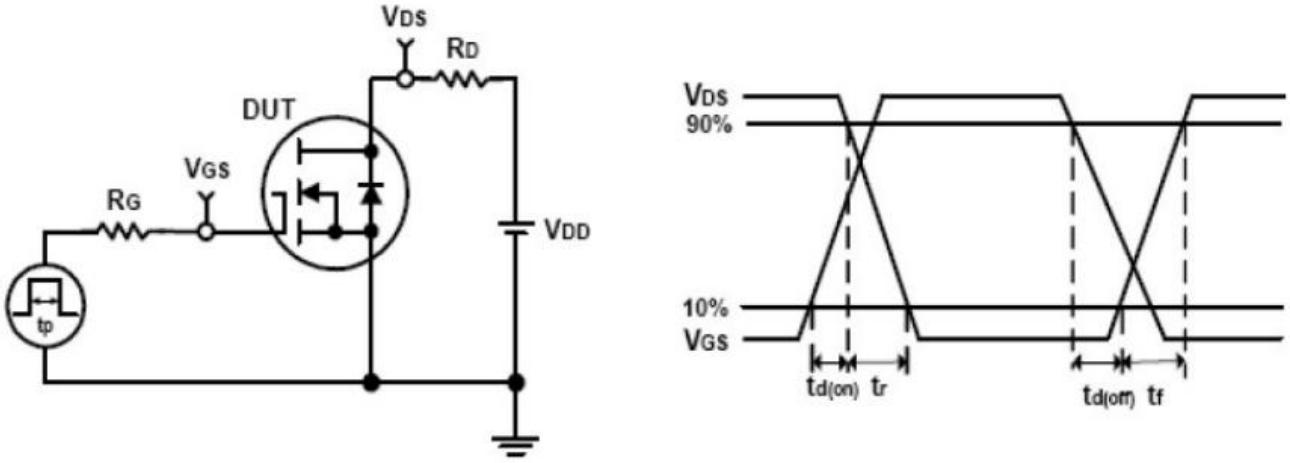
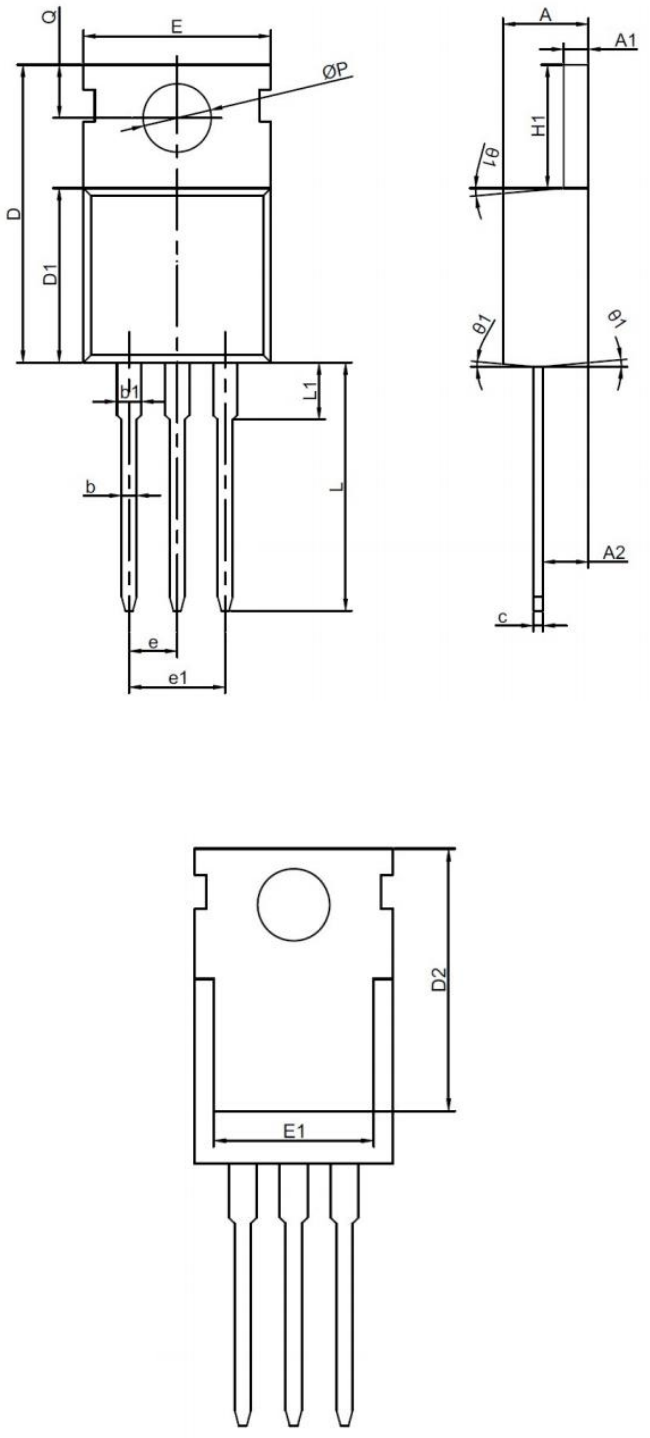


Fig15. Switching Time Test Circuit and waveforms

Package Outline Dimensions



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.30	4.52	4.70
A1	1.15	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	1.00
b1	1.15	1.32	1.50
c	0.45	0.50	0.65
D	15.10	15.70	16.10
D1	8.80	9.20	9.40
D2	12.80	-	13.70
E	9.65	9.90	10.30
E1	7.00	-	8.2
e	2.54 BSC		
e1	5.08 BSC		
H1	6.20	6.50	6.90
L	12.70	-	13.90
L1	-	-	3.50
ΦP	3.40	3.60	3.80
Q	2.60	2.80	3.00
θ1	1 °	3 °	7 °

Legal Disclaimer

The information given in this document shall be for illustrative purposes only and shall in no event be regarded as a guarantee of conditions or characteristics. Existar Technologies reserves the right to change any information herein. With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Existar Technologies or its affiliates hereby make no representation or warranty of any kind, expressed or implied, as to any information provided hereunder, including without limitation as to the accuracy, completeness or non-infringement of intellectual property rights of any third party, and they assume no liability for the consequences of use of such information. In addition, any information given in this document is subject to customer's compliance with its obligations stated herein and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Existar Technologies in customer's applications. The information contained herein is exclusively intended for technically trained staff. No license is granted by implication under any patent right, copyright, mask work right, or other intellectual property right. It is customer's sole responsibility to evaluate the suitability of the product for the intended application and the completeness of the product information given herein with respect to such application. In no event shall Existar Technologies or its affiliates be liable to any party for any direct, indirect, special, punitive, incidental or consequential damages of any nature whatsoever, including but not limited to loss of profits and loss of goodwill, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory.