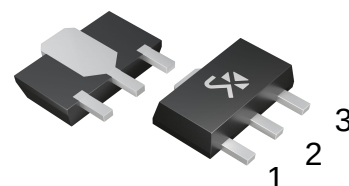


PNP Silicon Epitaxial Planar Transistor

Features

- World standard micro packaging.
- Low VCE (sat): VCE (sat)=-0.2V at 1A

SOT-89



1base 2collector 3emitter

MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Symbol	Parameter	Value	Units
V _{CBO}	Collector-Base Voltage	-60	V
V _{CEO}	Collector-Emitter Voltage	-50	V
V _{EBO}	Emitter-Base Voltage	-6	V
I _C	Collector Current -Continuous	-1.0	A
I _C	Collector Current -Continuous (Pulse) *	-2.0	A
P _C	Collector Power Dissipation	2	W
T _j	Junction Temperature	150	°C
T _{stg}	Storage Temperature	-55-150	°C

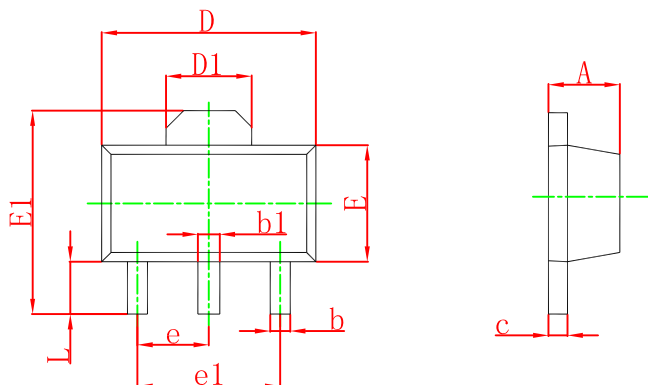
ELECTRICAL CHARACTERISTICS (T_{amb}=25°C unless otherwise specified)

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Base emitter voltage*	V _{BE}	V _{CE} =-2V, I _C =-10mA	-600		-700	mV
Collector cut-off current	I _{CBO}	V _{CB} =-60V, I _E =0			-100	nA
Collector cut-off current	I _{EBO}	V _{EB} =-6V, I _C =0			-100	uA
DC current gain	h _{FE}	V _{CE} =-2V, I _C =-100mA V _{CE} =-2V, I _C =-1A	135 100	340 200	600	
Collector-emitter saturation voltage	V _{CE} (sat)	I _C =-1A, I _B =-50mA		-0.2	-0.3	V
Base saturation voltage*	V _{BE} (sat)	I _C =-1A, I _B =-50mA		-0.9	-1.2	V
Transition frequency	f _T	V _{CE} =-2 V, I _E =100mA,	80	120		MHz
output capacitance	C _{Ob}	V _{CE} =-10 V, I _E =0 mA, f=1.0MHz		25		pF

h_{FE} Classification

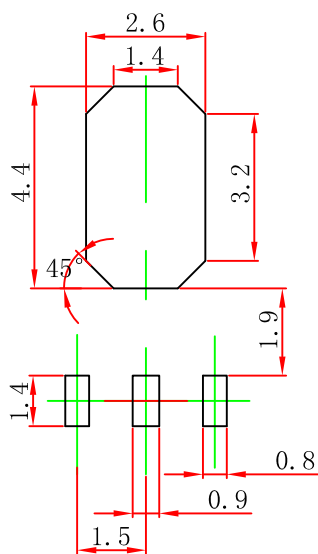
Marking	YM	YL	YK
h _{FE}	135-270	200-400	300-600

SOT-89 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF.		0.061 REF.	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP.		0.060 TYP.	
e1	3.000 TYP.		0.118 TYP.	
L	0.900	1.200	0.035	0.047

SOT-89 Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.