

# MSKSEMI 美森科

SEMICONDUCTOR



ESD



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PLED

## SI7336ADP-T1-E3-MS

Product specification

## Description

The SI7336ADP-T1-E3-MS uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application

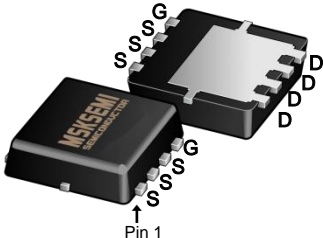
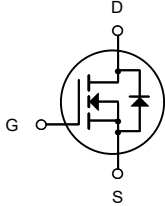

## Features

- $V_{DS} = 30V$   $I_D = 150A$
- $R_{DS(ON)} < 2.4m\Omega$   $V_{GS} = 10V$

## Application

- Battery protection
- Load switch
- Uninterruptible power supply

## Reference News

DFN5X6-8L	N-Channel MOSFET	Marking
		

## Absolute Maximum Ratings ( $T_c = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_c = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ <sup>1</sup>	150	A
$I_D @ T_c = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ <sup>1</sup>	80	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	160	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	180	mJ
$I_{AS}$	Avalanche Current	60	A
$P_D @ T_c = 25^\circ C$	Total Power Dissipation <sup>4</sup>	187	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	1.1	$^\circ C/W$

**Electrical Characteristics** ( $T_J=25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V$ , $I_D=250\mu A$	30	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	$BV_{DSS}$ Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=1mA$	---	0.014	---	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V$ , $I_D=30A$	---	2	2.4	m $\Omega$
		$V_{GS}=4.5V$ , $I_D=15A$	---	2.5	3.2	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$ , $I_D=250\mu A$	1.2	---	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4	---	mV/ $^\circ\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=24V$ , $V_{GS}=0V$ , $T_J=25^\circ\text{C}$	---	---	1	$\mu A$
		$V_{DS}=24V$ , $V_{GS}=0V$ , $T_J=55^\circ\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V$ , $V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=5V$ , $I_D=30A$	---	50	---	S
$R_g$	Gate Resistance	$V_{DS}=0V$ , $V_{GS}=0V$ , $f=1MHz$	---	1.7	---	$\Omega$
$Q_g$	Total Gate Charge (4.5V)	$V_{DS}=15V$ , $V_{GS}=10V$ , $I_D=15A$	---	56.9	---	nC
$Q_{gs}$	Gate-Source Charge		---	13.8	---	
$Q_{gd}$	Gate-Drain Charge		---	23.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V$ , $V_{GS}=10V$ , $R_G=3.3\Omega$ , $I_D=1A$	---	20.1	---	ns
$T_r$	Rise Time		---	6.3	---	
$T_{d(off)}$	Turn-Off Delay Time		---	124.6	---	
$T_f$	Fall Time		---	15.8	---	
$C_{iss}$	Input Capacitance	$V_{DS}=15V$ , $V_{GS}=0V$ , $f=1MHz$	---	4345	---	pF
$C_{oss}$	Output Capacitance		---	340	---	
$C_{rss}$	Reverse Transfer Capacitance		---	225	---	

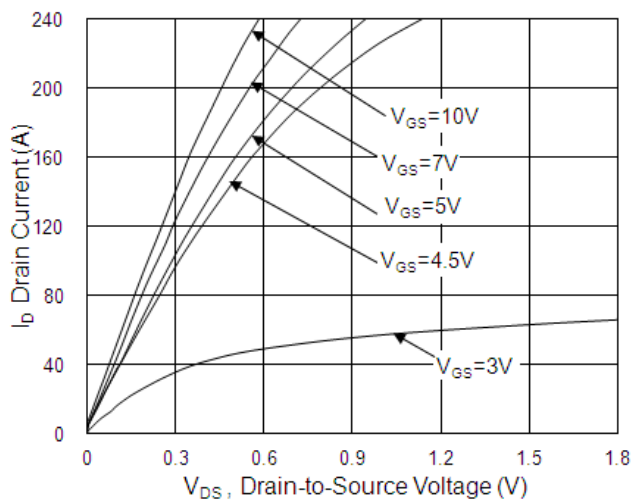
**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,6</sup>	$V_G=V_D=0V$ , Force Current	---	---	150	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V$ , $I_S=1A$ , $T_J=25^\circ\text{C}$	---	---	1.2	V

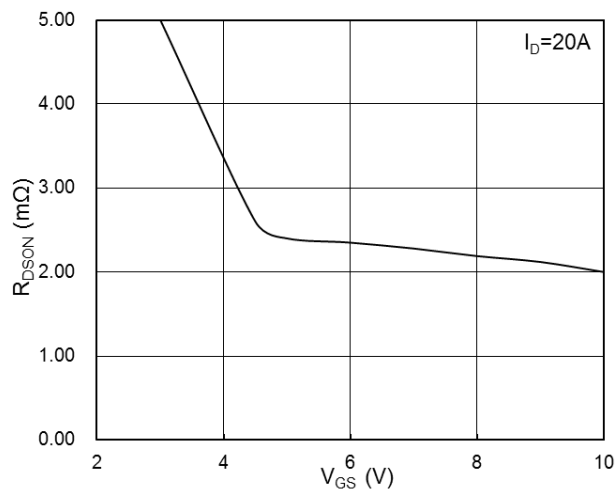
Note :

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper.
2. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is  $V_{DD}=25V$ ,  $V_{GS}=10V$ ,  $L=0.1mH$ ,  $I_{AS}=60A$
4. The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
5. The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.
6. Package limitation current is 85A.

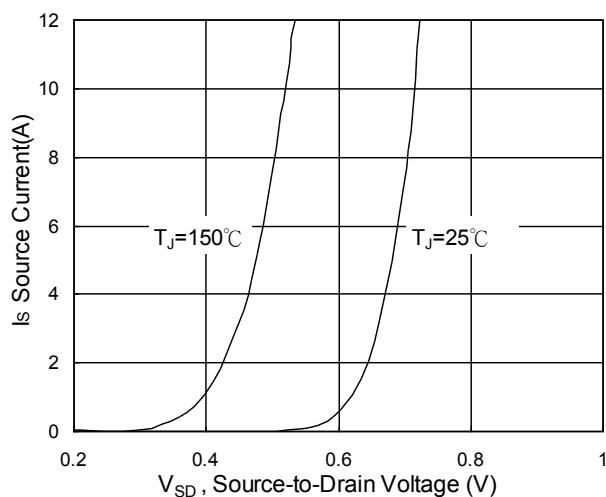
## Typical Characteristics



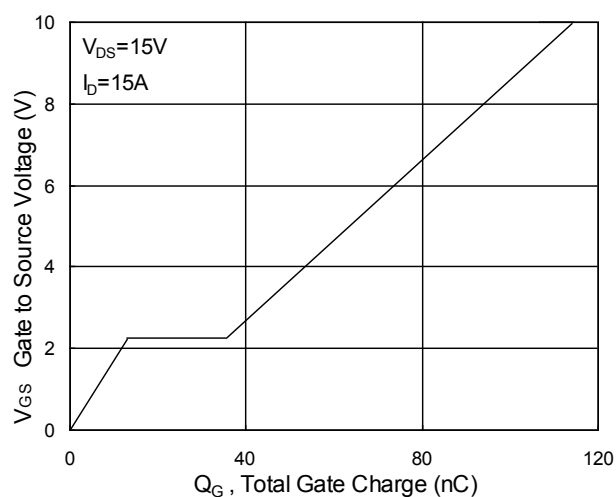
**Fig.1 Typical Output Characteristics**



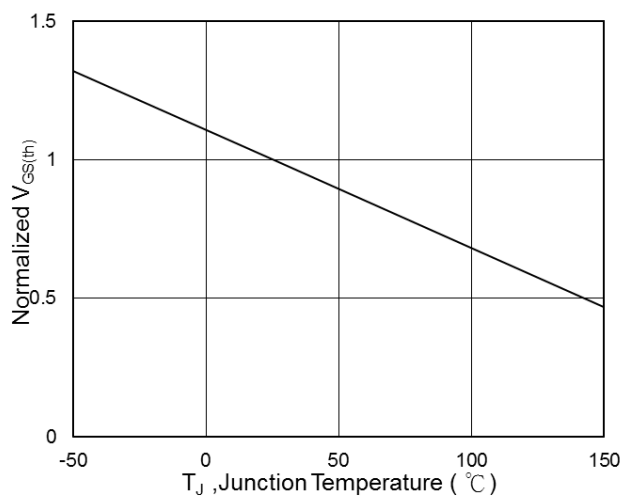
**Fig.2 On-Resistance v.s Gate-Source**



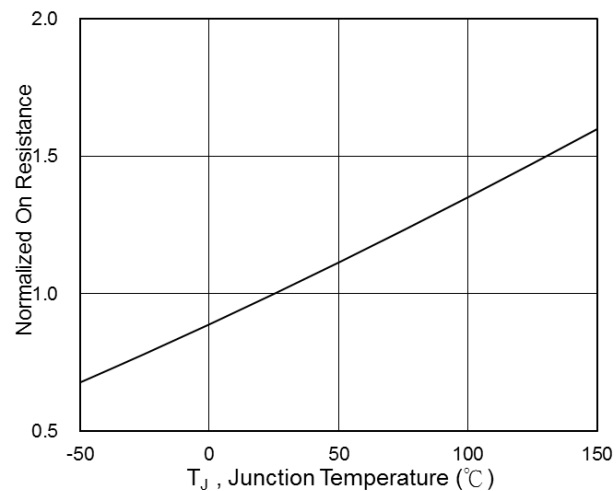
**Fig.3 Forward Characteristics of Reverse**



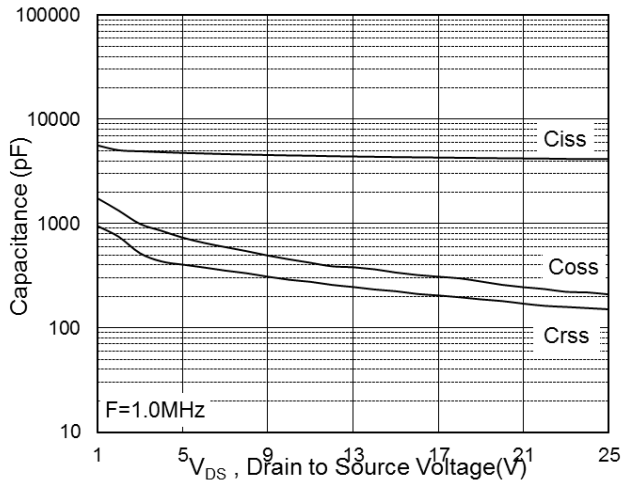
**Fig.4 Gate-Charge Characteristics**



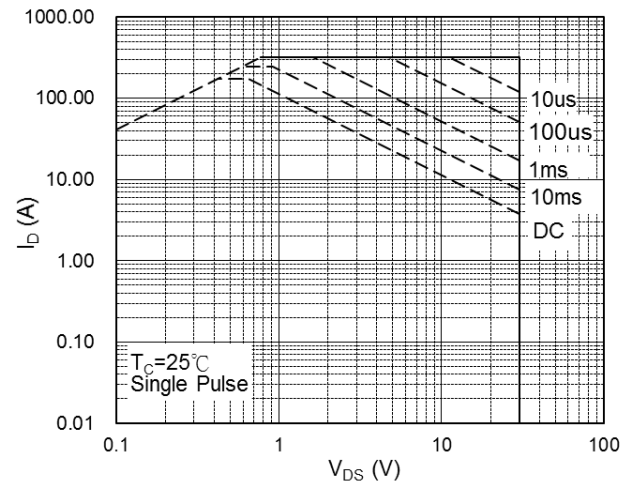
**Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$**



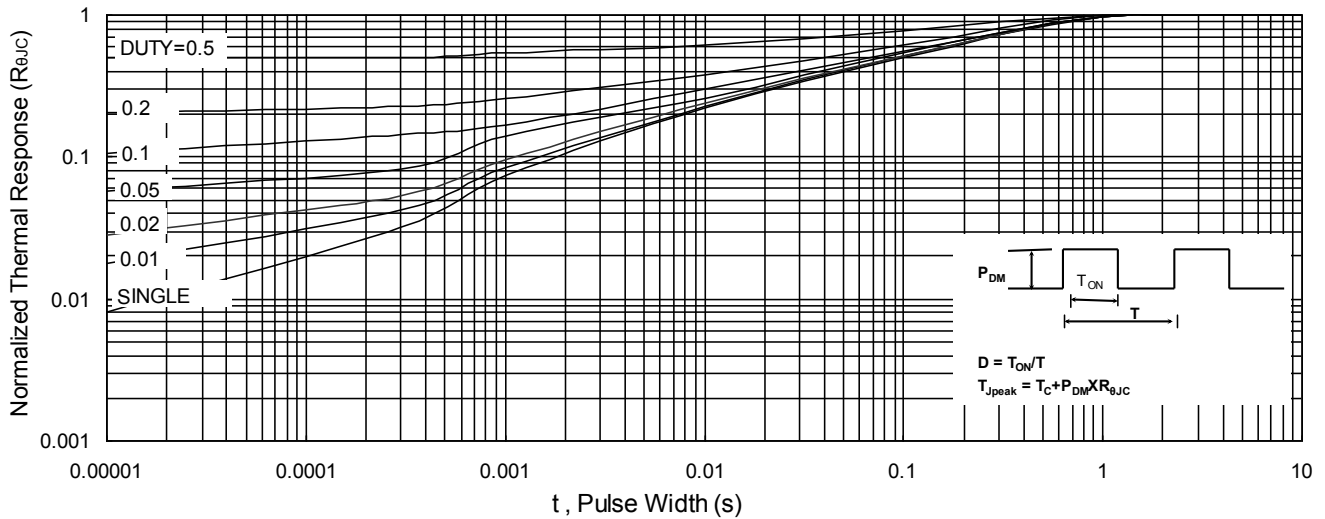
**Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$**



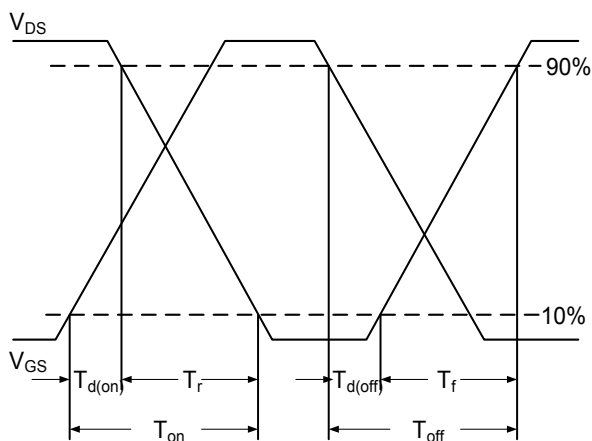
**Fig.7 Capacitance**



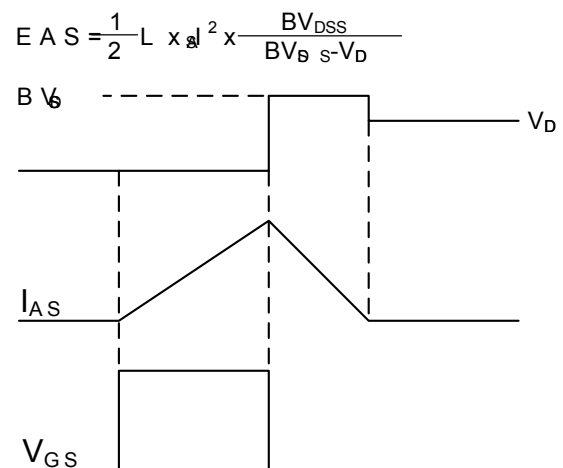
**Fig.8 Safe Operating Area**



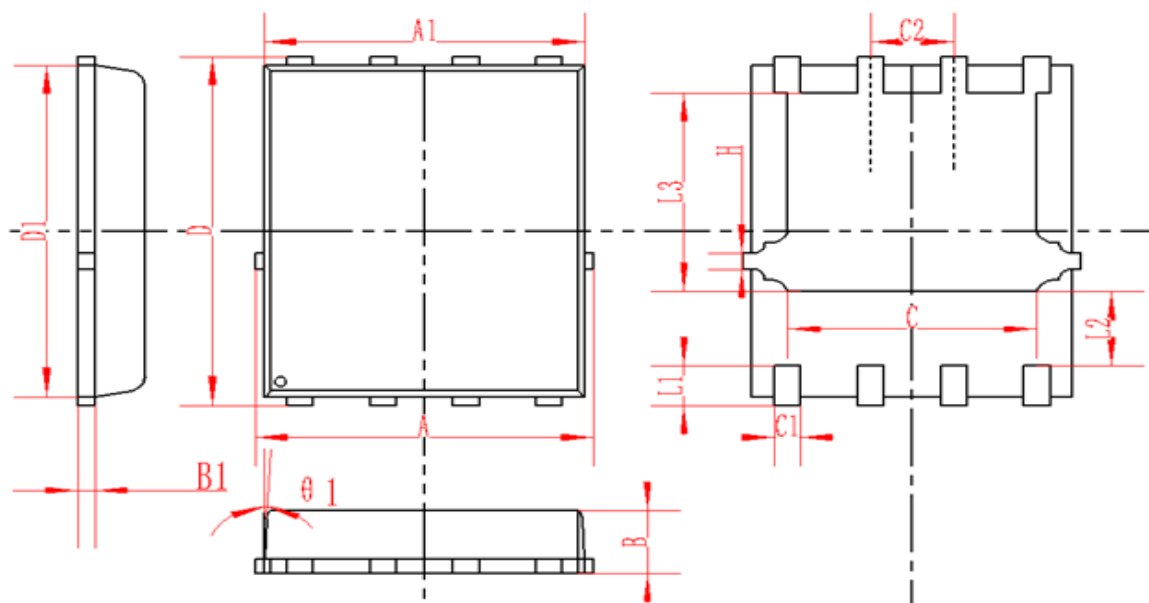
**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**

**DFN5X6-8L Package Information**


SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
B	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
θ1	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010

**REEL SPECIFICATION**

P/N	PKG	QTY
SI7336ADP-T1-E3-MS	DFN5X6-8L	5000

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