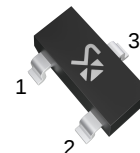


PNP Silicon Epitaxial Planar Transistor

SOT-23



1. BASE
2. EMITTER
3. COLLECTOR

MARKING:2L

MAXIMUM RATINGS ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	-160	V
V_{CEO}	Collector-Emitter Voltage	-150	V
V_{EBO}	Emitter-Base Voltage	-5	V
I_C	Collector Current -Continuous	-600	mA
P_C	Collector Power Dissipation	300	mW
T_j	Junction Temperature	150	$^{\circ}\text{C}$
T_{stg}	Storage Temperature	-55-+150	$^{\circ}\text{C}$
$R_{\theta JA}$	Thermal Resistance from Junction to Ambient Air	417	$^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_{amb}=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Collector-base breakdown voltage	$V_{(BR)CBO}$	$I_C=-100\mu\text{A}, I_E=0$	-160			V
Collector-emitter breakdown voltage	$V_{(BR)CEO}$	$I_C=-1\text{mA}, I_B=0$	-150			V
Emitter-base breakdown voltage	$V_{(BR)EBO}$	$I_E=-100\mu\text{A}, I_C=0$	-5			V
Collector cut-off current	I_{CBO}	$V_{CB}=-35\text{V}, I_E=0$			-0.1	μA
Emitter cut-off current	I_{EBO}	$V_{EB}=-6\text{V}, I_C=0$			-0.1	μA
DC current gain	h_{FE}	$V_{CE}=-5\text{V}, I_C=-1\text{mA}$ $V_{CE}=-5\text{V}, I_C=-10\text{mA}$ $V_{CE}=-5\text{V}, I_C=-50\text{mA}$	50 60 50		240	
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C=-10\text{mA}, I_B=-1\text{mA}$ $I_C=-50\text{mA}, I_B=-5\text{mA}$			-0.2 -0.5	V
Collector-emitter saturation voltage	$V_{BE(sat)}$	$I_C=-10\text{mA}, I_B=-1\text{mA}$ $I_C=-50\text{mA}, I_B=-5\text{mA}$			-1 -1	V
Output capacitance	C_{ob}	$V_{CB}=-10\text{V}, I_E=0, f=1\text{MHz}$			6	pF
Transition frequency	f_T	$V_{CE}=-10\text{V}, I_C=-10\text{mA}$ $f=100\text{MHz}$	100		300	MHz
Noise Figure	NF	$V_{CE}=5\text{V}, I_C=0.2\text{mA}, R_s=10\Omega, f=1\text{KHz}$			8	dB

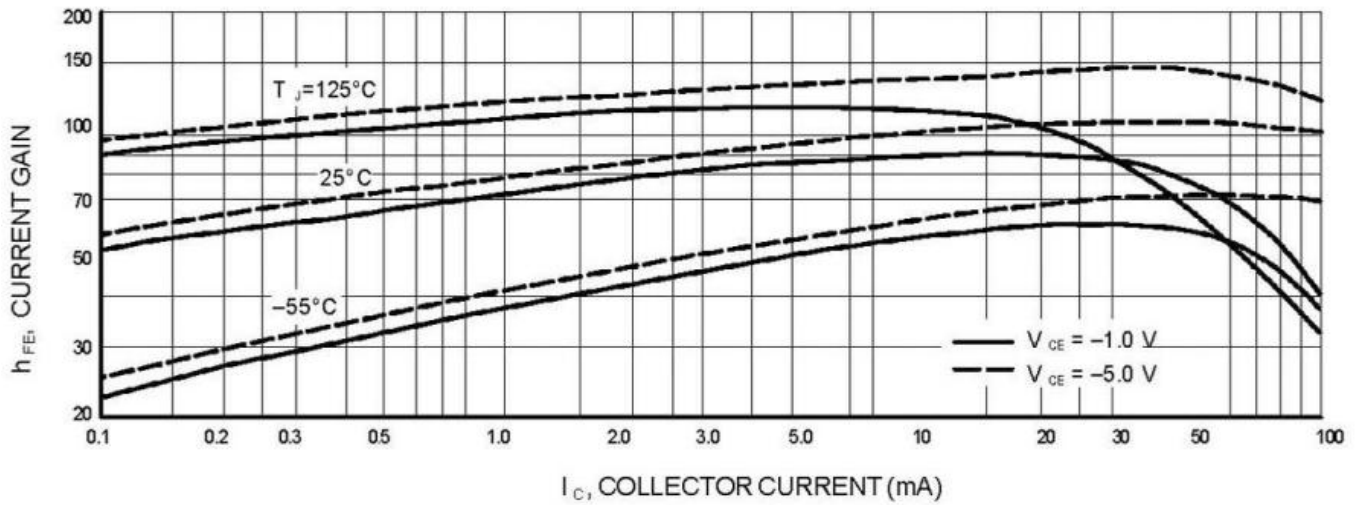


Figure 1. DC Current Gain

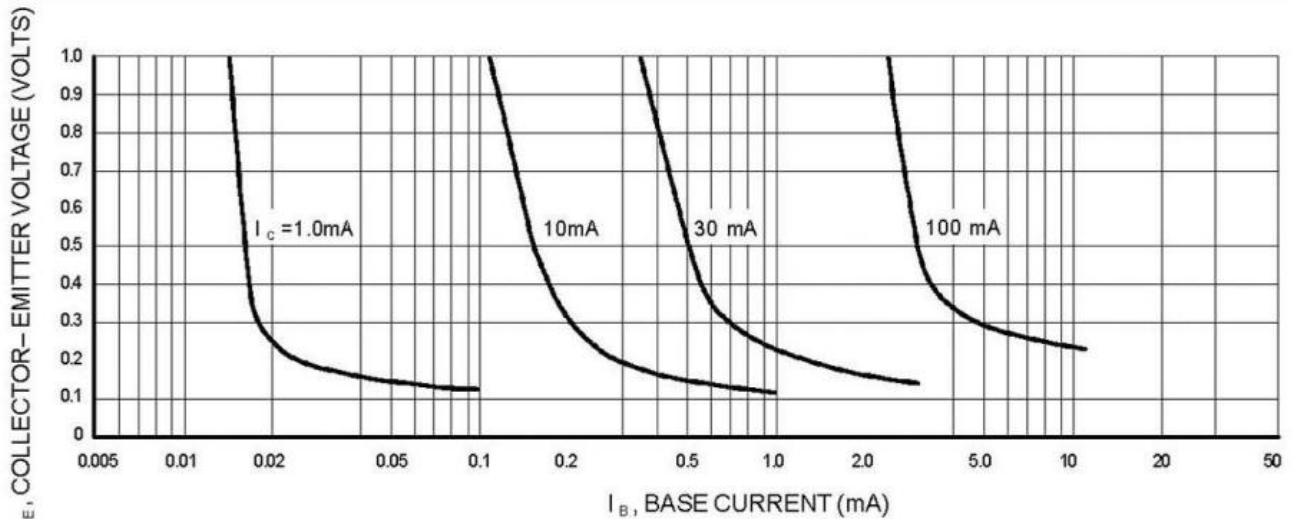


Figure 2. Collector Saturation Region

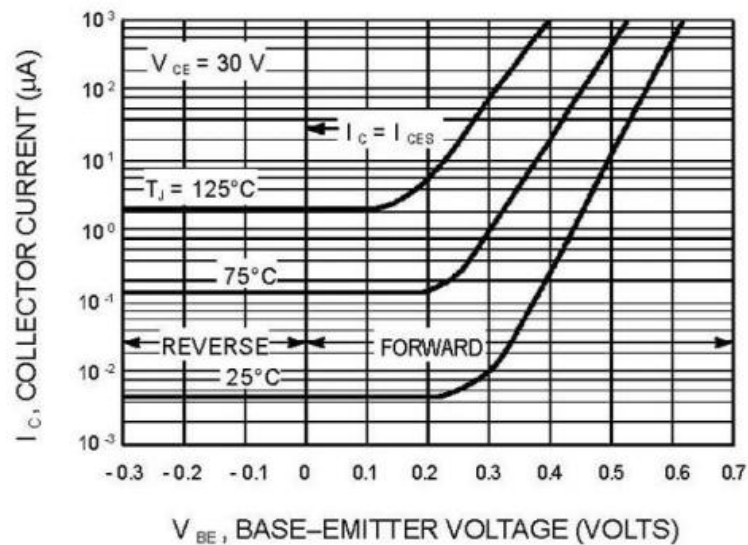


Figure 3. Collector Cut-Off Region

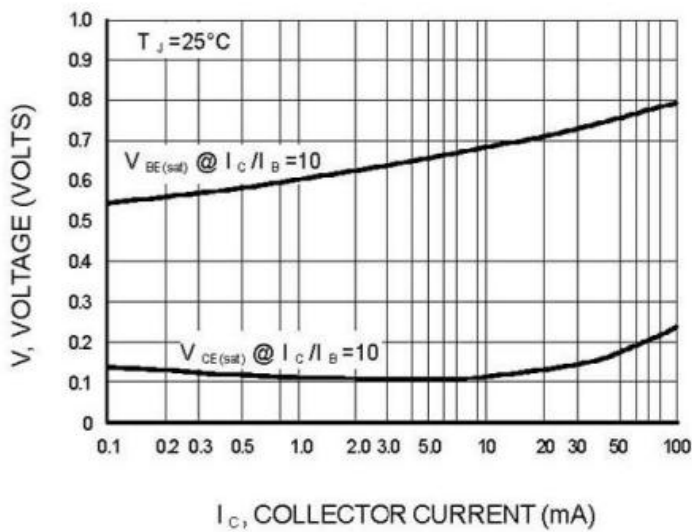


Figure 4. "On" Voltages

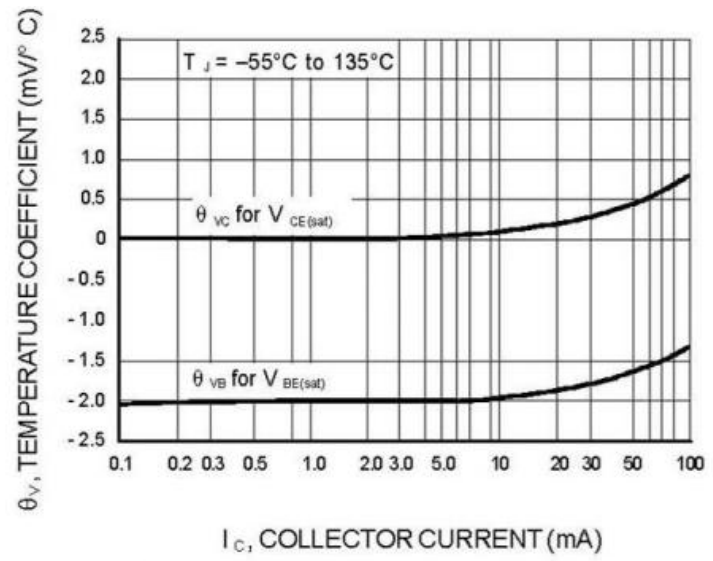


Figure 5. Temperature Coefficients

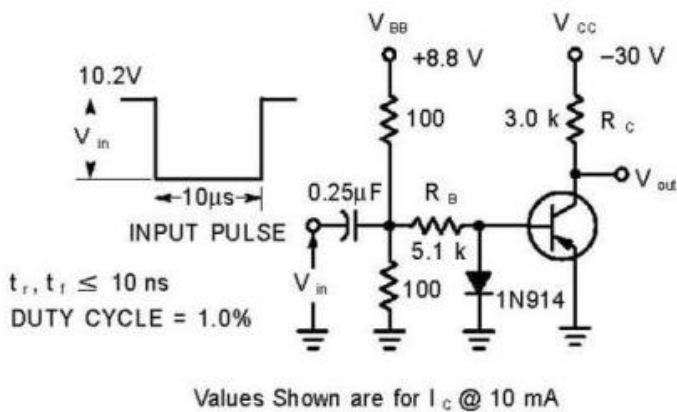


Figure 6. Switching Time Test Circuit

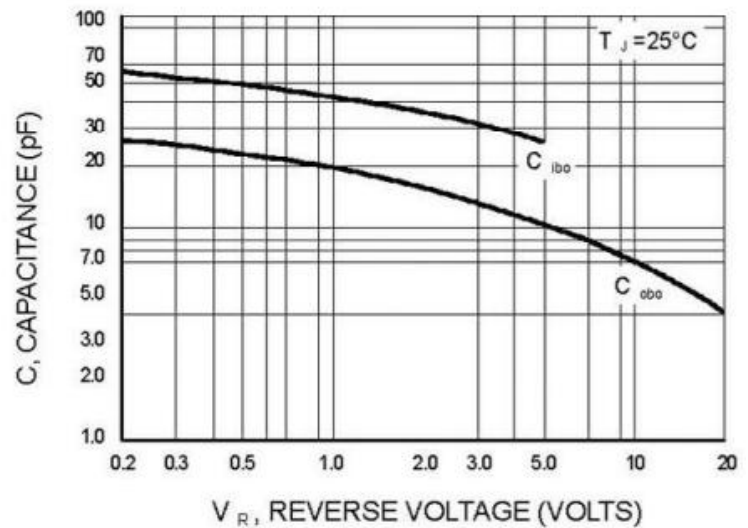


Figure 7. Capacitances

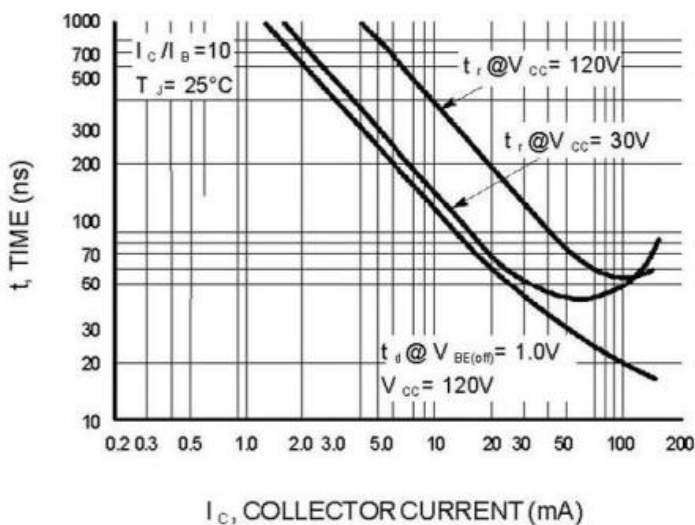


Figure 8. Turn-On Time

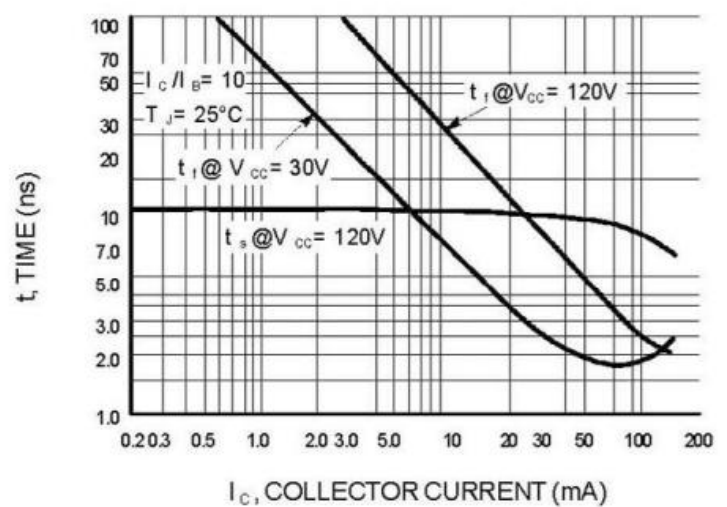


Figure 9. Turn-Off Time

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

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