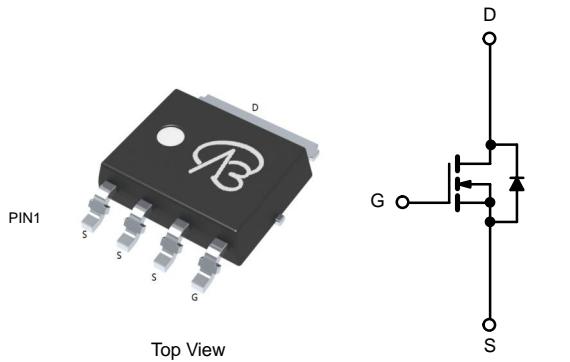


PSMN1R2-30YLD-VB Datasheet

N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^{a, c}	Q_g (Typ.)
40	0.0007 at $V_{GS} = 10$ V	150	80 nC
	0.0008 at $V_{GS} = 7.5$ V	120	



N-Channel MOSFET

FEATURES

- SGT Power MOSFET
- 100 % R_g and UIS Tested



APPLICATIONS

- Synchronous Rectification
- Power Supplies

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	40		V
Gate-Source Voltage	V_{GS}	± 25		
Continuous Drain Current ($T_J = 175$ °C)	$T_C = 25$ °C	150 ^{a, c}	A	
	$T_C = 70$ °C			
	$T_A = 25$ °C			
	$T_A = 70$ °C			
Pulsed Drain Current	I_{DM}	450		
Avalanche Current Pulse	I_{AS}	80		
Single Pulse Avalanche Energy	E_{AS}	320	mJ	
Continuous Source-Drain Diode Current	$T_C = 25$ °C	120 ^{a, c}	A	
	$T_A = 25$ °C			
Maximum Power Dissipation	$T_C = 25$ °C	375 ^a	W	
	$T_C = 70$ °C			
	$T_A = 25$ °C			
	$T_A = 70$ °C			
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175		°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^b	R_{thJA}	32	40	°C/W
Maximum Junction-to-Case	R_{thJC}	0.33	0.4	

Notes:

a. Based on $T_C = 25$ °C.

b. Surface Mounted on 1" x 1" FR4 board.

c. Calculated based on maximum junction temperature. Package limitation current is 150 A.

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

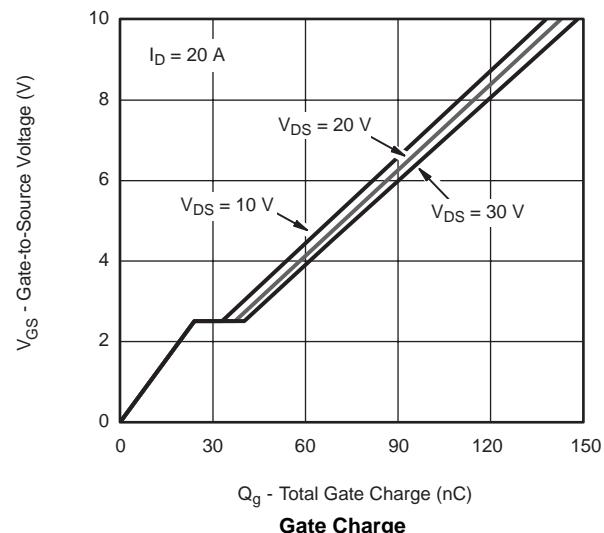
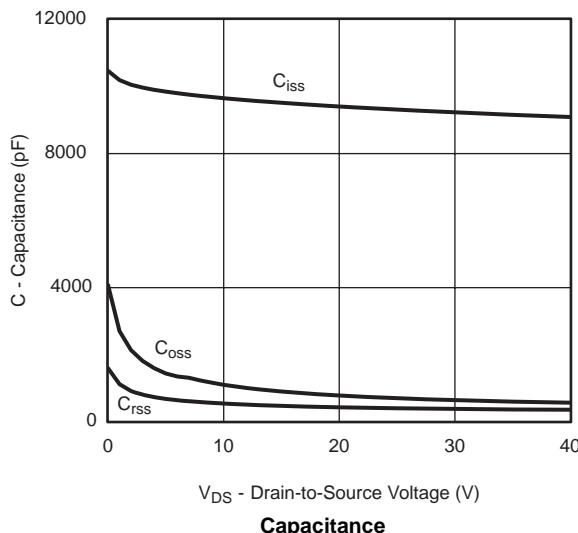
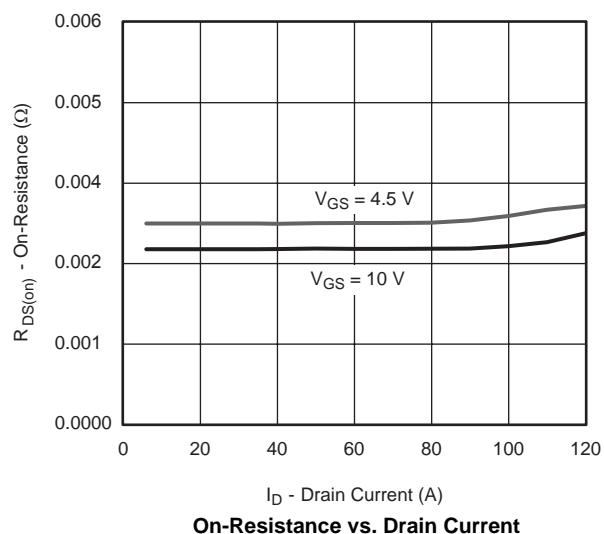
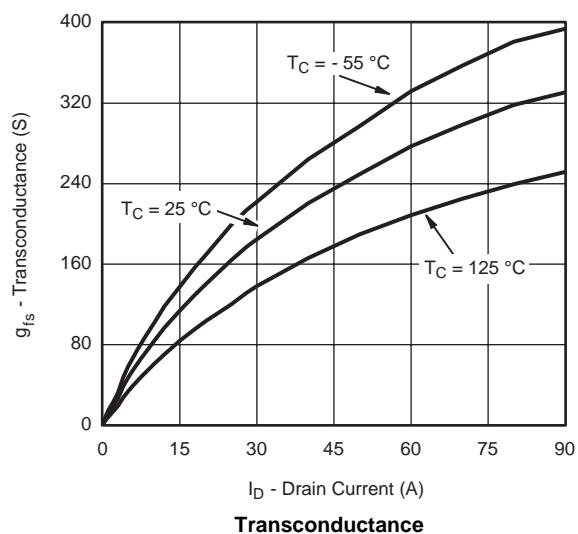
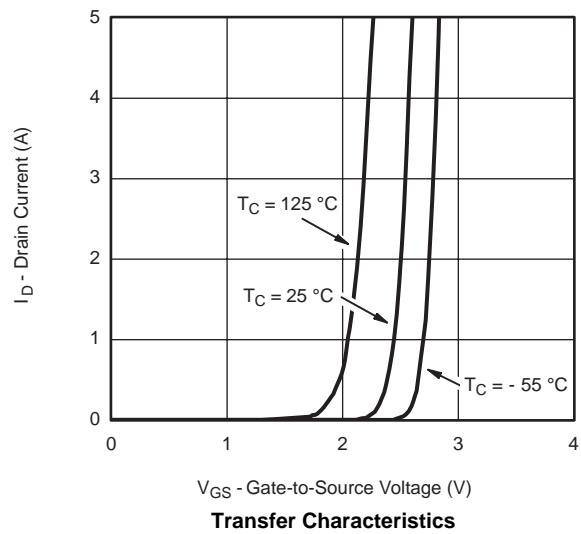
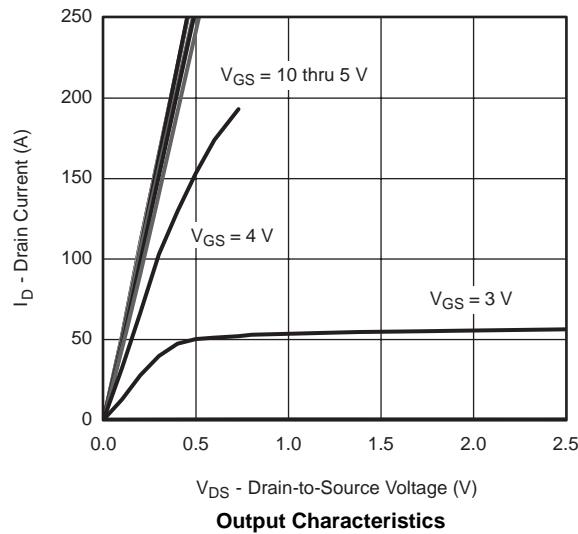
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		41		$\text{mV}/^\circ\text{C}$
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			-8		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2		4	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	150			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}$		0.0007		Ω
		$V_{GS} = 7.5 \text{ V}, I_D = 20 \text{ A}$		0.0008		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 30 \text{ A}$		100		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		6000		pF
Output Capacitance	C_{oss}			1650		
Reverse Transfer Capacitance	C_{rss}			450		
Total Gate Charge	Q_g	$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		80	100	nC
Gate-Source Charge	Q_{gs}			30		
Gate-Drain Charge	Q_{gd}			16		
Gate Resistance	R_g	$f = 1 \text{ MHz}$		0.85	1.3	Ω
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 20 \text{ V}, R_L = 1.0 \Omega$ $I_D \geq 20 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		20	30	ns
Rise Time	t_r			11	17	
Turn-Off Delay Time	$t_{d(\text{off})}$			77	115	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(\text{on})}$			20		
Rise Time	t_r	$V_{DD} = 20 \text{ V}, R_L = 1.0 \Omega$ $I_D \geq 20 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		18		ns
Turn-Off Delay Time	$t_{d(\text{off})}$			50		
Fall Time	t_f			30		
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			120	A
Pulse Diode Forward Current ^a	I_{SM}				200	
Body Diode Voltage	V_{SD}	$I_S = 20 \text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 20 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$			50	ns
Body Diode Reverse Recovery Charge	Q_{rr}				40	
Reverse Recovery Fall Time	t_a				20	
Reverse Recovery Rise Time	t_b				17	

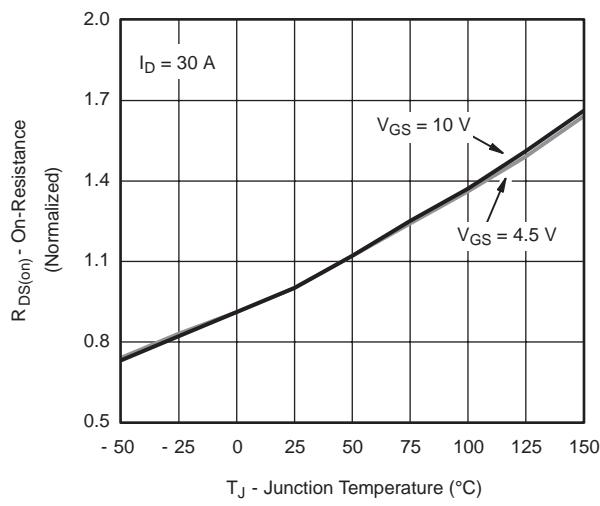
Notes:

a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

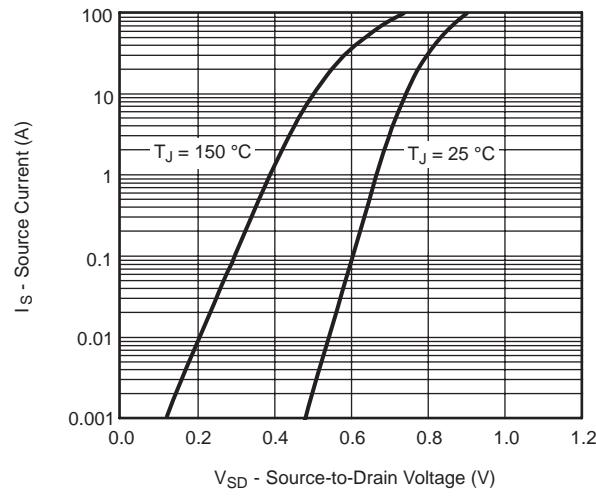
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

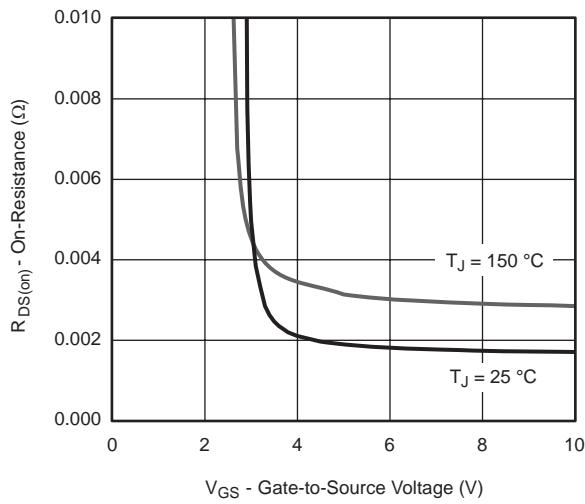
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


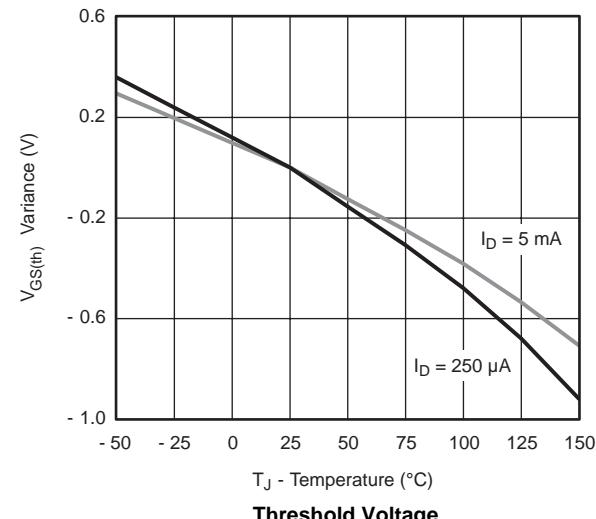
On-Resistance vs. Junction Temperature



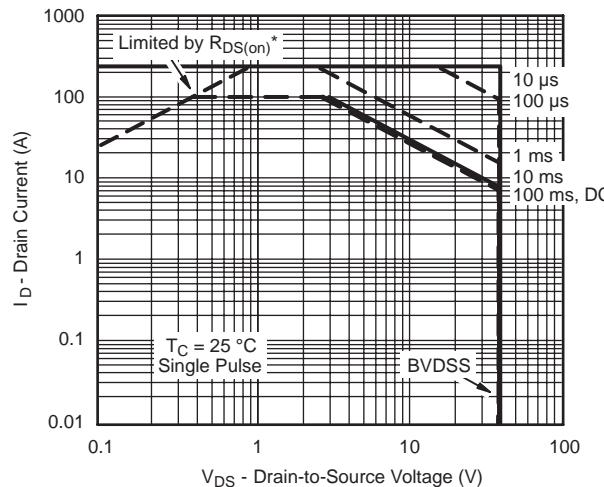
Forward Diode Voltage vs. Temperature



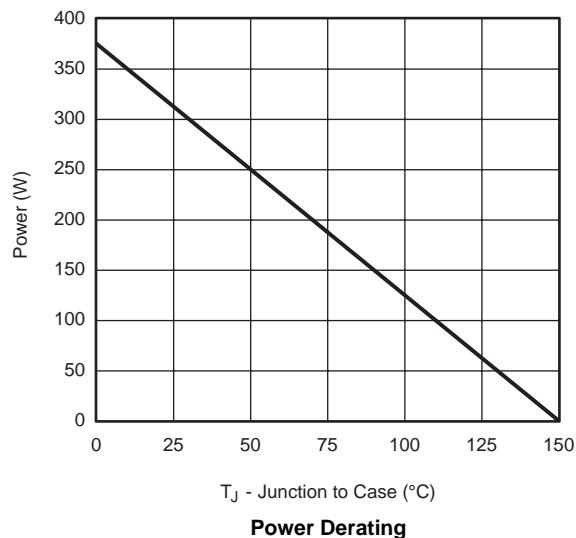
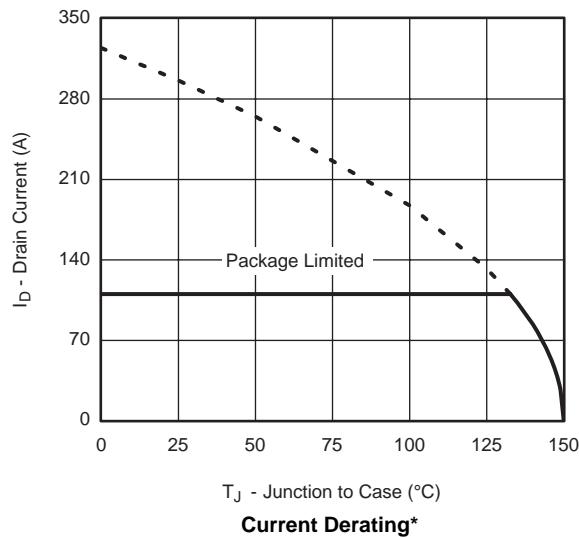
On-Resistance vs. Gate-to-Source Voltage



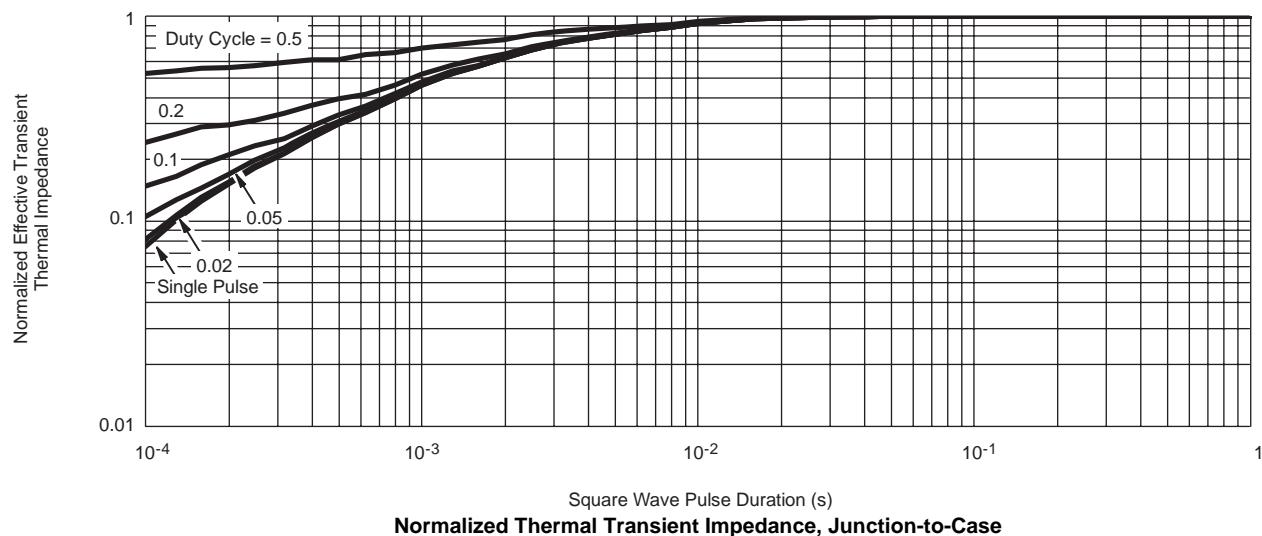
Threshold Voltage



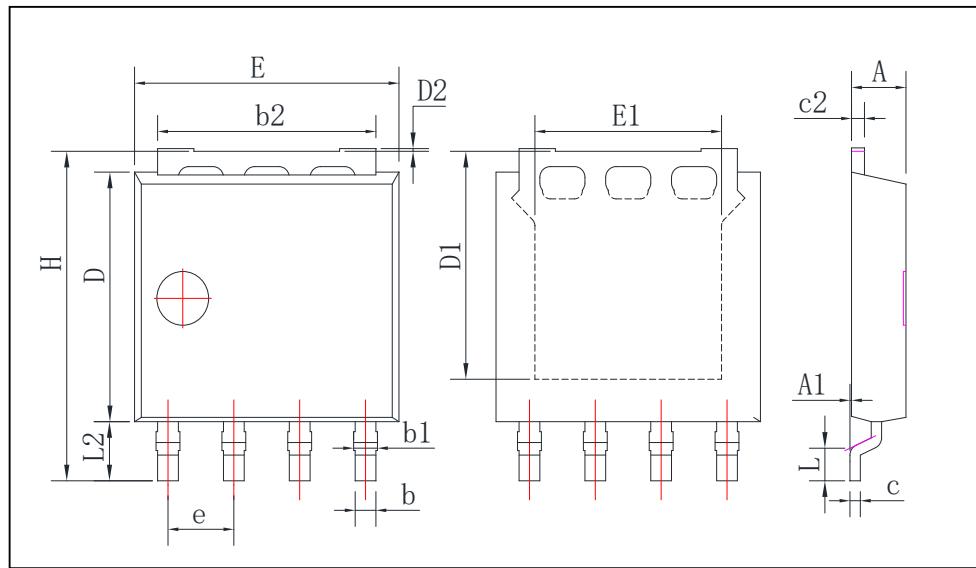
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



LFPAK56 CASE OUTLINE



Symbol	Min	Typ	Max
A	1.00	1.05	1.10
A1	0.00		0.15
b	0.35	0.40	0.50
b1	0.40	0.48	0.58
b2	4.01	4.21	4.41
c	0.18	0.20	0.25
c2	0.23	0.25	0.30
D	4.44	4.59	4.70
D1	4.10	4.24	4.40
D2			0.20
e	1.22	1.27	1.32
E	5.00	5.10	5.25
E1	3.50	3.60	3.70
H	6.05	6.15	6.25
L	0.40	0.60	0.80
L2	0.90	1.10	1.30

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