THCV353-Q

Audio Visual Serializer with bi-directional transceiver

1. General Description

THCV353-Q is designed to support 1080p60 24bit uncompressed video data on 100ohm differential STP or 50ohm Coaxial cable between graphic processor and panel display.

THCV353-Q supports audio.

THCV353-Q supports bi-directional command communication including 2-wire interface and GPIO, which can configure touch panel interface remote bridge.

2. Applications

Automotive Infotainment Display
Instrument Cluster Display
Industrial Display

3. Features

- AEC-Q100 Grade2 (-40 to 105˚C)
- V-by-One® HSII 4Gbps 2lane
- MIPI D-PHY / DSI receiver
  - Up to 1.5Gbps/lane and 4 data lanes
  - Support dual link
- Pixel Clock
  - Single Link: 5 to 116MHz
  - Dual-Link: 50 to 232MHz
- Color depth per pixel:18bit, 24bit
- Video Splitting
- Back Channel GPIO support up to 120kbps
- 2-wire 1Mbps serial interface bridge function
- Remote side GPIO control and monitoring
- 15 meters of cable transmission
- Wide range IO voltage from 1.71V to 3.465V
- Additional spread spectrum on data stream
- Error Detect and Notification
- 0.5mm pitch QFN64 9x9mm package

4. Block Diagram

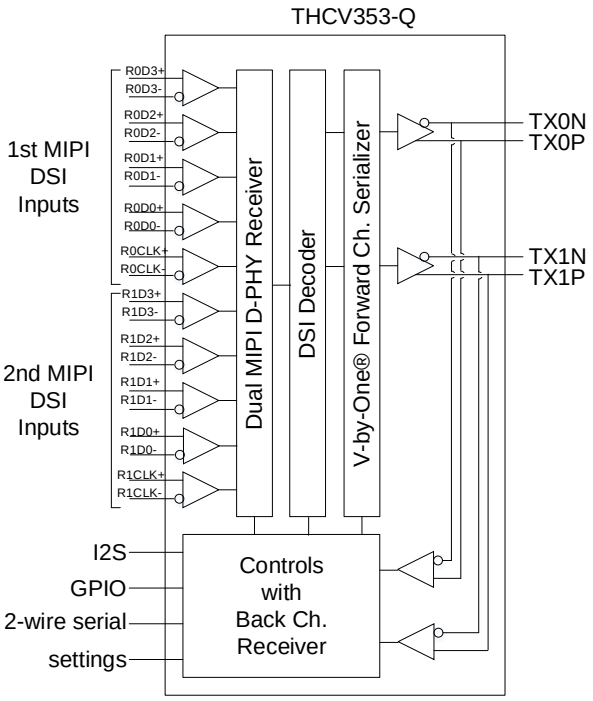

Figure 1. Block Diagram

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5. Pin Configuration and Functions

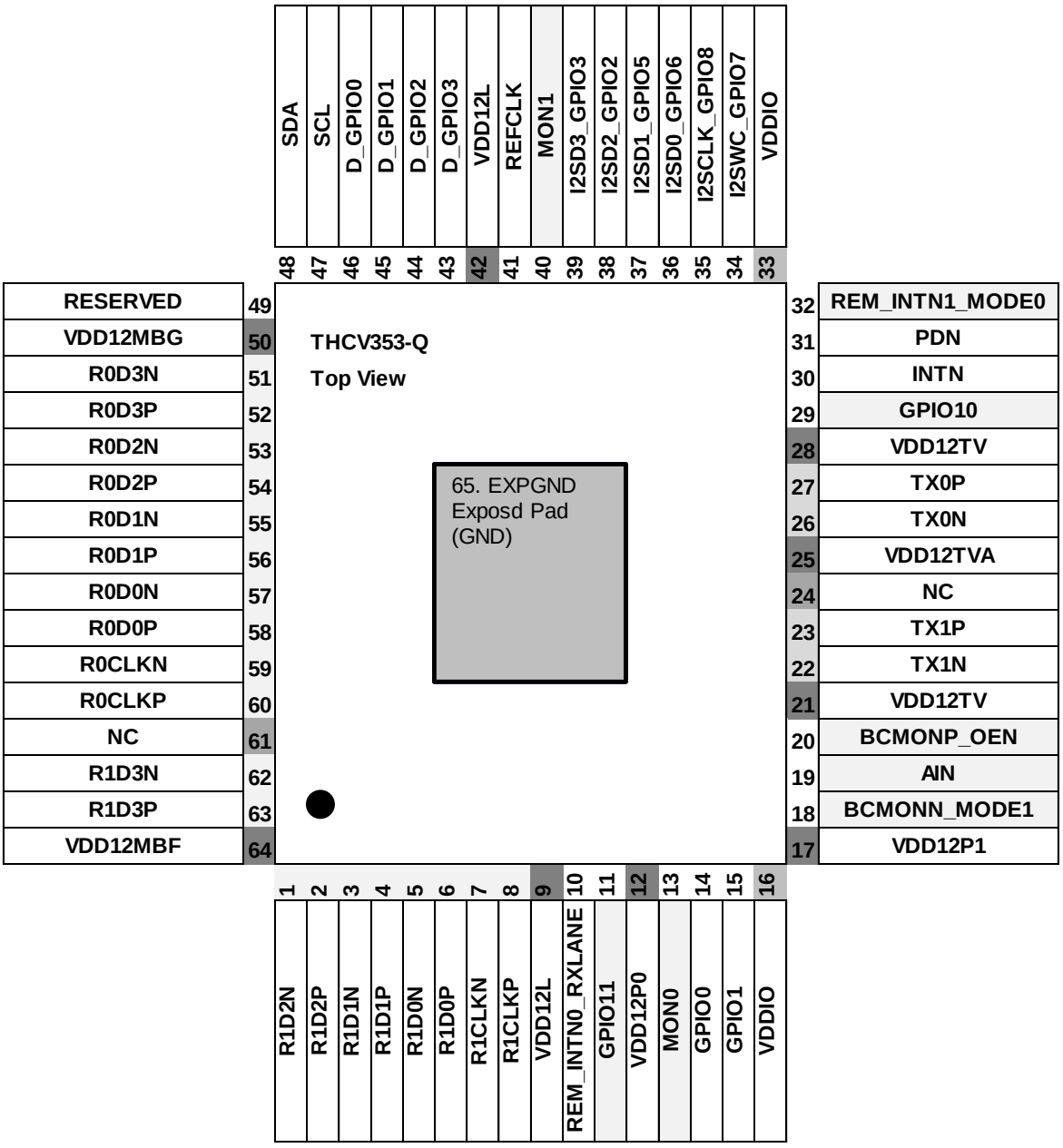


Figure 2. Pin Configuration

Pin Functions

Settings				
Pin Name	Pin#	I/O	PU/PD*	Description
RESERVED	49	B	PD	**Must be tied to GND** 0: GND MUST 1: Not Allowed.
REM_INT1_MODE0	32	B	PD	**Mode0 Select** Please refer to Mode guide MODE0 Setting can be override by register.
BCMONN_MODE1	18	B	PD	**Mode1 Select** Please refer to Mode guide MODE1 Setting can be override by register.
PDN	31	IL	PD	**Chip Power Down Negative** 0: Power-Down State 1: Normal Operation
REM_INTN0_RXLANE	10	B	PD	**MIPI DSI RX Lane Select** 0: 4lane 1: 2lane RXLANE Setting can be override by register.
BCMONP_OEN	20	B	PD	**Forward Ch. Output Enable** 0: Output Enable 1: Output Disable OEN Setting can be override by register.
2-Wire Serial Interface				
Pin Name	Pin#	I/O	PU/PD*	Description
AIN	19	B	PD	**Device Address Setting for 2-Wire Serial Interface** 0 : Device Address = 7'h0B (=7'b000_1011) 1 : Device Address = 7'h34 (=7'b011_0100)
SCL	47	B2	PU	**2-wire serial I/F Clock Line** Recommended ~4.7kohm pull-up to VDDIO.
SDA	48	B2	PU	**2-wire serial I/F Data Line** Recommended ~4.7kohm pull-up to VDDIO.
Reference Clock				
Pin Name	Pin#	I/O	PU/PD*	Description
REFCLK	41	B	PD	**Reference Clock Input**

I:VDDIO CMOS Input, IL/IL2:VDDIO CMOS Input (Low speed), O:VDDIO CMOS Output, B/B2:VDDIO CMOS Input and Output,

MI:MIPI D-PHY Input, VO:V-by-One® Forward Ch. Output and Back Ch. Input, BM:Back Ch. monitor Output, PS:Power Supply

*PU/PD:Pull-Up/Down hardware initial state with pre-installed weak internal resister. PU/PD become active when particular pin is PCB open.

Pin Functions (continued)

General Purpose I/O				
Pin Name	Pin#	I/O	PU/PD*	Description
GPIO0, GPIO1, I2SD2_GPIO2, I2SD3_GPIO3, I2SD1_GPIO5, I2SD0_GPIO6, I2SWC_GPIO7, I2SCLK_GPIO8, GPIO10, GPIO11, D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3	14, 15, 38, 39, 37, 36, 34, 35, 29, 11, 46, 45, 44, 43	B	PD	**General Purpose Input Output**
Interrupt				
Pin Name	Pin#	I/O	PU/PD*	Description
INTN	30	B	PD	**Interrupt Signal Output (default Open-Drain)** 0: Interrupt State 1: No Interrupt State Recommended ~4.7kohm pull-up to VDDIO. DO NOT FLOAT.
REM_INTN0_RXLANE REM_INTN1_MODE0	10, 32	B	PD	**Remote Interrupt Signal Output** 0: Interrupt State 1: No Interrupt State
Signal Monitor				
Pin Name	Pin#	I/O	PU/PD*	Description
MON0, MON1	13, 40	O	PD	**Internal Status Monitor**
I2S Interface				
Pin Name	Pin#	I/O	PU/PD*	Description
I2SWC_GPIO7	34	I	PD	**I2S WC(Word Clock) input**
I2SCLK_GPIO8	35	I	PD	**I2S Bit Clock input**
I2SD0_GPIO6	36	I	PD	**I2S Data input 0**
I2SD1_GPIO5	37	I	PD	**I2S Data input 1**
I2SD2_GPIO2	38	I	PD	**I2S Data input 2**
I2SD3_GPIO3	39	I	PD	**I2S Data input 3**

I:VDDIO CMOS Input, IL:VDDIO CMOS Input (Low speed), O:VDDIO CMOS Output, B:VDDIO CMOS Input and Output, PU/PD:Pull-Up/Down
MI:MIPI D-PHY Input, VO:V-by-One® Forward Ch. Output and Back Ch. Input, BM:Back Ch. monitor Output, PS:Power Supply
*PU/PD:Pull-Up/Down hardware initial state with pre-installed weak internal resister. PU/PD become active when particular pin is PCB open.

Pin Functions (continued)

V-by-One® HS II Forward Channel Tx / Back Channel Rx				
Pin Name	Pin#	I/O	P-Domain	Description
TX0P, TX0N	27, 26	VO	VDD12TV	**V-by-One® HS II FC Tx Output** (0lane) **Back Channel Rx Input** (0lane)
TX1P, TX1N	23, 22	VO	VDD12TV	**V-by-One® HS II FC Tx Output** (1lane) **Back Channel Rx Input** (1lane)
MIPI DSI Rx				
Pin Name	Pin#	I/O	P-Domain	Description
R0D3P, R0D3N	52, 51	MI	VDD12MBF	**MIPI DSI Input** (Port0 Data Lane3) If unused, they are recommended to tie to VDD12MBF with 10kohm. See 7.3.1.
R0D2P, R0D2N	54, 53	MI	VDD12MBF	**MIPI DSI Input** (Port0 Data Lane2) If unused, they are recommended to tie to VDD12MBF with 10kohm. See 7.3.1.
R0D1P, R0D1N	56, 55	MI	VDD12MBF	**MIPI DSI Input** (Port0 Data Lane1) If unused, they are recommended to tie to VDD12MBF with 10kohm. See 7.3.1.
R0D0P, R0D0N	58, 57	MI	VDD12MBF	**MIPI DSI Input** (Port0 Data Lane0) If unused, they are recommended to tie to VDD12MBF with 10kohm. See 7.3.1.
R0CLKP, R0CLKN	60, 59	MI	VDD12MBF	**MIPI DSI Input** (Port0 Clock) If unused, they are recommended to tie to VDD12MBF with 10kohm. See 7.3.1.
R1D3P, R1D3N	63, 62	MI	VDD12MBF	**MIPI DSI Input** (Port1 Data Lane3) If unused, they are recommended to tie to VDD12MBF with 10kohm. See 7.3.1.
R1D2P, R1D2N	2, 1	MI	VDD12MBF	**MIPI DSI Input** (Port1 Data Lane2) If unused, they are recommended to tie to VDD12MBF with 10kohm. See 7.3.1.
R1D1P, R1D1N	4, 3	MI	VDD12MBF	**MIPI DSI Input** (Port1 Data Lane1) If unused, they are recommended to tie to VDD12MBF with 10kohm. See 7.3.1.
R1D0P, R1D0N	6, 5	MI	VDD12MBF	**MIPI DSI Input** (Port1 Data Lane0) If unused, they are recommended to tie to VDD12MBF with 10kohm. See 7.3.1.
R1CLKP, R1CLKN	8, 7	MI	VDD12MBF	**MIPI DSI Input** (Port1 Clock) If unused, they are recommended to tie to VDD12MBF with 10kohm. See 7.3.1.

I:VDDIO CMOS Input, IL:VDDIO CMOS Input (Low speed), O:VDDIO CMOS Output, B:VDDIO CMOS Input and Output, PU/PD:Pull-Up/Down

MI:MIPI D-PHY Input, VO:V-by-One® Forward Ch. Output and Back Ch. Input, BM:Back Ch. monitor Output, PS:Power Supply

Pin Functions (continued)

BC receive monitor				
Pin Name	Pin#	I/O	P-Domain	Description
BCMONP_OEN, BCMONN_MODE1	20, 18	BM	VDDIO	**Throughout received Back Channel Signal**
Power Line				
Pin Name	Pin#	I/O	P-Domain	Description
VDDIO	16,33	PS	VDDIO	**Power Supply for LVCMOS I/O. (1.8V/3.3V)**
VDD12L	9,42	PS	VDD12L	**Power Supply for Digital (1.2V)**
VDD12P0	12	PS	VDD12P0	**Power Supply for PLL. (1.2V)**
VDD12P1	17	PS	VDD12P1	**Power Supply for PLL. (1.2V)**
VDD12TV	21,28	PS	VDD12TV	**Power Supply for V-by-One Tx and Back Channel Analog. (1.2V)**
VDD12TVA	25	PS	VDD12TVA	**Power Supply for V-by-One PLL. (1.2V)**
VDD12MBG	50	PS	VDD12MBG	**Power Supply for MIPI D-PHY. (1.2V)**
VDD12MBF	64	PS	VDD12MBF	**Power Supply for MIPI D-PHY. (1.2V)**
EXPGND	65	PS	VSSEXP	**Exposed Pad Ground** Must be tied to PCB Ground
Others				
Pin Name	Pin#	I/O	P-Domain	Description
NC	24,61	-	-	**Not Connected or connect to power**

I:VDDIO CMOS Input, IL:VDDIO CMOS Input (Low speed), O:VDDIO CMOS Output, B:VDDIO CMOS Input and Output, PU/PD:Pull-Up/Down

MI:MIPI D-PHY Input, VO:V-by-One® Forward Ch. Output and Back Ch. Input, BM:Back Ch. monitor Output, PS:Power Supply

6. Specifications

6.1. Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings*

Parameter	min.	typ.	max.	Unit
Supply Voltage (VDDIO)	-0.3	-	+4.0	V
Supply Voltage (VDD12L,VDD12P0,VDD12P1,VDD12TV, VDD12TVA,VDD12MBG,VDD12MBF)	-	-	1.6	V
LVCMOS Input Voltage	-0.3	-	VDDIO+0.3	V
LVCMOS Output Voltage	-0.3	-	VDDIO+0.3	V
LVCMOS Bi-directional buffer Input Voltage	-0.3	-	VDDIO+0.3	V
LVCMOS Bi-directional buffer Output Voltage	-0.3	-	VDDIO+0.3	V
MIPI Input Voltage	-0.3	-	VDD12MBF+0.3	V
Forward Channel CML Transmitter / Back Channel Receiver Voltage	-0.3	-	VDD12TV+0.3	V
Storage Temperature	-55	-	+125	˚C
Junction Temperature	-	-	+125	˚C
Reflow Peak Temperature/time	-	-	+260/10	˚C/sec

* “Absolute Maximum Ratings” are values of safety limit for a device beyond which a device safety cannot be guaranteed.

They do not imply that a device should be operated at these limits. The tables of “Recommended Operating Condition” specify conditions for device operation.

6.2. Electrostatic discharge Ratings

Table 2. Electrostatic discharge (ESD) Ratings

Symbol	Parameter	Condition		Value	Unit
VESD	Electrostatic Discharge	Human Body Model (HBM) on AEC-Q100-002		+/-2000	V
		Charged Device Model (CDM) on AEC-Q100-011		+/-750	
		IEC61000-4-2	Air Discharge	+/-15000	
			Contact Discharge	+/-8000	
		ISO10605	Air Discharge	+/-15000	
			Contact Discharge	+/-8000	

6.3. Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	min.	typ.	max.	Unit
Supply Voltage (VDDIO)	3.135	3.300	3.465	V
	1.89	-	3.135	V
	1.71	1.8	1.89	V
Supply Voltage (VDD12L,VDD12P0,VDD12P1,VDD12TV, VDD12TVA,VDD12MBG,VDD12MBF)	1.14	1.2	1.26	V
Operating Temperature (Ta)	-40	-	105	˚C

6.4. Thermal Information

Table 4. Thermal Information

Symbol	Parameter	Value	Unit
θja	Junction-to-ambient thermal resistance	27.06	˚C/W
Ψjt	Junction-to-top characterization parameter	3.46	˚C/W

6.5. DC Specifications

6.5.1. LVCMOS DC Specifications

Table 5. LVCMOS DC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
IIH	Input Leak Current High	-	-10	-	+10	uA
IIL	Input Leak Current Low	-	-10	-	+10	uA
VIH1	High Level Input Voltage (I, IL and B)	VDDIO=3~3.465V	2.00	-	VDDIO	V
		VDDIO=2~3V	0.70*VDDIO	-	VDDIO	V
		VDDIO=1.71~2V	0.65*VDDIO	-	VDDIO	V
VIL1	Low Level Input Voltage (I, IL and B)	VDDIO=3~3.465V	0	-	0.80	V
		VDDIO=2~3V	0	-	0.30*VDDIO	V
		VDDIO=1.71~2V	0	-	0.35*VDDIO	V
VIH2	High Level Input Voltage (B2)	-	0.70*VDDIO	-	VDDIO	V
VIL2	Low Level Input Voltage (B2)	-	0	-	0.30*VDDIO	V
VOH	High Level Output Voltage	IOH=1mA	VDDIO-0.45		VDDIO	V
VOL	Low Level Output Voltage	IOL=1mA	0	-	0.45	V

6.5.2. CML Forward Channel Transmitter DC Specifications

Table 6. CML Forward Channel (FC) Transmitter DC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
VTOD	CML Differential Mode Output Voltage	DRV[1:0]=00	133	200	267	mV
		DRV[1:0]=01	200	300	400	mV
		DRV[1:0]=10	300	400	500	mV
		DRV[1:0]=11	350	450	550	mV
VTOC	CML Common Mode Output Voltage		-	VDD12TV-VTOD	-	mV
ITOZH	CML Output Leak Current High	PDN=L			10	uA
ITOZL	CML Output Leak Current Low	PDN=L			10	uA
ITOS	CML Output Short Current	VDDTV=1.2V	-60		-38.4	mA

6.5.3. MIPI DSI Receiver D-PHY DC Specifications

Table 7. MIPI D-PHY Receiver DC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
Vcmrx(DC)	MIPI D-PHY Voltage input common Rx	HS mode	70	200	330	mV
Vidth	MIPI D-PHY Voltage diff. input high thres.	HS mode	-	-	70	mV
Vidtl	MIPI D-PHY Voltage diff. input low thres.	HS mode	-70	-	-	mV
Vihhs	MIPI D-PHY Single-end. input high limit at HS mode	HS mode	-	-	460	mV
Vilhs	MIPI D-PHY Single-end. input low limit at HS mode	HS mode	-40	-	-	mV
Vterm-en	MIPI D-PHY Single-ended threshold for HS termination enable	HS mode	-	-	450	mV
Zid	MIPI D-PHY differential input impedance	HS mode	80	100	125	Ohm

6.6. AC Specifications

6.6.1. General AC Specifications

Table 8. General AC Specifications (1/4)

Symbol	Parameter	Condition	min.	typ.	max.	unit
tDL_V2V_01	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Single CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: 8cycle mode DSI.Data-rate.input=648Mbps DSI.bpp=24(RGB888) PCLK.input=108MHz Low Freq: x1mode	333*1/(PCLK.input*DSIportNum/FClaneNum) +10	343*1/(PCLK.input*DSIportNum/FClaneNum)	353*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_03	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Single CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: Off DSI.Data-rate.input=648Mbps DSI.bpp=24(RGB888) PCLK.input=108MHz Low Freq: x1mode	338*1/(PCLK.input*DSIportNum/FClaneNum) +10	348*1/(PCLK.input*DSIportNum/FClaneNum)	358*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_04	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Single CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: 8cycle mode DSI.Data-rate.input=175Mbps DSI.bpp=24(RGB888) PCLK.input=29.17MHz Low Freq: x1mode	332*1/(PCLK.input*DSIportNum/FClaneNum) +10	342*1/(PCLK.input*DSIportNum/FClaneNum)	352*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_05	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Single CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: 4cycle mode DSI.Data-rate.input=175Mbps DSI.bpp=24(RGB888) PCLK.input=29.17MHz Low Freq: x1mode	323*1/(PCLK.input*DSIportNum/FClaneNum) +10	333*1/(PCLK.input*DSIportNum/FClaneNum)	343*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_06	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Single CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: 8cycle mode DSI.Data-rate.input=175Mbps DSI.bpp=24(RGB888) PCLK.input=29.17MHz Low Freq: x2mode	256*1/(PCLK.input*DSIportNum/FClaneNum) +10	266*1/(PCLK.input*DSIportNum/FClaneNum)	276*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_07	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Single CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: 4cycle mode DSI.Data-rate.input=175Mbps DSI.bpp=24(RGB888) PCLK.input=29.17MHz Low Freq: x2mode	247*1/(PCLK.input*DSIportNum/FClaneNum) +10	257*1/(PCLK.input*DSIportNum/FClaneNum)	267*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_08	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Single CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: 8cycle mode DSI.Data-rate.input=175Mbps DSI.bpp=24(RGB888) PCLK.input=29.17MHz Low Freq: x4mode	215*1/(PCLK.input*DSIportNum/FClaneNum) +10	225*1/(PCLK.input*DSIportNum/FClaneNum)	235*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_10	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Dual CML FC output Des: Dual CML FC input/ Single-Link oLDI output FC_THRIO: 8cycle mode DSI.Data-rate.input=891Mbps DSI.bpp=24(RGB888) PCLK.input=148.5MHz Low Freq: x1mode	268*1/(PCLK.input*DSIportNum/FClaneNum) +10	278*1/(PCLK.input*DSIportNum/FClaneNum)	288*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_11	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Dual CML FC output Des: Dual CML FC input/ Single-Link oLDI output FC_THRIO: 4cycle mode DSI.Data-rate.input=891Mbps DSI.bpp=24(RGB888) PCLK.input=148.5MHz Low Freq: x1mode	260*1/(PCLK.input*DSIportNum/FClaneNum) +10	270*1/(PCLK.input*DSIportNum/FClaneNum)	280*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_12	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Dual CML FC output Des: Dual CML FC input/ Dual-Link oLDI output FC_THRIO: 8cycle mode DSI.Data-rate.input=891Mbps DSI.bpp=24(RGB888) PCLK.input=148.5MHz Low Freq: x1mode	324*1/(PCLK.input*DSIportNum/FClaneNum) +10	334*1/(PCLK.input*DSIportNum/FClaneNum)	344*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns

*Serializer above table is THCV353-Q. Deserializer above table is THCV334-Q.

Table 9. General AC Specifications (continued 2/4)

Symbol	Parameter	Condition	min.	typ.	max.	unit
tDL_V2V_13	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Dual CML FC output Des: Dual CML FC input/ Dual-Link oLDI output FC_THRIO: 4cycle mode DSI.Data-rate.input=891Mbps DSI.bpp=24(RGB888) PCLK.input=148.5MHz Low Freq: x1mode	317*1/(PCLK.input*DSIportNum/FClaneNum)	327*1/(PCLK.input*DSIportNum/FClaneNum)	337*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_14	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Dual CML FC output Des: Dual CML FC input/ Dual-Link oLDI output FC_THRIO: 8cycle mode DSI.Data-rate.input=175Mbps DSI.bpp=24(RGB888) PCLK.input=29.17MHz Low Freq: x2mode	299*1/(PCLK.input*DSIportNum/FClaneNum)	309*1/(PCLK.input*DSIportNum/FClaneNum)	319*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_15	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Dual CML FC output Des: Dual CML FC input/ Dual-Link oLDI output FC_THRIO: 4cycle mode DSI.Data-rate.input=175Mbps DSI.bpp=24(RGB888) PCLK.input=29.17MHz Low Freq: x2mode	298*1/(PCLK.input*DSIportNum/FClaneNum)	308*1/(PCLK.input*DSIportNum/FClaneNum)	318*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_16	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Dual CML FC output Des: Dual CML FC input/ Dual-Link oLDI output FC_THRIO: 8cycle mode DSI.Data-rate.input=175Mbps DSI.bpp=24(RGB888) PCLK.input=29.17MHz Low Freq: x4mode	203*1/(PCLK.input*DSIportNum/FClaneNum)	213*1/(PCLK.input*DSIportNum/FClaneNum)	223*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_17	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Dual CML FC output Des: Dual CML FC input/ Dual-Link oLDI output FC_THRIO: 4cycle mode DSI.Data-rate.input=175Mbps DSI.bpp=24(RGB888) PCLK.input=29.17MHz Low Freq: x4mode	202*1/(PCLK.input*DSIportNum/FClaneNum)	212*1/(PCLK.input*DSIportNum/FClaneNum)	222*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_18	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Dual CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: 8cycle mode DSI.Data-rate.input=891Mbps DSI.bpp=24(RGB888) PCLK.input=148.5MHz Low Freq: x1mode	318*1/(PCLK.input*DSIportNum/FClaneNum)	328*1/(PCLK.input*DSIportNum/FClaneNum)	338*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_19	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Dual-port(4Lane) input/Dual CML FC output Des: Dual CML FC input/ Dual-Link oLDI output FC_THRIO: 8cycle mode DSI.Data-rate.input=512Mbps DSI.bpp=24(RGB888) PCLK.input=85.378MHz Low Freq: x1mode	332*1/(PCLK.input*DSIportNum/FClaneNum)	342*1/(PCLK.input*DSIportNum/FClaneNum)	352*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_20	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Single-port(4Lane) input/Dual CML FC output Des: Dual CML FC input/ Dual-Link oLDI output FC_THRIO: 4cycle mode DSI.Data-rate.input=512Mbps DSI.bpp=24(RGB888) PCLK.input=85.378MHz Low Freq: x1mode	325*1/(PCLK.input*DSIportNum/FClaneNum)	335*1/(PCLK.input*DSIportNum/FClaneNum)	345*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_21	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Dual-port(4Lane) input/Dual CML FC output Des: Dual CML FC input/ Dual-Link oLDI output FC_THRIO: 8cycle mode DSI.Data-rate.input=445.5Mbps DSI.bpp=24(RGB888) PCLK.input=74.25MHz Low Freq: x1mode	334*1/(PCLK.input*DSIportNum/FClaneNum)	344*1/(PCLK.input*DSIportNum/FClaneNum)	354*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_22	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Dual-port(4Lane) input/Dual CML FC output Des: Dual CML FC input/ Dual-Link oLDI output FC_THRIO: 4cycle mode DSI.Data-rate.input=445.5Mbps DSI.bpp=24(RGB888) PCLK.input=74.25MHz Low Freq: x1mode	328*1/(PCLK.input*DSIportNum/FClaneNum)	338*1/(PCLK.input*DSIportNum/FClaneNum)	348*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns

*Serializer above table is THCV353-Q. Deserializer above table is THCV334-Q.

Table 10. General AC Specifications (continued 3/4)

Symbol	Parameter	Condition	min.	typ.	max.	unit
tDL_V2V_23	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Dual-port(4Lane) input/Dual CML FC output Des: Dual CML FC input/ Dual-Link oLDI output FC_THRIO: 8cycle mode DSI.Data-rate.input=512Mbps DSI.bpp=24(RGB888) PCLK.input=85.378MHz Low Freq: x1mode	332*1/(PCLK.input*DSIportNum/FClaneNum)	342*1/(PCLK.input*DSIportNum/FClaneNum)	352*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_V2V_24	Data Latency Video from Serializer input to Deserializer output	Ser: MIPI Dual-port(4Lane) input/Dual CML FC output Des: Dual CML FC input/ Dual-Link oLDI output FC_THRIO: 4cycle mode DSI.Data-rate.input=512Mbps DSI.bpp=24(RGB888) PCLK.input=85.378MHz Low Freq: x1mode	327*1/(PCLK.input*DSIportNum/FClaneNum)	337*1/(PCLK.input*DSIportNum/FClaneNum)	347*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_A2A_01	Data latency Audio from Serializer input to Deserializer Output	Ser: I2S_WC input Des: I2S_WC output Ser: MIPI Single-port(4Lane) input/Single CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: 8cycle mode DSI.Data-rate.input=648Mbps DSI.bpp=24(RGB888) PCLK.input=108MHz Low Freq: x1mode	103*1/(PCLK.input*DSIportNum/FClaneNum)	113*1/(PCLK.input*DSIportNum/FClaneNum)	123*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_A2A_02	Data latency Audio from Serializer input to Deserializer Output	Ser: I2S_WC input Des: I2S_WC outputSer: MIPI Single-port(4Lane) input/Dual CML FC output Des: Dual CML FC input/ Single-Link oLDI output FC_THRIO: 8cycle mode DSI.Data-rate.input=891Mbps DSI.bpp=24(RGB888) PCLK.input=148.5MHz Low Freq: x1mode	89*1/(PCLK.input*DSIportNum/FClaneNum)	99*1/(PCLK.input*DSIportNum/FClaneNum)	109*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_A2A_03	Data latency Audio from Serializer input to Deserializer Output	Ser: I2S_WC input Des: I2S_WC outputSer: MIPI Single-port(4Lane) input/Dual CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: 8cycle mode DSI.Data-rate.input=891Mbps DSI.bpp=24(RGB888) PCLK.input=148.5MHz Low Freq: x1mode	88*1/(PCLK.input*DSIportNum/FClaneNum)	98*1/(PCLK.input*DSIportNum/FClaneNum)	108*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_A2A_04	Data latency Audio from Serializer input to Deserializer Output	Ser: I2S_WC input Des: I2S_WC output DSI.Data-rate.input=512MbpsSer: MIPI Dual-port(4Lane) input/Dual CML FC output Des: Dual CML FC input/ Dual-Link oLDI output FC_THRIO: 8cycle mode DSI.bpp=24(RGB888) PCLK.input=85.378MHz Low Freq: x1mode	90*1/(PCLK.input*DSIportNum/FClaneNum)	100*1/(PCLK.input*DSIportNum/FClaneNum)	110*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns

*Serializer above table is THCV353-Q. Deserializer above table is THCV334-Q.

Table 11. General AC Specifications (continued 4/4)

Symbol	Parameter	Condition	min.	typ.	max.	unit
tDL_GPI2FC2GPO	Data latency Through GPIO from Serializer GPI to Deserializer GPO	FC THRIO_MODE=8cycle FC Through GPIO=8bit Ser: MIPI Single-port(4Lane) input/Single CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: 8cycle mode DSI.Data-rate.input=648Mbps DSI.bpp=24(RGB888) PCLK.input=108MHz Low Freq: x1mode	89*1/(PCLK.input*DSIportNum/FClaneNum)	99*1/(PCLK.input*DSIportNum/FClaneNum)	109*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_GPI2BC2GPO	Data latency Through GPIO from Deserializer GPI to Serializer GPO	BC Through GPIO=8bit DSI.Data-rate.input=648Mbps Ser: MIPI Single-port(4Lane) input/Single CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: 8cycle mode DSI.bpp=24(RGB888) PCLK.input=108MHz Low Freq: x1mode	887*1/(PCLK.input*DSIportNum/FClaneNum)	897*1/(PCLK.input*DSIportNum/FClaneNum)	907*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_2WIRE WRITE2FC2REM2WIRE	Data latency 2-wire remote wirte from Serializer input to Deserializer output	FC THRIO_MODE=8cycle DSI.Data-rate.input=648Mbps Ser: MIPI Single-port(4Lane) input/Single CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: 8cycle mode DSI.bpp=24(RGB888) PCLK.input=108MHz Low Freq: x1mode	407*1/(PCLK.input*DSIportNum/FClaneNum)	417*1/(PCLK.input*DSIportNum/FClaneNum)	427*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_2WIRE WRITEACK2BC2LOCAL2WIRE	Data latency 2-wire remote ACK from Deserializer input to Serializer output	FC THRIO_MODE=8cycle DSI.Data-rate.input=648Mbps Ser: MIPI Single-port(4Lane) input/Single CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: 8cycle mode DSI.bpp=24(RGB888) PCLK.input=108MHz Low Freq: x1mode	2019*1/(PCLK.input*DSIportNum/FClaneNum)	2029*1/(PCLK.input*DSIportNum/FClaneNum)	2039*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_2WIRE READ2FC2REM2WIRE	Data latency 2-wire remote read from Serializer input to Deserializer output	FC THRIO_MODE=8cycle DSI.Data-rate.input=648Mbps Ser: MIPI Single-port(4Lane) input/Single CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: 8cycle mode DSI.bpp=24(RGB888) PCLK.input=108MHz Low Freq: x1mode	379*1/(PCLK.input*DSIportNum/FClaneNum)	389*1/(PCLK.input*DSIportNum/FClaneNum)	399*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_2WIRE READBACK2BC2LOCAL2WIRE	Data latency 2-wire remote read from Deserializer input to Serializer output	FC THRIO_MODE=8cycle DSI.Data-rate.input=648Mbps Ser: MIPI Single-port(4Lane) input/Single CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: 8cycle mode DSI.bpp=24(RGB888) PCLK.input=108MHz Low Freq: x1mode	2436*1/(PCLK.input*DSIportNum/FClaneNum)	2446*1/(PCLK.input*DSIportNum/FClaneNum)	2456*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns
tDL_INTIN2INTN	Data Latency Interrupt from Deserializer INTN_IN to Serializer INTN	FC THRIO_MODE=8cycle DSI.Data-rate.input=648Mbps Ser: MIPI Single-port(4Lane) input/Single CML FC output Des: Single CML FC input/ Single-Link oLDI output FC_THRIO: 8cycle mode DSI.bpp=24(RGB888) PCLK.input=108MHz Low Freq: x1mode	1907*1/(PCLK.input*DSIportNum/FClaneNum)	1917*1/(PCLK.input*DSIportNum/FClaneNum)	1927*1/(PCLK.input*DSIportNum/FClaneNum) +10	ns

*Serializer above table is THCV353-Q. Deserializer above table is THCV334-Q.

6.6.2. MIPI DSI Receiver D-PHY AC Specifications

Table 12. MIPI DSI Receiver AC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
UI	Unit Interval	-	0.666 (1.5Gbps)	-	12.5 (80Mbps)	ns
tSETUP	Data to Clock Setup Time	80Mbps<UI UI<1Gbps	-	-	0.15*UI	ps
tSETUP	Data to Clock Setup Time	1Gbps<UI UI<1.5Gbps	-	-	0.2*UI	ps
tHOLD	Clock to Data Hold Time	80Mbps<UI UI<1Gbps	-	-	0.15*UI	ps
tHOLD	Clock to Data Hold Time	1Gbps<UI UI<1.5Gbps	-	-	0.2*UI	ps

6.6.3. CML Forward Channel Transmitter AC Specifications

Table 13. CML Forward Channel (FC) Transmitter AC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
TTFCBIT	TXxP/N out each bit Period Forward Ch. (Unit Interval)		250 (4Gbps)	-	1000 (1Gbps)	ps
FTFC	Forward Channel Data-Rate	-	1.0	-	4.0	Gbps
TTRF	CML Output Rise and Fall Time (20-80%)	-	50	-	150	ps
TTOSK_INTRA	Intra-pair Skew	-		-	40	ps
TTOSK_INTER	Inter-pair Skew between TX0P/N and TX1P/N	-		-	2	UI
Δmod	Spread Spectrum Clock Amplitude Tolerance	30KHz modulation	-0.5		0.5	%

6.6.4. CML Back Channel Receiver AC Specifications

Table 14. CML Back Channel Receiver AC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
TTBCBIT	TXxP/N input each bit Period Back Channel (Unit Interval)		37.5 (26.7Mbps)	TTFCBIT *150	150 (6.7Mbps)	ns

6.6.5. 2-wire serial Interface AC Specifications

Table 15. 2-wire serial Interface AC Specifications

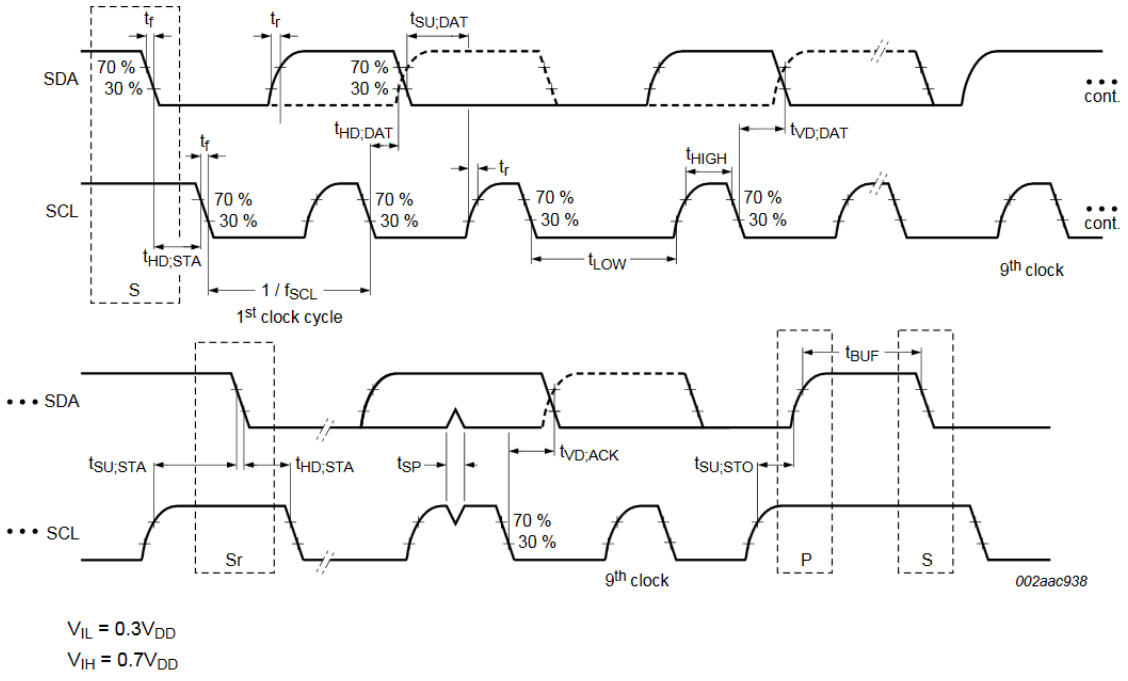
Symbol	Parameter	Condition	min.	typ.	max.	Unit
t_{OSC}	Cycle of internal oscillator clock	-	10.4	12.5	15.7	ns
F_{scl}	SCL clock frequency	-	-	-	1000	kHz
t_{LOW}	LOW period of the SCL clock	-	0.5	-	-	us
t_{HIGH}	HIGH period of the SCL clock	-	0.26	-	-	us
$t_{HD;STA}$	hold time START condition	-	0.26	-	-	us
$t_{SH;STA}$	set-up time for a repeated START condition	-	0.26	-	-	us
$t_{HD;DAT}$	Data hold time (input)	-	0	-	-	ns
$t_{SU;DAT}$	Data setup time (input)	-	50	-	-	ns
t_r	rise time of both SDA and SCL signals	-	-	-	120	ns
t_f	fall time of both SDA and SCL signals	pull-up:2.5kohm bus cap:400pF	-	-	120	ns
$t_{SU;STO}$	set-up time for STOP condition	-	0.26	-	-	us
t_{BUF}	Bus free time between a STOP and START condition	-	0.5	-	-	us
$t_{VD;DAT}$	Data valid time				0.45	us
$t_{VD;ACK}$	Data valid acknowledge time				0.45	us
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	-	-	-	50	ns
t_{PDS}	Required wait time from PDN high to START condition	-	500	-	-	us

6.6.6. Power On and Lock/Re-Lock Sequence AC Specifications

Table 16. Power On Sequence AC Specifications

symbol	discription	min	typ	max	unit
t1	1.8V to 1.2V	0	0	-	us
t2	Internal Pow er On Reset	1	-	-	us
t3	PDN Pin ReleaseTime	-	any	-	us
t5	OSC EN to CLKOUT output delay	4.99	-	8.75	us
t6	Register Access Enable from tOSC start after Reset Release	80	100	120	us
t720	Received clock processing	-	-	2	ms
t8	FNPLL Lock Time	-	500	1000	1/F(PFD) Cycle
t9	FC PLL Lock Time	-	0.5	1	ms
t10	FCBC CX Link Up Time	-	-	10	ms

6.6.7. AC Specifications Timing Diagrams



$V_{IL} = 0.3V_{DD}$
$V_{IH} = 0.7V_{DD}$

Figure 3. 2-wire serial Interface AC timing

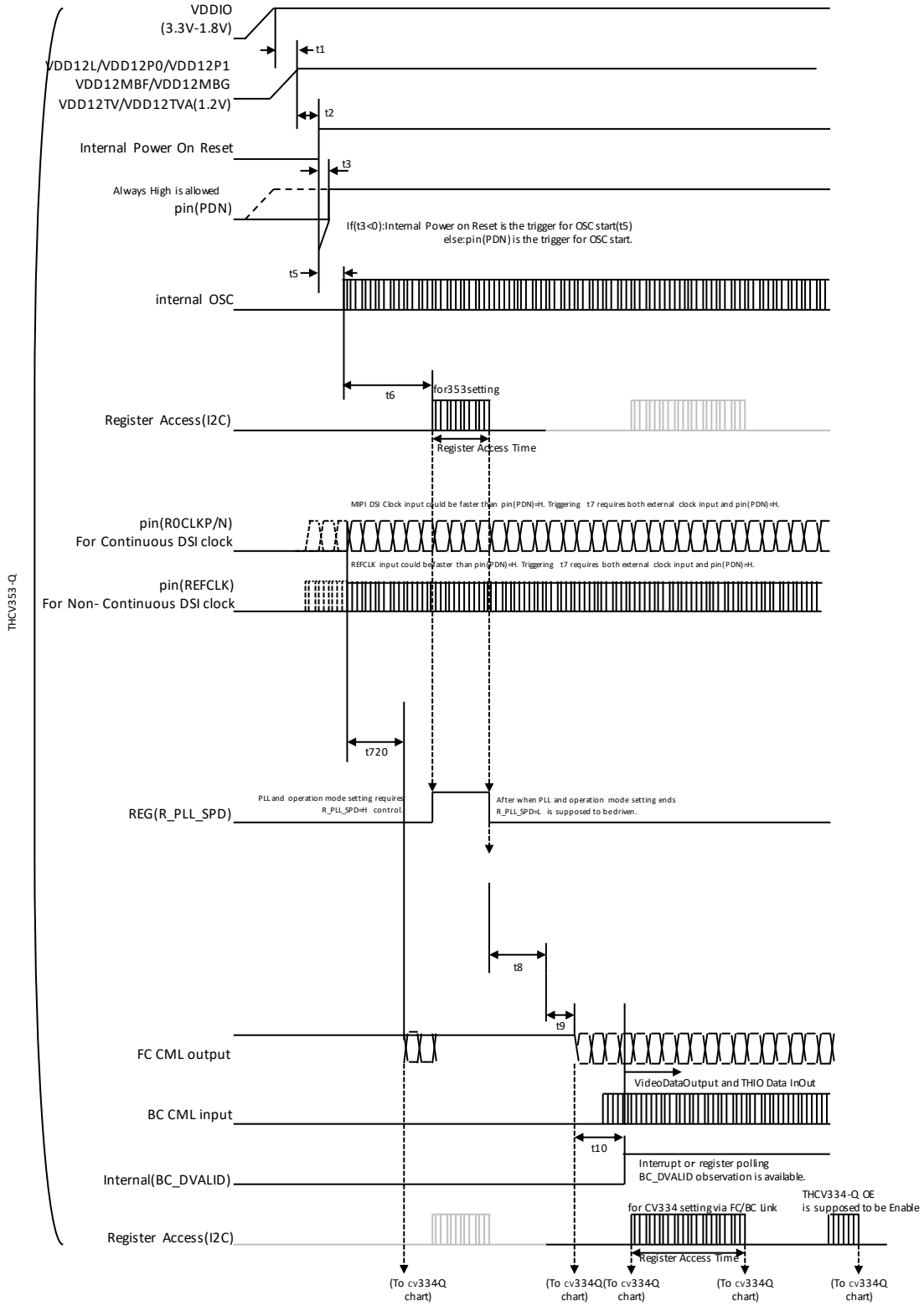


Figure 4. THCV353-Q Power On Sequence

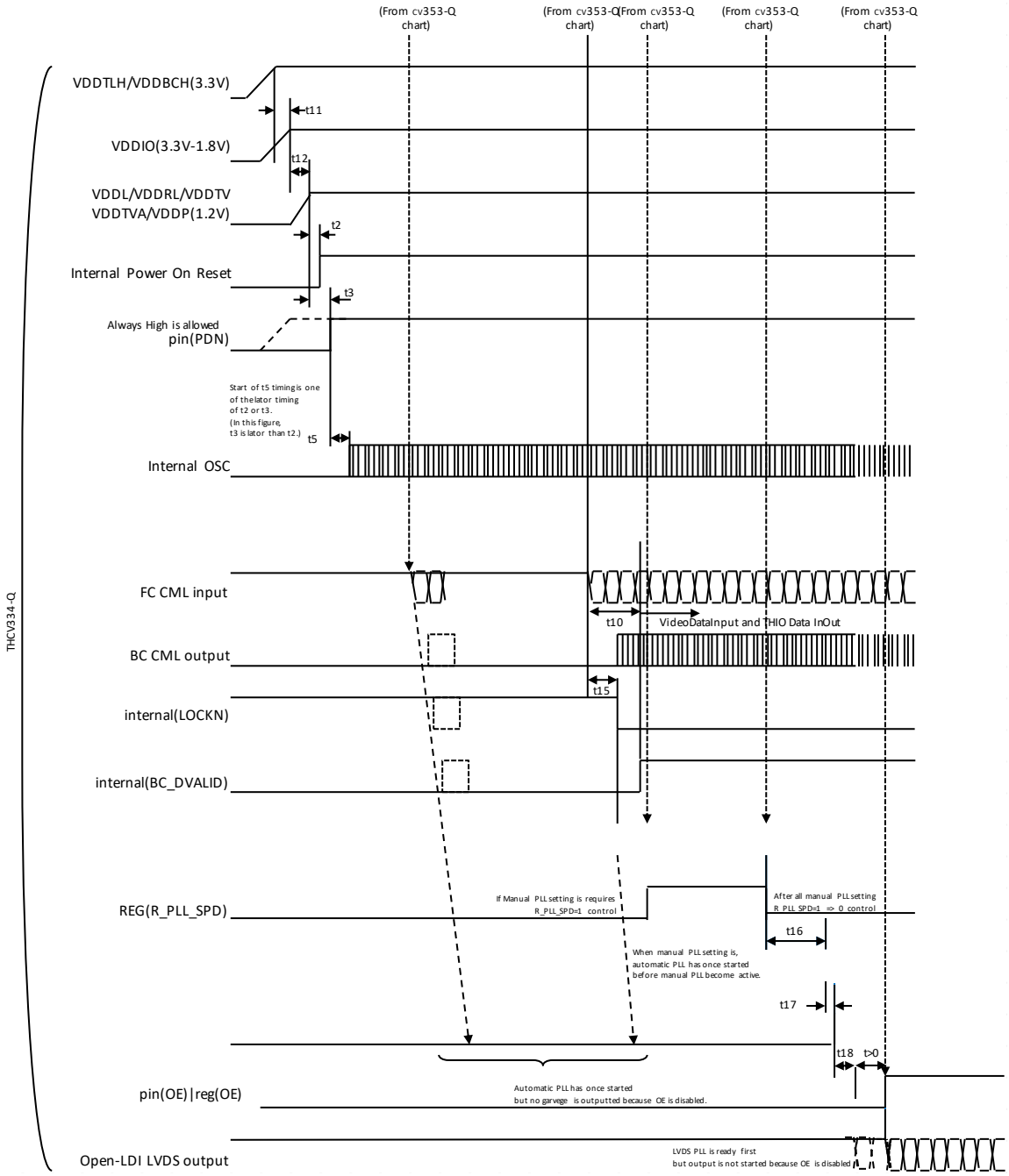


Figure 5. THCV334-Q Power On Sequence Register Entry

6.7. Consumption Current

Table 17. Consumption Current at Power Down

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ICCSIO33	Power Down Supply Current	PDN=0, VDDIO=3.465V	-	0.01	0.1	mA
ICCSIO18		PDN=0, VDDIO=1.89V	-	0.01	0.1	mA
ICCS12		PDN=0, VDD12L,VDD12P0,VDD12P1,VDD12TV, VDD12TVA,VDD12MBG,VDD12MBF =1.26V	-	1	60	mA

Table 18. Consumption Current of VDDIO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ITCCWIO_33_1	VDDIO=3.3V	No Audio, No GPIO	-	0.02	0.07	mA
ITCCWIO_33_2		I2S Audio 48kHz 16bit stereo, No GPIO	-	0.03	0.08	mA
ITCCWIO_33_3		No Audio, GPIO UART 115200bps Tx/Rx and PWM 20kHz 99% to FC	-	0.07	0.12	mA
ITCCWIO_33_4		I2S Audio 48kHz 16bit stereo, GPIO UART 115200bps Tx/Rx and PWM 20kHz 99% to FC	-	0.07	0.12	mA
ITCCWIO_18_1	VDDIO=1.8V	No Audio, No GPIO	-	0.001	0.03	mA

Table 19. Consumption Current of VDD12

Symbol	port.in#	port.out#	video format	input	output	min.	typ.	max.	Unit
ITCCW12_1	1	1	640x480p60 RGB888	25MHz x 24bitRGB Single-Link	1Gbps x1lane	-	82.7	126.3	mA
ITCCW12_2	1	1	1920x720p60(1) RGB888	85MHz x 24bitRGB Single-Link	3Gbps x1lane	-	140.5	188.2	mA
ITCCW12_3	1	1	1920x720p60(2) RGB888	116MHz x 24bitRGB Single-Link	4Gbps x1lane	-	155.8	209.1	mA
ITCCW12_4	1	2	1920x1080p60(1) RGB888	150MHz x 24bitRGB Single-Link	2.6Gbps x2lane	-	207.5	262.9	mA
ITCCW12_5	1	2	1920x720p60(3) RGB888	85MHz x 24bitRGB Single-Link	3Gbps x2lane (Replicate)	-	199.9	253.8	mA
ITCCW12_11	1	2	1920x720p60(3)x2 RGB888	85MHz x 24bitRGB x2 Single-Link to Split	3Gbps x2lane (Split)	-	234.7	293.5	mA
ITCCW12_15	1	2	1920x720p60(3)x2 RGB888	85MHz x 24bitRGB x2 Single-Link to Split & Crop	3Gbps x2lane (Split & Crop)	-	239.0	299.0	mA
ITCCW12_9	2	2	3840x720p60 RGB888	116MHzx24bitRGB Dual-Link (232MHz)	4Gbps x2lane	-	283.1	347.0	mA
ITCCW12_21	2	2	1920x1080p60(2) /2 x2 RGB888	75MHz x 24bitRGB (Align) Dual to Combine (150MHz)	2.6Gbps x2lane (Combine)	-	229.5	284.9	mA
ITCCW12_31	2	2	1920x720p60(1) RGB888 1920x720p60(2) RGB888	85MHz x 24bitRGB (Async) 116MHz x 24bitRGB (Async)	3Gbps x1lane (Async) 4Gbps x1lane (Async)	-	278.0	339.5	mA

Condition: Checkerboard Pattern

7. Detailed Description

7.1. Overview

The THCV353-Q is a Display Serial Interface (DSI) to V-by-One® HS II interface Bridge device that, in conjunction with the THCV334-Q deserializers over two low-cost, 50 Ω coaxial or two 100 Ω shielded twisted-pair (STP) cables, transmits high-resolution video, audio, and control information. Each of the dual DSI links has (4 lanes + 1 clock). They support video resolutions up to 2K with 24-bit color depth, and translates into dual-pair high-speed serialized interfaces. The serial bus scheme, V-by-One® HS II, supports video and audio data transmission and full duplex control including I2C communication over two differential links. Consolidation of video data and control over two differential pairs reduce the interconnect size and weight, while also eliminating skew issues and simplifying system design. EMI is minimized by the use of low voltage differential signaling, data scrambling, and randomization. In backward-compatible operation, the device supports link to the THCV242-Q or other V-by-One® HS deserializers.

The THCV353-Q supports up to eight I2S audio channels. Audio data received from the I2S input is encrypted and sent over the V-by-One® HS II interfaces where it can be regenerated at up to 8-channel I2S interface or maximum sample rate of 192 kHz.

7.2. Functional Block Diagram

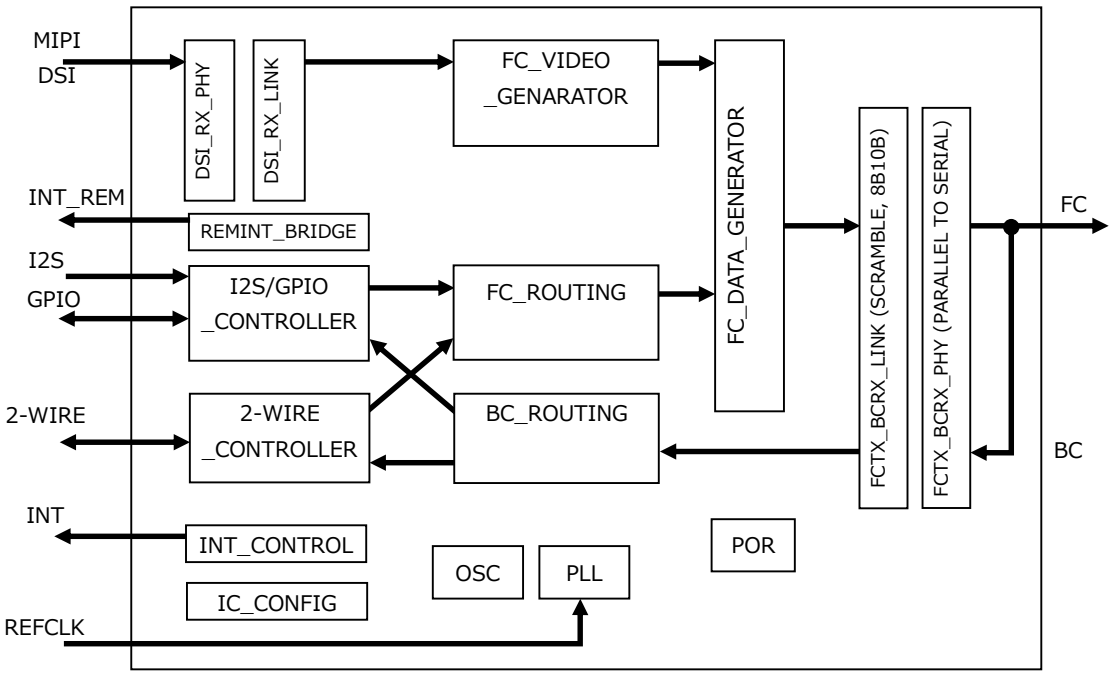


Figure 6. Functional Block Diagram

7.3. Feature Description

The THCV353-Q implements a bridge between a DSI interface and dual V-by-One® HS II interface. The device integrates a DSI Receiver with the V-by-One® HS II Transmitters to provide audio and video transmission.

7.3.1. DSI Receiver

The THCV353-Q features two separate MIPI D-PHY v1.2 / DSI v1.3.1 compliant input ports. Selection of DSI input port could be selectable by register. Each port allows 1, 2 or 4-lane operation (0x0109, 0x010A). The number of lanes for both ports is controlled by register, and may be set at power up through a strap option on the REM_INTN0_RXLANE pin. Automatic lane detection is not supported.

The DSI lane ordering can be reversed internally and independently for each of the two DSI ports, using register (0x010B, 0x010C). To set an independent lane number from 0 to 3 for each RXSWAP_Lx_REG_P0/1 allows arbitrary lane swap.

In addition, the DSI clock and data lane polarity can be inverted internally and independently for each of the two D-PHY ports (0x010E):

0x010E [0] RXFLIP_P0 = 0x1:

- DSI0_D3P/N -> DSI0_D3N/P
- DSI0_D2P/N -> DSI0_D2N/P
- DSI0_D1P/N -> DSI0_D1N/P
- DSI0_D0P/N -> DSI0_D0N/P

0x010E [1] RXFLIPCLK_P0 = 0x1:

- DSI0_CLKP/N -> DSI0_CLKN/P

0x010E [4] RXFLIP_P1 = 0x1:

- DSI1_D3P/N -> DSI1_D3N/P
- DSI1_D2P/N -> DSI1_D2N/P
- DSI1_D1P/N -> DSI1_D1N/P
- DSI1_D0P/N -> DSI1_D0N/P

0x010E [5] RXFLIPCLK_P1 = 0x1:

- DSI1_CLKP/N -> DSI1_CLKN/P

RXLANE0SEL(0x0109) and RXLANE1SEL(0x010A) setting of MIPI DSI must be previously set before MODE_REG_OVERRIDE(0x0100[4])=1 Enable activation.

For only single MIPI DSI input mode of operation, MIPI DSI setting RXLANESEL_OVERRIDE_P1(0x010A[4]) must be set to 0x0 from default value 0x1.

When MIPI DSI port1 is unused, RX1VREFEN/ RX1IREFEN(0x010D) setting had better be changed to 0x03 from default value 0x33 to reduce unintended small power consumption. Another method of this topic is to tie unused DSI port1 pins to VDD12MBF with 10kohm if RX1VREFEN/ RX1IREFEN(0x010D)=0x03 is not set. When RX1VREFEN/ RX1IREFEN(0x010D)=0x03 is set, any pin condition (e.g. open, GND, etc.) does not result in unintended small power consumption. Unused DSI pins have the same topic and recommended to tie to . VDD12MBF with 10kohm.

For non-continuous MIPI DSI clock input, REFCLK_EN_REG (0x0108[0]) should be Enabled to 0x1 and RXLOCKN_EN_Px (0x001A[0] and 0x005A[0]) should be Disabled to 0x0. Also PLL manual operation setting is required.

7.3.1.1. DSI Operating Modes

The D-PHY receiver can be in High-Speed (HS) or Escape mode. During normal operation, a Data Lane will be in High-Speed mode. In Escape Mode, the D-PHY will be in a Low-Power (LP) State. In High-Speed mode, the data transmission happens in a burst and may start and end at a Stop state (LP-11), or remain in HS mode with null or blanking packets transmitted. There is a transition state to take the D-PHY from a Normal mode to the Low-Power state.

The sequence to enter High-Speed mode is: LP-11, LP-01, LP-00 at which point the Data Lane remains in High-Speed mode until a Stop state (LP-11) is received.

High-Speed Mode

During high-speed data transmission, the digital D-PHY will enable termination signal to allow proper termination of the HS RX, and the LP RX should stay at LP-00 state. Both DSI data lane and clock lane operate in the same manner. The THCV353-Q supports DSI continuous clock lane mode where the clock LP RX stays at LP-00 state.

Low-Power Mode

Low power data transmission and low power escape modes are not supported.

MIPI D-PHY v1.2 defines global operation timing for both D-PHY TX and RX. The THCV353-Q implements RX timing parameters by register (0x0406, 0x0407, 0x0506 and 0x0507).

7.3.1.2. DSI Errors and Status

The THCV353-Q detects and reports DSI errors.

- SoT 1bit Error
- Packet header ECC 1bit Error
- Packet header ECC 2bit Error

7.3.1.3. Supported DSI Video Formats

The THCV353-Q supports four DSI RGB video formats:

· RGB888 (Packed Pixel Stream, 24-bit Format, Data Type 0x3E)

· RGB666 (Loosely Packed Pixel Stream, 18-bit format in Three Bytes, Data Type 0x2E)

· RGB666 (Packed Pixel Stream, 18-bit Format, Data Type 0x1E)

· RGB565 (Packed Pixel Stream, 16-bit Format, Data Type 0x0E)

· YCbCr 4:2:2 16-bit (Packed Pixel Stream, Data Type 0x2C)

Note

Each video line is expected to be sent as a single DSI packet. Multi-packet per line video formats are not supported

The RGB video formats are automatically converted, if necessary, to 3-byte RGB888 for transmission over V-by-One® HS II.

7.3.2. High-Speed Forward Channel Data Transfer

The High-Speed Forward Channel (FC) is composed of 30 bits of data containing RGB data, sync signals, 2-wire interface, GPIOs, and I2S audio transmitted from serializer to deserializer. The serial stream mostly contains RGB data, sync signals and internally calculated CRC information, while once in determined cycle time by FCTHRIO_MODE it contains 2-wire interface, GPIOs and I2S audio. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, balanced and scrambled.

The device supports DSI data-rate in the range of 80 Mbps to 1.5Gbps over one lane, or 5 MHz to 232 MHz Pixel Clock over one or two channels. The V-by-One® HS II serial stream rate is 4 Gbps maximum (1 Gbps minimum).

[DSI.Data-rate.input] = Data-rate input on DSI per lane = [F(DSIin)]
[DSIlaneNum] = DSI input lane number per port channel selected by register setting
[DSI.bpp] = DSI input bit per pixel selected by register setting for Packed Pixel Format
or 24 (when Loosely Packed RGB666 Format)
[PCLK.input] = Pixel clock input on DSI per port = [F(DSIin)] x [DSIlaneNum] / [DSI.bpp]
[DSIportNum] = DSI input port channel number selected by register setting
[PCLK.input.total] = Total Pixel clock input on DSI = [PCLK.input] x [DSIportNum]
[FClaneNum] = V-by-One® HS II Forward Channel output Lane number selected by pin setting
[THRIOrate] = 8/7 (when FCTHRIO_MODE=0 selected by register setting as 8cycle mode)
4/3 (when FCTHRIO_MODE=1 selected by register setting as 4cycle mode)
[LowFreqMode] = x1 or x2 or x4 or x8 selected by register setting
[PCLK.FCout)] = Pixel clock output on Forward Channel (FC) per lane
[Data-rate.FCout)] = Output Data-rate on Forward Channel (FC) per lane
[PCLK.FCout)] = [PCLK.input] x {[DSIportNum] / [FClaneNum]} x [THRIOrate] x [LowFreqMode]
[Data-rate.FCout)] = [PCLK.FCout] x (3 x 8 x 10/8)

7.3.3. Back Channel Data Transfer

The Backward Channel (BC) provides bidirectional communication between the display and host processor. The information is carried from the deserializer to the serializer as serial frames. The back channel control data is transferred over both serial links along with the high-speed forward data with DC balance coding. This architecture provides a backward path across the serial link together with a high-speed forward channel. The back channel contains the 2-wire interface, CRC and GPIO information with 6.7 ~ 26.7 Mbps line rate (configured by the compatible deserializer).

[Data-rate.BCin)] = Input Data-rate on Backward Channel (BC)

[Data-rate.BCin)] = [Data-rate.FCout)] / 150

7.3.4. BCC Port Register Access

The THCV353-Q contains two downstream ports. Two ports are independent each other which requires independent setting transaction.

The THCV353-Q and counterpart compatible deserializer have independent 2-wire slave address respectively. They require independent setting transaction.

7.3.5. Video Control Signals

The video control signal bits embedded in the high-speed MIPI DSI are subject to certain limitations relative to the video pixel clock period (PCLK). By default, the THCV353-Q applies a minimum pulse width filter on these signals to help eliminate spurious transitions.

Normal Mode Control Signals (VS, HS, DE) have the following restrictions:

· Horizontal Sync (HS): The video control signal pulse width must be 4 PCLKs or longer when the Control Signal Filter (register) is enabled. Disabling the Control Signal Filter removes this restriction (minimum is 1 PCLK). As an additional function, HS could be activated to have at most two transitions per 130 PCLKs by register.

· Vertical Sync (VS): The video control signal pulse width must be 4 PCLKs or longer when the Control Signal Filter (register) is enabled. As an additional function, VS could be activated to be limited to 1 transition per 130 PCLKs by register, whose minimum pulse width could be 130 PCLKs. Period from DE High=>Low fall timing to VS activating timing and period from VS inactivating timing to DE Low=>High rise timing must be both at least 1 Line time period of the video frame.

· Data Enable Input (DE): The video control signal pulse width must be 4 PCLKs or longer when the Control Signal Filter (register) is enabled. Disabling the Control Signal Filter removes this restriction (minimum is 1 PCLK). DE could be activated to have at most two transitions per 130 PCLKs by register. DE High maximum time period is 5000PCLKs.

In addition, Sync Control Signals (VS, HS) have the following restrictions related with DE.

In DE=Low blanking period, at the beginning and around at the end of DE=Low, there are several invalid window.

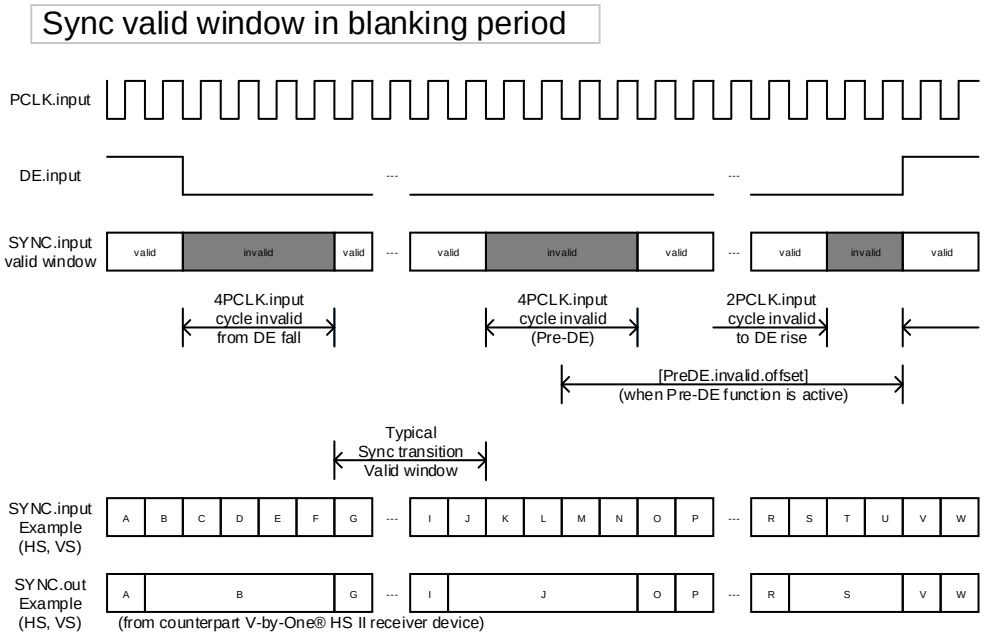


Figure 7. Sync Valid Window in Blanking Period

[PreDE.invalid.offset] = Pre-DE invalid period offset from DE rise (when Pre-DE function is active)

[PreDE.Set] = Pre-DE position set by register PRE_DE_POSITION

[DSIportNum] = DSI input port channel number selected by register setting

[FClaneNum] = V-by-One® HS II Forward Channel output Lane number selected

[THRIOrate] = 8/7 (when FCTHRIO_MODE=0 selected by pin setting as 8cycle mode)

4/3 (when FCTHRIO_MODE=1 selected by pin setting as 4cycle mode)

[LowFreqMode] = x1 or x2 or x4 or x8 selected by register setting

[PreDE.invalid.offset] = [PreDE.set] x {[FClaneNum] / [DSIportNum]} x {1 / [THRIOrate]} x [LowFreqMode]

Sync generation have several alternatives depending on R_SYNCGEN_MODE. Some R_SYNCGEN_MODE have matching response against panel display behavior especially relating Horizontal Back Porch. Trying several R_SYNCGEN_MODE options may help to match display panel behavior.

7.3.5.1. Dummy DE operation

When only clock signal is supplied from source and DE input (active data input with MIPI High-Speed mode) have not yet been supplied, THCV353-Q is able to start BCC communication not with DE input but with utilizing Dummy DE function prepared as register trigger.

Dummy DE internally generates DE signal for BCC communication for mainly GPIO, 2-wire and other control signal bridge.

Video RGB image is usually not be appropriate to display panel; therefore, counterpart receiver OE Output Enable is supposed to be disabled to block further video output transfer.

After proper DE is input from DSI source, Dummy DE function is supposed to be turned off to transfer input RGB data.

Just after turning off Dummy DE function, the very first DE High input from DSI is discarded and is not able to be sent properly. From the next DE High, proper DE started to process properly.

Note : During Dummy DE=High to Low transition, any 2-wire, GPIO and I2S control bridge communication are all unstable and not able to be used. Users must take care of this behavior.

7.3.6. Power Down (PDN)

The Serializer has a PDN input pin to ENABLE or POWER DOWN the device. This pin may be controlled by an external device, or through VDDIO, where VDDIO = 1.71 V to 1.89 V. To save power, disable the link when the display is not needed (PDN = LOW). Ensure that this pin is not driven HIGH before all power supplies have reached final levels. When PDB is driven low, ensure that the pin is driven to 0V for at least 3ms before releasing or driving high. In the case where PDN is pulled up to VDDIO directly, register clock domain reset control after stable frequency (not transitioning) REFCLK input or MIPI DSI clock input may be required (See Power-On-Sequence).

Toggling PDN low will POWER DOWN the device and RESET all control registers to default. During this time, PDN must be held low for a minimum of 3ms before going high again.

7.3.7. Serial Link Fault Detect

The THCV353-Q can detect fault conditions in the FC, BC and BCC interconnect. If a fault condition occurs, the Link Status is detected. The THCV353-Q will detect any of the following conditions:

1. Cable open
2. “+” to “-” short
3. ”+” to GND short
4. ”-” to GND short
5. ”+” to battery short
6. ”-” to battery short
7. Cable is linked incorrectly (DOUT+/DOUT- connections reversed)

Note: The device will detect any of the above conditions, but does not report specifically which one has occurred.

7.3.8. Interrupt Pin (INTN)

The INTN pin is an active low interrupt output pin that acts as an interrupt for various local and remote interrupt conditions. For the remote interrupt condition, the INTN pin works in conjunction with the INTN_IN pin on the deserializer. This interrupt signal, when configured, will propagate from the deserializer to the serializer.

1. On the Serializer, set remote INTN_IN interrupt Enable
2. Deserializer INTN_IN pin is set LOW by some downstream device.
3. Serializer pulls INTN pin LOW. The signal is active LOW, so a LOW indicates an interrupt condition.
4. External controller detects INTB = LOW; to determine interrupt source, read Interrupt source indicator register.
5. The external controller typically must then access the remote device to determine downstream interrupt source and clear the interrupt driving the Deserializer INTN_IN. This would be when the downstream device releases the INTN_IN pin on the Deserializer. The system is now ready to return to step (2) at next falling edge of INTN_IN.
6. A wrote to Interrupt clear will clear the interrupt at the Serializer, releasing INTN.

7.3.9. Remote Interrupt Pin (REM_INTN0 and REM_INTN1)

REM_INTN will mirror the status of INTN_IN pin on the deserializer and does not need to be cleared. If the serializer is not linked to the deserializer, REM_INTN will be high.

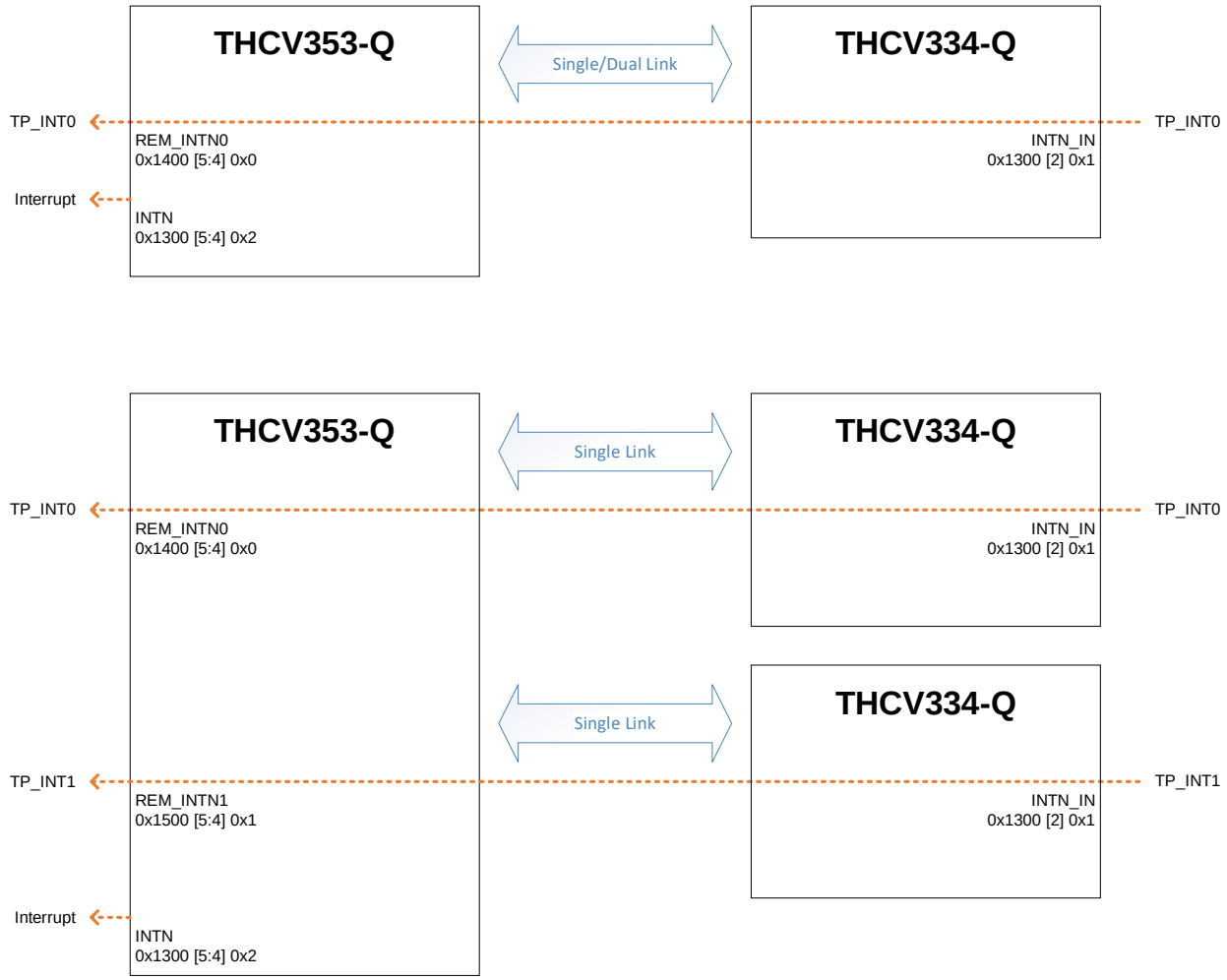


Figure 8. Remote Interrupt Pin

7.3.10. General-Purpose I/O

7.3.10.1. GPIO[3:0] Configuration

In normal operation, GPIO[3:0] may be used as general-purpose IOs in either forward channel (outputs) or back channel (inputs) mode. GPIO modes may be configured from the registers.

7.3.10.2. D_GPIO[3:0] Configuration

In normal operation, D_GPIO[3:0] may be used as general-purpose IOs in either forward channel (outputs) or back channel (inputs) mode. GPIO modes may be configured from the registers.

7.3.10.3. GPIO[8:5] Configuration

GPIO[8:5] are register-only GPIOs and may be programmed as outputs or read as inputs through local register bits only for single FC connection access. Where applicable, these bits are shared with I2S pins and will override I2S input if enabled into GPIO_REG mode.

NOTE: Local GPIO value may be configured and read through local register access.

GPIO[8:5] may be used as general-purpose IOs in either forward channel (outputs) or back channel (inputs) mode. GPIO modes may be configured from the registers for dual FC connection 2nd FC control.

7.3.10.4. GPIO[11/10] Configuration

GPIO[11/10] may be used as general-purpose IOs in either forward channel (outputs) or back channel (inputs) mode. GPIO modes may be configured from the registers for dual FC connection 2nd FC control.

7.3.10.5. Example command of GPIO setting for one deserializer without I2S transport

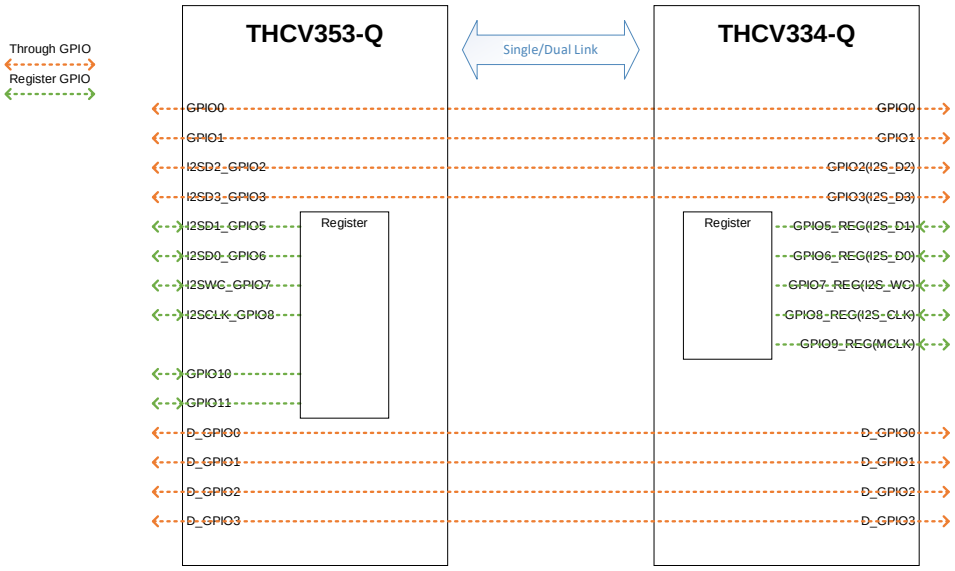


Figure 9. Example GPIO Setting for One Deserializer without I2S Transport

cmd: write devaddr: 0x0B regaddr: 0x0C00 val: 0x03 //353 GPIO0 Through Input
cmd: write devaddr: 0x0B regaddr: 0x0C01 val: 0x03 //353 GPIO1 Through Input
cmd: write devaddr: 0x0B regaddr: 0x0C02 val: 0x03 //353 I2SD2_GPIO2 Through Input
cmd: write devaddr: 0x0B regaddr: 0x0C03 val: 0x03 //353 I2SD3_GPIO3 Through Input
cmd: write devaddr: 0x0B regaddr: 0x0C04 val: 0x09 //353 I2SD1_GPIO5 Register output H
cmd: write devaddr: 0x0B regaddr: 0x0C05 val: 0x09 //353 I2SD0_GPIO6 Register output H
cmd: write devaddr: 0x0B regaddr: 0x0C06 val: 0x09 //353 I2SWC_GPIO7 Register output H
cmd: write devaddr: 0x0B regaddr: 0x0C07 val: 0x09 //353 I2SCLK_GPIO8 Register output H
cmd: write devaddr: 0x0B regaddr: 0x0C80 val: 0x09 //353 GPIO10 Register output H
cmd: write devaddr: 0x0B regaddr: 0x0C81 val: 0x09 //353 GPIO11 Register output H
cmd: write devaddr: 0x0B regaddr: 0x0C08 val: 0x03 //353 D_GPIO0 Through Input
cmd: write devaddr: 0x0B regaddr: 0x0C09 val: 0x03 //353 D_GPIO1 Through Input
cmd: write devaddr: 0x0B regaddr: 0x0C0A val: 0x03 //353 D_GPIO2 Through Input
cmd: write devaddr: 0x0B regaddr: 0x0C0B val: 0x03 //353 D_GPIO3 Through Input
cmd: write devaddr: 0x77 regaddr: 0x0C00 val: 0x05 //334 GPIO0 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C01 val: 0x05 //334 GPIO1 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C02 val: 0x05 //334 GPIO2 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C03 val: 0x05 //334 GPIO3 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C04 val: 0x09 //334 GPIO5_REG Register output H
cmd: write devaddr: 0x77 regaddr: 0x0C05 val: 0x09 //334 GPIO6_REG Register output H
cmd: write devaddr: 0x77 regaddr: 0x0C06 val: 0x09 //334 GPIO7_REG Register output H
cmd: write devaddr: 0x77 regaddr: 0x0C07 val: 0x09 //334 GPIO8_REG Register output H
cmd: write devaddr: 0x77 regaddr: 0x0C0C val: 0x09 //334 GPIO9_REG Register output H
cmd: write devaddr: 0x77 regaddr: 0x0C08 val: 0x05 //334 D_GPIO0 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C09 val: 0x05 //334 D_GPIO1 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C0A val: 0x05 //334 D_GPIO2 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C0B val: 0x05 //334 D_GPIO3 Through Output

7.3.10.6. Example command of GPIO setting for one deserializer with I2S transport

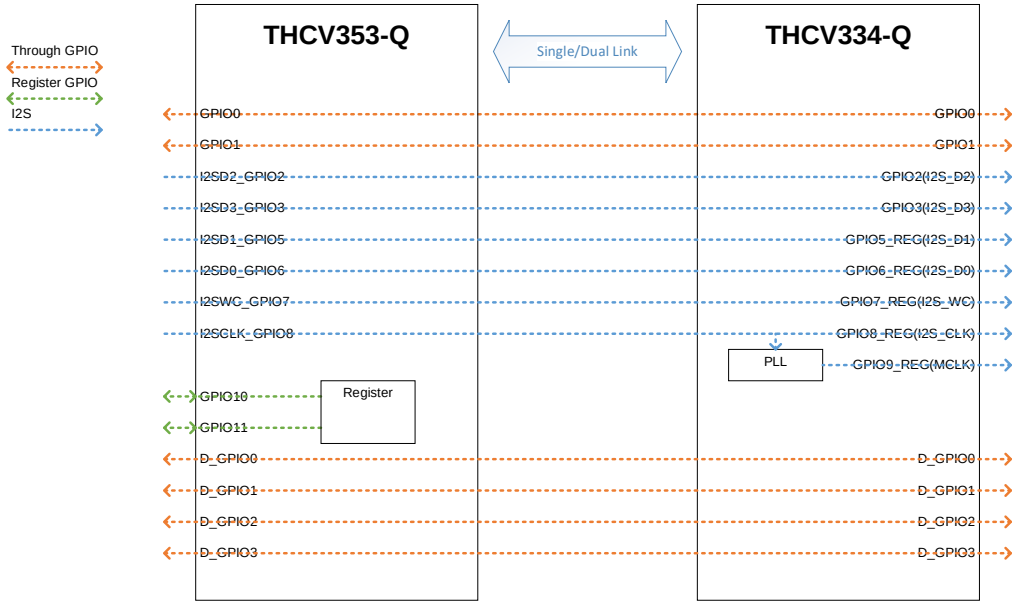


Figure 10. Example GPIO Setting for One Deserializer with I2S Transport

cmd: write devaddr: 0x0B regaddr: 0x0C00 val: 0x03 //353 GPIO0 Through Input
cmd: write devaddr: 0x0B regaddr: 0x0C01 val: 0x03 //353 GPIO1 Through Input
cmd: write devaddr: 0x0B regaddr: 0x0C02 val: 0x00 //353 I2SD2_GPIO2 D2 Input
cmd: write devaddr: 0x0B regaddr: 0x0C03 val: 0x00 //353 I2SD3_GPIO3 D3 Input
cmd: write devaddr: 0x0B regaddr: 0x0C04 val: 0x00 //353 I2SD1_GPIO5 D1 Input
cmd: write devaddr: 0x0B regaddr: 0x0C05 val: 0x00 //353 I2SD0_GPIO6 D0 Input
cmd: write devaddr: 0x0B regaddr: 0x0C06 val: 0x00 //353 I2SWC_GPIO7 WC Input
cmd: write devaddr: 0x0B regaddr: 0x0C07 val: 0x00 //353 I2SCLK_GPIO8 CLK Input
cmd: write devaddr: 0x0B regaddr: 0x0C80 val: 0x09 //353 GPIO10 Register output H
cmd: write devaddr: 0x0B regaddr: 0x0C81 val: 0x09 //353 GPIO11 Register output H
cmd: write devaddr: 0x0B regaddr: 0x0C08 val: 0x03 //353 D_GPIO0 Through Input
cmd: write devaddr: 0x0B regaddr: 0x0C09 val: 0x03 //353 D_GPIO1 Through Input
cmd: write devaddr: 0x0B regaddr: 0x0C0A val: 0x03 //353 D_GPIO2 Through Input
cmd: write devaddr: 0x0B regaddr: 0x0C0B val: 0x03 //353 D_GPIO3 Through Input
cmd: write devaddr: 0x77 regaddr: 0x0C00 val: 0x05 //334 GPIO0 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C01 val: 0x05 //334 GPIO1 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C02 val: 0x00 //334 GPIO2 D2 Output
cmd: write devaddr: 0x77 regaddr: 0x0C03 val: 0x00 //334 GPIO3 D3 Output
cmd: write devaddr: 0x77 regaddr: 0x0C04 val: 0x00 //334 GPIO5_REG D1 output
cmd: write devaddr: 0x77 regaddr: 0x0C05 val: 0x00 //334 GPIO6_REG D0 output
cmd: write devaddr: 0x77 regaddr: 0x0C06 val: 0x00 //334 GPIO7_REG WC output
cmd: write devaddr: 0x77 regaddr: 0x0C07 val: 0x00 //334 GPIO8_REG CLK output
cmd: write devaddr: 0x77 regaddr: 0x0C0C val: 0x00 //334 GPIO9_REG MCLK output
cmd: write devaddr: 0x77 regaddr: 0x0C08 val: 0x05 //334 D_GPIO0 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C09 val: 0x05 //334 D_GPIO1 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C0A val: 0x05 //334 D_GPIO2 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C0B val: 0x05 //334 D_GPIO3 Through Output

7.3.10.7. Example command of GPIO setting for two deserializers without I2S transport

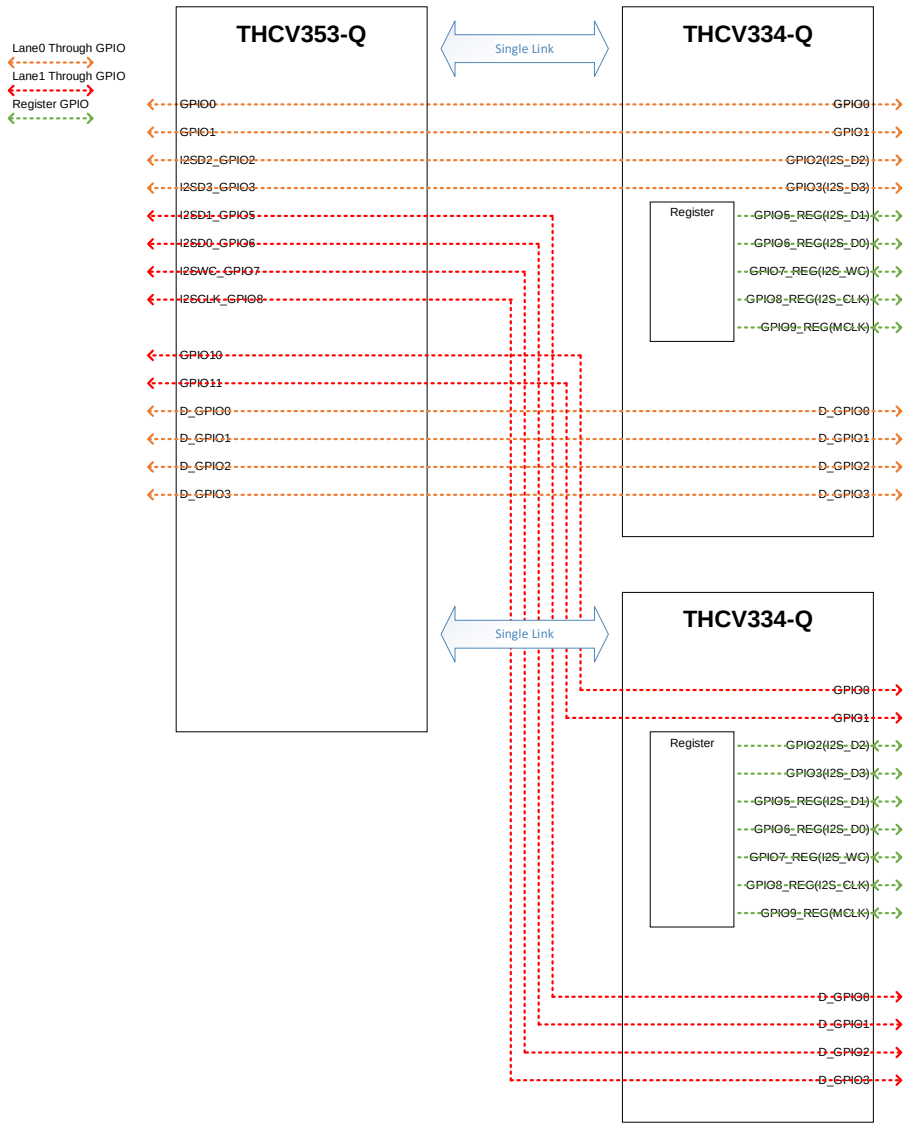


Figure 11. Example GPIO Setting for Two Deserializer without I2S Transport

cmd: write devaddr: 0x0B regaddr: 0x0C00 val: 0x03 //353 GPIO0 Through Input to Lane0
cmd: write devaddr: 0x0B regaddr: 0x0C01 val: 0x03 //353 GPIO1 Through Input to Lane0
cmd: write devaddr: 0x0B regaddr: 0x0C02 val: 0x03 //353 I2SD2_GPIO2 Through Input to Lane0
cmd: write devaddr: 0x0B regaddr: 0x0C03 val: 0x03 //353 I2SD3_GPIO3 Through Input to Lane0
cmd: write devaddr: 0x0B regaddr: 0x0C88 val: 0x03 //353 I2SD1_GPIO5 Through Input to Lane1 D_GPIO0
cmd: write devaddr: 0x0B regaddr: 0x0C89 val: 0x03 //353 I2SD0_GPIO6 Through Input to Lane1 D_GPIO1
cmd: write devaddr: 0x0B regaddr: 0x0C8A val: 0x03 //353 I2SWC_GPIO7 Through Input to Lane1 D_GPIO2
cmd: write devaddr: 0x0B regaddr: 0x0C8B val: 0x03 //353 I2SCLK_GPIO8 Through Input to Lane1 D_GPIO3
cmd: write devaddr: 0x0B regaddr: 0x0C80 val: 0x03 //353 GPIO10 Through Input to Lane1 GPIO0
cmd: write devaddr: 0x0B regaddr: 0x0C81 val: 0x03 //353 GPIO11 Through Input to Lane1 GPIO1
cmd: write devaddr: 0x0B regaddr: 0x0C08 val: 0x03 //353 D_GPIO0 Through Input Lane0
cmd: write devaddr: 0x0B regaddr: 0x0C09 val: 0x03 //353 D_GPIO1 Through Input Lane0
cmd: write devaddr: 0x0B regaddr: 0x0C0A val: 0x03 //353 D_GPIO2 Through Input Lane0
cmd: write devaddr: 0x0B regaddr: 0x0C0B val: 0x03 //353 D_GPIO3 Through Input Lane0
cmd: write devaddr: 0x77 regaddr: 0x0C00 val: 0x05 //Lane0 334 GPIO0 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C01 val: 0x05 //Lane0 334 GPIO1 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C02 val: 0x05 //Lane0 334 GPIO2 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C03 val: 0x05 //Lane0 334 GPIO3 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C04 val: 0x09 //Lane0 334 GPIO5_REG Register output H
cmd: write devaddr: 0x77 regaddr: 0x0C05 val: 0x09 //Lane0 334 GPIO6_REG Register output H
cmd: write devaddr: 0x77 regaddr: 0x0C06 val: 0x09 //Lane0 334 GPIO7_REG Register output H
cmd: write devaddr: 0x77 regaddr: 0x0C07 val: 0x09 //Lane0 334 GPIO8_REG Register output H
cmd: write devaddr: 0x77 regaddr: 0x0C0C val: 0x09 //Lane0 334 GPIO9_REG Register output H
cmd: write devaddr: 0x77 regaddr: 0x0C08 val: 0x05 //Lane0 334 D_GPIO0 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C09 val: 0x05 //Lane0 334 D_GPIO1 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C0A val: 0x05 //Lane0 334 D_GPIO2 Through Output
cmd: write devaddr: 0x77 regaddr: 0x0C0B val: 0x05 //Lane0 334 D_GPIO3 Through Output
cmd: write devaddr: 0x65 regaddr: 0x0C00 val: 0x05 //Lane1 334 GPIO0 Through Output
cmd: write devaddr: 0x65 regaddr: 0x0C01 val: 0x05 //Lane1 334 GPIO1 Through Output
cmd: write devaddr: 0x65 regaddr: 0x0C02 val: 0x09 //Lane1 334 GPIO2 Register output H
cmd: write devaddr: 0x65 regaddr: 0x0C03 val: 0x09 //Lane1 334 GPIO3 Register output H
cmd: write devaddr: 0x65 regaddr: 0x0C04 val: 0x09 //Lane1 334 GPIO5_REG Register output H
cmd: write devaddr: 0x65 regaddr: 0x0C05 val: 0x09 //Lane1 334 GPIO6_REG Register output H
cmd: write devaddr: 0x65 regaddr: 0x0C06 val: 0x09 //Lane1 334 GPIO7_REG Register output H
cmd: write devaddr: 0x65 regaddr: 0x0C07 val: 0x09 //Lane1 334 GPIO8_REG Register output H
cmd: write devaddr: 0x65 regaddr: 0x0C0C val: 0x09 //Lane1 334 GPIO9_REG Register output H
cmd: write devaddr: 0x65 regaddr: 0x0C08 val: 0x05 //Lane1 334 D_GPIO0 Through Output
cmd: write devaddr: 0x65 regaddr: 0x0C09 val: 0x05 //Lane1 334 D_GPIO1 Through Output
cmd: write devaddr: 0x65 regaddr: 0x0C0A val: 0x05 //Lane1 334 D_GPIO2 Through Output
cmd: write devaddr: 0x65 regaddr: 0x0C0B val: 0x05 //Lane1 334 D_GPIO3 Through Output

7.3.10.8. Example command of GPIO setting for two deserializers with distribution I2S transport

Active Operation mode;

MODE_REG (0x0100[3:0]): 0x0, Distribution output enable

MODE_REG (0x0100[3:0]): 0x2

MODE_REG (0x0100[3:0]): 0x5

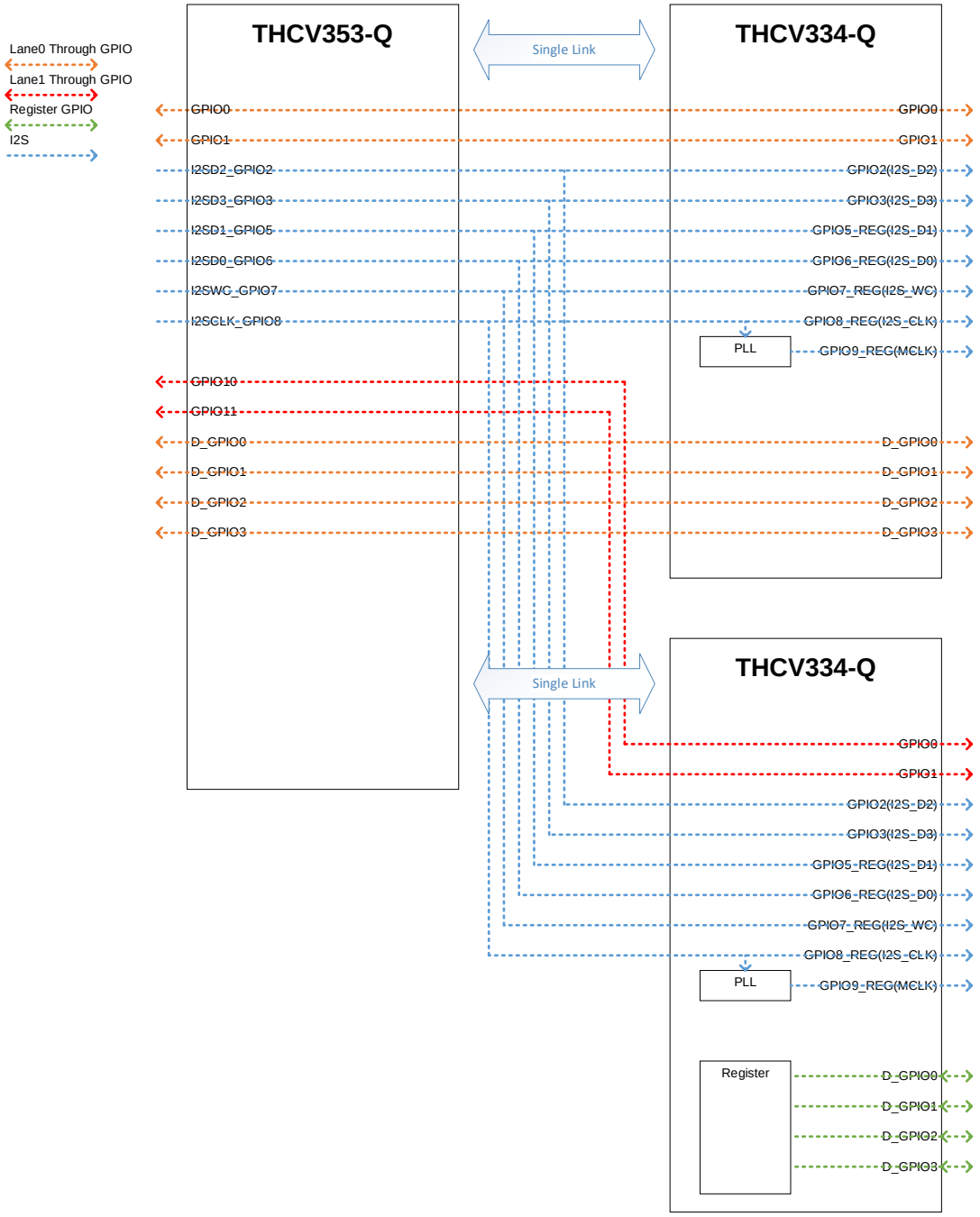


Figure 12. Example GPIO Setting for Two Deserializer with distribution I2S Transport

```
cmd: write   devaddr: 0x0B   regaddr: 0x0C00 val: 0x03 //353 GPIO0 Through Input to Lane0
cmd: write   devaddr: 0x0B   regaddr: 0x0C01 val: 0x03 //353 GPIO1 Through Input to Lane0
cmd: write   devaddr: 0x0B   regaddr: 0x0C02 val: 0x00 //353 I2SD2_GPIO2 D2 Input to Lane0/1
cmd: write   devaddr: 0x0B   regaddr: 0x0C03 val: 0x00 //353 I2SD3_GPIO3 D3 Input to Lane0/1
cmd: write   devaddr: 0x0B   regaddr: 0x0C04 val: 0x00 //353 I2SD1_GPIO5 D1 Input to Lane0/1
cmd: write   devaddr: 0x0B   regaddr: 0x0C05 val: 0x00 //353 I2SD0_GPIO6 D0 Input to Lane0/1
cmd: write   devaddr: 0x0B   regaddr: 0x0C06 val: 0x00 //353 I2SWC_GPIO7 WC Input to Lane0/1
cmd: write   devaddr: 0x0B   regaddr: 0x0C07 val: 0x00 //353 I2SWC_GPIO8 CLK Input to Lane0/1
cmd: write   devaddr: 0x0B   regaddr: 0x0C80 val: 0x03 //353 GPIO10 Through Input to Lane1 GPIO0
cmd: write   devaddr: 0x0B   regaddr: 0x0C81 val: 0x03 //353 GPIO11 Through Input to Lane1 GPIO1
cmd: write   devaddr: 0x0B   regaddr: 0x0C08 val: 0x03 //353 D_GPIO0 Through Input to lane0
cmd: write   devaddr: 0x0B   regaddr: 0x0C09 val: 0x03 //353 D_GPIO0 Through Input to lane0
cmd: write   devaddr: 0x0B   regaddr: 0x0C0A val: 0x03 //353 D_GPIO0 Through Input to lane0
cmd: write   devaddr: 0x0B   regaddr: 0x0C0B val: 0x03 //353 D_GPIO0 Through Input to lane0
cmd: write   devaddr: 0x77   regaddr: 0x0C00 val: 0x05 //Lane0 334 GPIO0 Through Output
cmd: write   devaddr: 0x77   regaddr: 0x0C01 val: 0x05 //Lane0 334 GPIO1 Through Output
cmd: write   devaddr: 0x77   regaddr: 0x0C02 val: 0x00 //Lane0 334 GPIO2 D2 Output
cmd: write   devaddr: 0x77   regaddr: 0x0C03 val: 0x00 //Lane0 334 GPIO3 D3 Output
cmd: write   devaddr: 0x77   regaddr: 0x0C04 val: 0x00 //Lane0 334 GPIO5_REG D1 output
cmd: write   devaddr: 0x77   regaddr: 0x0C05 val: 0x00 //Lane0 334 GPIO6_REG D0 output
cmd: write   devaddr: 0x77   regaddr: 0x0C06 val: 0x00 //Lane0 334 GPIO7_REG WC output
cmd: write   devaddr: 0x77   regaddr: 0x0C07 val: 0x00 //Lane0 334 GPIO8_REG CLK output
cmd: write   devaddr: 0x77   regaddr: 0x0C0C val: 0x00 //Lane0 334 GPIO9_REG MCLK output
cmd: write   devaddr: 0x77   regaddr: 0x0C08 val: 0x05 //Lane0 334 D_GPIO0 Through Output
cmd: write   devaddr: 0x77   regaddr: 0x0C09 val: 0x05 //Lane0 334 D_GPIO0 Through Output
cmd: write   devaddr: 0x77   regaddr: 0x0C0A val: 0x05 //Lane0 334 D_GPIO0 Through Output
cmd: write   devaddr: 0x77   regaddr: 0x0C0B val: 0x05 //Lane0 334 D_GPIO0 Through Output
cmd: write   devaddr: 0x65   regaddr: 0x0C00 val: 0x05 //Lane1 334 GPIO0 Through Output
cmd: write   devaddr: 0x65   regaddr: 0x0C01 val: 0x05 //Lane1 334 GPIO1 Through Output
cmd: write   devaddr: 0x65   regaddr: 0x0C02 val: 0x00 //Lane1 334 GPIO2 D2 Output
cmd: write   devaddr: 0x65   regaddr: 0x0C03 val: 0x00 //Lane1 334 GPIO3 D3 Output
cmd: write   devaddr: 0x65   regaddr: 0x0C04 val: 0x00 //Lane1 334 GPIO5_REG D1 output
cmd: write   devaddr: 0x65   regaddr: 0x0C05 val: 0x00 //Lane1 334 GPIO6_REG D0 output
cmd: write   devaddr: 0x65   regaddr: 0x0C06 val: 0x00 //Lane1 334 GPIO7_REG WC output
cmd: write   devaddr: 0x65   regaddr: 0x0C07 val: 0x00 //Lane1 334 GPIO8_REG CLK output
cmd: write   devaddr: 0x65   regaddr: 0x0C0C val: 0x00 //Lane1 334 GPIO9_REG MCLK output
cmd: write   devaddr: 0x65   regaddr: 0x0C08 val: 0x09 //Lane1 334 D_GPIO0 Register Output H
cmd: write   devaddr: 0x65   regaddr: 0x0C09 val: 0x09 //Lane1 334 D_GPIO0 Register Output H
cmd: write   devaddr: 0x65   regaddr: 0x0C0A val: 0x09 //Lane1 334 D_GPIO0 Register Output H
cmd: write   devaddr: 0x65   regaddr: 0x0C0B val: 0x09 //Lane1 334 D_GPIO0 Register Output H
```

7.3.10.9. Example command of GPIO setting for two deserializers with Asynchronous I2S transport

Active Operation mode;

MODE_REG (0x0100[3:0]): 0x6

MODE_REG (0x0100[3:0]): 0xC

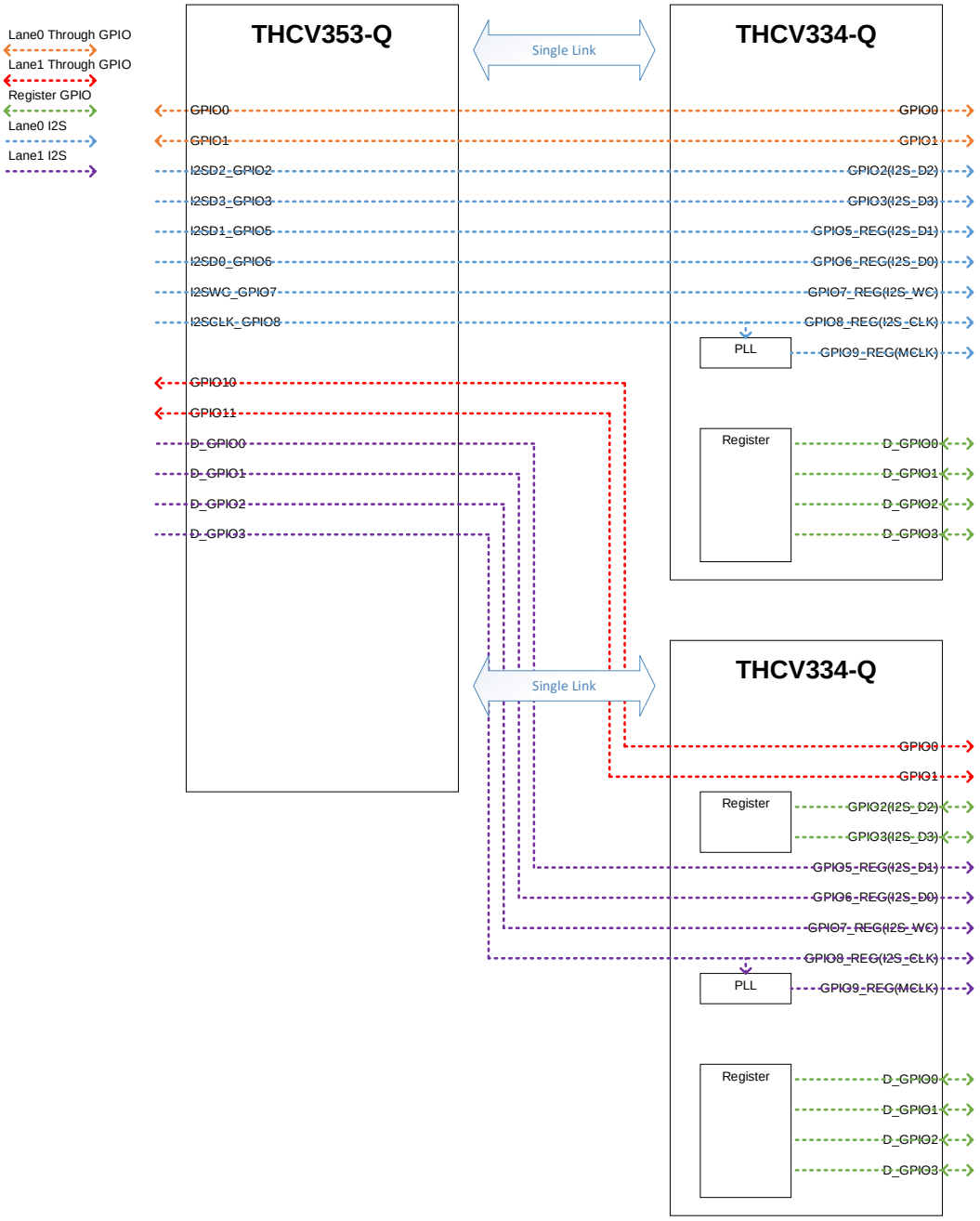


Figure 13. Example GPIO Setting for Two Deserializer with Asynchronous I2S Transport

```
cmd: write   devaddr: 0x0B   regaddr: 0x0C00 val: 0x03 //353 GPIO0 Through Input to Lane0
cmd: write   devaddr: 0x0B   regaddr: 0x0C01 val: 0x03 //353 GPIO1 Through Input to Lane0
cmd: write   devaddr: 0x0B   regaddr: 0x0C02 val: 0x00 //353 I2SD2_GPIO2 D2 Input to Lane0
cmd: write   devaddr: 0x0B   regaddr: 0x0C03 val: 0x00 //353 I2SD3_GPIO3 D3 Input to Lane0
cmd: write   devaddr: 0x0B   regaddr: 0x0C04 val: 0x00 //353 I2SD1_GPIO5 D1 Input to Lane0
cmd: write   devaddr: 0x0B   regaddr: 0x0C05 val: 0x00 //353 I2SD0_GPIO6 D0 Input to Lane0
cmd: write   devaddr: 0x0B   regaddr: 0x0C06 val: 0x00 //353 I2SWC_GPIO7 WC Input to Lane0
cmd: write   devaddr: 0x0B   regaddr: 0x0C07 val: 0x00 //353 I2SWC_GPIO8 CLK Input to Lane0
cmd: write   devaddr: 0x0B   regaddr: 0x0C80 val: 0x03 //353 GPIO10 Through Input to Lane1 GPIO0
cmd: write   devaddr: 0x0B   regaddr: 0x0C81 val: 0x03 //353 GPIO11 Through Input to Lane1 GPIO1
cmd: write   devaddr: 0x0B   regaddr: 0x0C84 val: 0x03 //353 D_GPIO0 I2S_D1 Input to Lane1
cmd: write   devaddr: 0x0B   regaddr: 0x0C85 val: 0x03 //353 D_GPIO0 I2S_D0 Input to Lane1
cmd: write   devaddr: 0x0B   regaddr: 0x0C86 val: 0x03 //353 D_GPIO0 I2S_WC Input to Lane1
cmd: write   devaddr: 0x0B   regaddr: 0x0C87 val: 0x03 //353 D_GPIO0 I2S_CLK Input to Lane1
cmd: write   devaddr: 0x77   regaddr: 0x0C00 val: 0x05 //Lane0 334 GPIO0 Through Output
cmd: write   devaddr: 0x77   regaddr: 0x0C01 val: 0x05 //Lane0 334 GPIO1 Through Output
cmd: write   devaddr: 0x77   regaddr: 0x0C02 val: 0x00 //Lane0 334 GPIO2 D2 Output
cmd: write   devaddr: 0x77   regaddr: 0x0C03 val: 0x00 //Lane0 334 GPIO3 D3 Output
cmd: write   devaddr: 0x77   regaddr: 0x0C04 val: 0x00 //Lane0 334 GPIO5_REG D1 output
cmd: write   devaddr: 0x77   regaddr: 0x0C05 val: 0x00 //Lane0 334 GPIO6_REG D0 output
cmd: write   devaddr: 0x77   regaddr: 0x0C06 val: 0x00 //Lane0 334 GPIO7_REG WC output
cmd: write   devaddr: 0x77   regaddr: 0x0C07 val: 0x00 //Lane0 334 GPIO8_REG CLK output
cmd: write   devaddr: 0x77   regaddr: 0x0C0C val: 0x00 //Lane0 334 GPIO9_REG MCLK output
cmd: write   devaddr: 0x77   regaddr: 0x0C08 val: 0x09 //Lane0 334 D_GPIO0 Register Output H
cmd: write   devaddr: 0x77   regaddr: 0x0C09 val: 0x09 //Lane0 334 D_GPIO0 Register Output H
cmd: write   devaddr: 0x77   regaddr: 0x0C0A val: 0x09 //Lane0 334 D_GPIO0 Register Output H
cmd: write   devaddr: 0x77   regaddr: 0x0C0B val: 0x09 //Lane0 334 D_GPIO0 Register Output H
cmd: write   devaddr: 0x65   regaddr: 0x0C00 val: 0x05 //Lane1 334 GPIO0 Through Output
cmd: write   devaddr: 0x65   regaddr: 0x0C01 val: 0x05 //Lane1 334 GPIO1 Through Output
cmd: write   devaddr: 0x65   regaddr: 0x0C02 val: 0x09 //Lane1 334 GPIO2 Register Output H
cmd: write   devaddr: 0x65   regaddr: 0x0C03 val: 0x09 //Lane1 334 GPIO3 Register Output H
cmd: write   devaddr: 0x65   regaddr: 0x0C04 val: 0x00 //Lane1 334 GPIO5_REG D1 output
cmd: write   devaddr: 0x65   regaddr: 0x0C05 val: 0x00 //Lane1 334 GPIO6_REG D0 output
cmd: write   devaddr: 0x65   regaddr: 0x0C06 val: 0x00 //Lane1 334 GPIO7_REG WC output
cmd: write   devaddr: 0x65   regaddr: 0x0C07 val: 0x00 //Lane1 334 GPIO8_REG CLK output
cmd: write   devaddr: 0x65   regaddr: 0x0C0C val: 0x00 //Lane1 334 GPIO9_REG MCLK output
cmd: write   devaddr: 0x65   regaddr: 0x0C08 val: 0x09 //Lane1 334 D_GPIO0 Register Output H
cmd: write   devaddr: 0x65   regaddr: 0x0C09 val: 0x09 //Lane1 334 D_GPIO0 Register Output H
cmd: write   devaddr: 0x65   regaddr: 0x0C0A val: 0x09 //Lane1 334 D_GPIO0 Register Output H
cmd: write   devaddr: 0x65   regaddr: 0x0C0B val: 0x09 //Lane1 334 D_GPIO0 Register Output H
```

7.3.11. General Protocol Communication

7.3.11.1. SPI Communication

SPI Communication can be configured by utilizing GPIO function.

SPI data rates are not symmetrical for the two modes of operation. Data over the forward channel can be sent much faster than data over the reverse channel. The SPI Control Channel can operate in a high-speed when writing data only by FC, but must operate at lower frequencies when reading data by FC, BC, and BCC.

NOTE: SPI cannot be used to access Serializer / Deserializer registers.

Original intended pin assignments are as follows;

43:SS

44:SCLK

45:MISO

46:MOSI

Especially MISO Master Input Slave Output pin is supposed to be assigned right to read data .

7.3.11.2. UART Communication

UART Communication can be configured by utilizing GPIO function.

7.3.11.3. PWM Bridge

PWM Bridge can be configured by utilizing GPIO function. Data over the forward channel can be sent much faster than data over the reverse channel.

7.3.12. Family Compatibility

This V-by-One® HS II serializer is not backward compatible to the THCV23x nor THCV24x series with the Backward Channel operation.

Part of only Forward Channel operation are backward compatible to the THCV23x nor THCV24x series.

7.3.13. Audio Modes

7.3.13.1. I2S Audio Interface

The THCV353-Q serializer features six I2S input pins that, when paired with a compatible deserializer, supports 7.1 High-Definition (HD) Surround Sound audio applications. The bit clock (I2S_CLK) supports frequencies restricted by FC PCLK. Four I2S data inputs transport two channels of I2S-formatted digital audio each, with each channel delineated by the word select (I2S_WC) input.

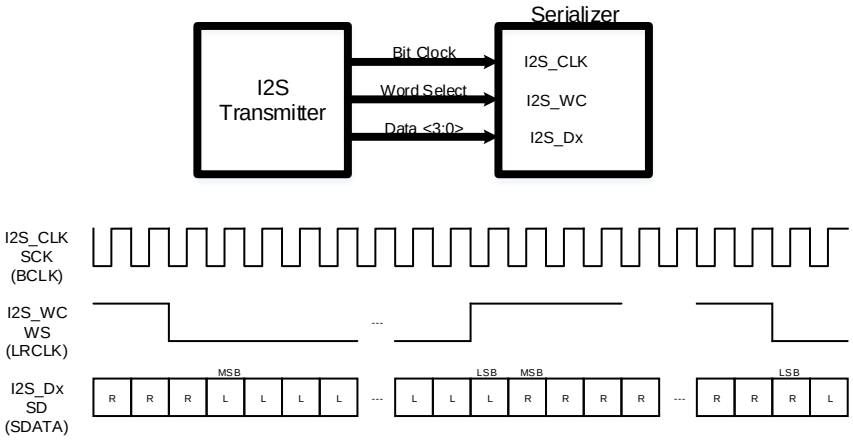


Figure 14. I2S Audio

Table 20. Audio Interface Frequencies

SAMPLE RATE (kHz)	I2S DATA WORD SIZE (bits)	I2S CLK (MHz)
32	16	1.024
44.1	16	1.411
48	16	1.536
96	16	3.072
32	24	1.536
44.1	24	2.117
48	24	2.304
32	32	2.048
44.1	32	2.822
48	32	3.072

7.3.14. Data Transfer Speed

Table 21. Data Transfer Speed

Symbol	Parameter	Condition	formula	unit
fSMPL_A2FC	Digitize Sampling Rate Audio from I2S_CLK, I2S_WC and I2S_D[3:0] to FC	x=FCTHRIO_MODE =4or8 (cycle)	fSMPL_A2FC =1/[{x/8}*8*(30*TTFCBIT)]	(sample /second)
fSMPL _GPI2FC	Digitize Sampling Rate Through GPIO from GPI to FC	x=FCTHRIO_MODE =4or8 (cycle) y=register.I2SGPIO.SMP_NUM=4or8 (active GPIOs)	fSMPL_GPI2FC =1/[{(x*y)/8}*(30*TTFCBIT)]	(sample /second)

7.3.15. Link Status Monitor

The THCV353-Q serializer have several Link Status Monitor functions like below.

2-wire interface unique ID

MIPI DSI Rx monitor (including CRC, which is only available with specially prepared counterpart Tx)

Bi-directional Control Channel remote status monitor

Backward Channel status monitor (including CRC)

7.3.16. Internal Pattern Generation

The THCV353-Q serializer provides an internal pattern generation feature. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode but with clock input, the test pattern will be displayed even if no data input is applied.

7.3.17. Internal Status Monitoring output

Internal status signal can be monitored as external MON0/MON1 pin output by register setting.

7.3.18. Output Spread Spectrum

Spread Spectrum Clock Generation (SSCG) modulation is available to apply on FC output.

SSCG modulated input and internal additional SSCG modulation are not available at the same time.

$$[PCLK.FCout]|_{no\ SSCG} \times \frac{(100 - |[R\_SPREAD]|)}{100} < [PCLK.FCout]|_{SSCG.CenterSpread} < [PCLK.FCout]|_{no\ SSCG} \times \frac{(100 + |[R\_SPREAD]|)}{100}$$

$$[PCLK.FCout]|_{no\ SSCG} \times \frac{(100 - |[R\_SPREAD]|)}{100} < [PCLK.FCout]|_{SSCG.DownSpread} < [PCLK.FCout]|_{no\ SSCG}$$

7.3.19. IO digital filter

Digital filters are prepared for IOs. GPIO digital filter can be arranged by register setting. SCL, SDA, and PDN, several VDDIO CMOS Input (Low speed) pins have also prepared digital filters with fixed tOSC x8 cycle filter setting behavior.

7.3.20. PLL manual operation

For typical continuous MIPI DSI clock driven operation, PLL manual setting is not required.

When [PCLK.input] is below 25MHz or non-continuous MIPI DSI clock operation, PLL manual setting is required.

For PLL manual setting and reference clock change setting, PLL_SPD is supposed to be set 1 (PLL Power down) from default value 0 before PLL manual parameters setting, operation mode setting, and reference clock change setting.

Re-activation (PLL_SP=0, PLL power on) and normal operation must be follow these settings afterword.

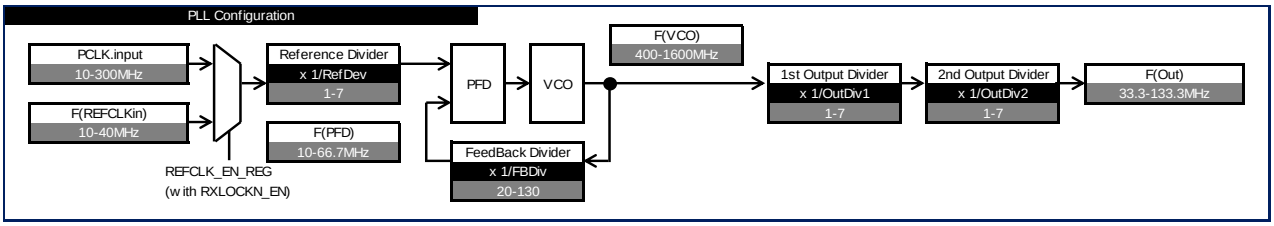


Figure 15. PLL manual control

PLL settings must be selected proper to meet below constraints.

Table 22. PLL constraints table

symbol	discription	condition	min	typ	max	unit
PCLK.input	Pixel clock input frequency on DSI per port	-	10	-	300	MHz
F(REFCLKin)	REFCLK input frequency	-	10	-	40	MHz
RefDiv	Reference Divider value	-	1	-	7	-
FBDiv	FeedBack Divider value	-	20	-	130	-
OutDiv1	1st Output Divider value (OutDiv1 must be >= OutDiv2)	-	1	-	7	-
OutDiv2	2nd Output Divider value (OutDiv1 must be >= OutDiv2)	-	1	-	7	-
F(PFD)	PFD frequency	-	10	-	66.7	MHz
F(VCO)	VCO frequency	-	400	-	1600	MHz
F(OUT)	PLL output pixel clock frequency	-	33.3	-	133.3	MHz

Pixel clock frequency made by PLL is calculated as below.

[PCLK.FCout] = Pixel clock output on Forward Channel (FC) per lane = [F(OUT)]

$$[F(PFD)] = \frac{[PCLK.input]}{[RefDiv]} \text{ or } \frac{[F(REFCLKin)]}{[RefDiv]}$$

$$[F(VCO)] = \frac{[PCLK.input] \times [FBDiv]}{[RefDiv]} \text{ or } \frac{[F(REFCLKin)] \times [FBDiv]}{[RefDiv]}$$

$$[PCLK.FCout] = [F(OUT)] = \frac{[PCLK.input] \times [FBDiv]}{[RefDiv] \times [OutDiv1] \times [OutDiv2]} \text{ or } \frac{[F(REFCLKin)] \times [FBDiv]}{[RefDiv] \times [OutDiv1] \times [OutDiv2]}$$

The registers which must be changed during PLL_SPD=1 (PLL Power down) are summarized as below.

MODEREG（0x0100)
REFCLK_EN_REG（0x0108）
LINK_NUM
FPLL0_REFDIV (0x0291)
FPLL0_INTIN (0x0292, 0x0293)
FPLL0_FRACIN (0x0294, 0x0295, 0x0296)
FPLL0_POSTDIV1 (0x0297)
FPLL0_POSTDIV2 (0x0297)
FPLL0_DIRECTMODE (0x0298)
FPLL0_DIVVAL (0x02B0)
FPLL0_SPREAD (0x02B1)
FPLL0_DOWNSPREAD (0x02B2)
FPLL0_DISABLE_SSCG (0x02B3)
FPLL1_REFDIV (0x02A1)
FPLL1_INTIN (0x02A2, 0x02A3)
FPLL1_FRACIN (0x02A4, 0x02A5, 0x02A6)
FPLL1_POSTDIV1 (0x02A7)
FPLL1_POSTDIV2 (0x02A7)
FPLL1_DIRECTMODE (0x02A8)
FPLL1_DIVVAL (0x02C0)
FPLL1_SPREAD (0x02C1)
FPLL1_DOWNSPREAD (0x02C2)
FPLL1_DISABLE_SSCG (0x02C3)
INFORMAT_SEL0_REG (0x011A)
RXLANESEL0_REG (0x0109)
FPLL0_OLANE (0x0105)
FCTHRIO_MODE0 (0x0101)
DUPLICATED0_REG (0x0104)
INFORMAT_SEL1_REG (0x011A)
RXLANESEL1_REG (0x010A)
FPLL1_OLANE (0x0106)
FCTHRIO_MODE1 (0x0102)
DUPLICATED1_REG (0x0104)

7.3.21. Internal Oscillator Clock operation mode

To link up with the Deserializer to enable the control signal when DSI clock or REFCLK are not inputted, the THCV353-Q Internal Oscillator can be used to link up. The PATGEN function is used because DE is needed to synchronize the control signals. Since the PATGEN signal is output from the Deserializer, it is recommended that the Deserilizer output be set to disable. After the video signal is input, this function should be set to disable.

For reference clock change setting, PLL_SPD is supposed to be set 1 (PLL Power down) from default value 0 before PLL manual parameters setting, operation mode setting, and reference clock change setting.
Re-activation (PLL_SP=0, PLL power on) and normal operation must be follow these settings afterword.

// Internal Oscillator Clock operation enable
cmd: write devaddr: 0x0B regaddr: 0x0640 val: 0x01 // PTGEN enable
cmd: write devaddr: 0x0B regaddr: 0x0103 val: 0x10 // V-by-One® HS output enable override
cmd: write devaddr: 0x0B regaddr: 0x1C15 val: 0x04 // Internal Oscillator Clock enable
cmd: write devaddr: 0x0B regaddr: 0x0108 val: 0x01 // Internal Oscillator Clock REFCLK mode enable

// Internal Oscillator Clock operation disable
cmd: write devaddr: 0x0B regaddr: 0x0640 val: 0x00 // PTGEN Disable
cmd: write devaddr: 0x0B regaddr: 0x1C15 val: 0x00 // Internal Oscillator Clock disable
cmd: write devaddr: 0x0B regaddr: 0x0108 val: 0x00 // Internal Oscillator Clock REFCLK mode disable

7.3.22. Color Space Conversion

The THCV353-Q can convert RGB888 to YUV422.
Color space conversion coefficients are compliant with ITU-R BT.601.

7.4. Device Functional Modes

7.4.1. Mode Select Configuration in Pin Entry

Configuration of the device may be done via MODE0 (REM_INTN1_MODE0), MODE1 (BCMONN_MODE1) and RXLANE (REM_INT0_RXLANE) input pins.

Pin Entry setting of Dual Asynchronous MIPI DSI input / Dual V-by-One®HSII output is prohibited to change mode of operation and RXLANE_EN by register control. If any mode of operation and RXLANE_EN change by register control is required, Pin Entry setting must be other setting.

RXLANE0SEL(0x0109) and RXLANE1SEL(0x010A) setting of MIPI DSI must be previously set before MODE_REG_OVERRIDE(0x0100 [4])=1 Enable activation.

For only single MIPI DSI input mode of operation, MIPI DSI setting RXLANESEL_OVERRIDE_P1(0x010A[4]) must be set to 0x0 from default value 0x1.

Table 23. Mode Select Configuration in Pin Entry

INDEX	BCMONN_MODE1	REM_INTN1_MODE0	REM_INTN0_RXLANE	MIPI DSI lane	Operation mode
1	L	L	L	4lane	Single MIPI DSI Input / Single V-by-One®HSII Output
	L	L	H	2lane	
2	L	H	L	4lane	Single MIPI DSI input / Dual Odd/Even V-by-One® HSII output
	L	H	H	2lane	
3	H	L	L	4lane	Single MIPI DSI input / Dual Left/Right Splitting V-by-One®HSII output
	H	L	H	2lane	
4	H	H	L	4lane	Dual Asynchronous MIPI DSI input / Dual V-by-One®HSII output (Restriction of no mode and DSI lane setting change by register)
	H	H	H	2lane	

Common setting;

FCTHRIO_MODE=8cyble, Low Frequency mode disable, RGB888 format, Distribution mode disable

7.4.2. V-by-One® HS II Modes of Operation

The V-by-One® HS II transmit logic supports several modes of operation, dependent on the downstream receiver as well as the video being delivered.

For operation mode setting, PLL_SPD is supposed to be set 1 (PLL Power down) from default value 0 before PLL manual parameters setting, operation mode setting, and reference clock change setting.
Re-activation (PLL_SP=0, PLL power on) and normal operation must be follow these settings afterword.

Pin Entry setting of Dual Asynchronous MIPI DSI input / Dual V-by-One®HSII output is prohibited to change mode of operation and RXLANE_EN by register control. If any mode of operation and RXLANE_EN change by register control is required, Pin Entry setting must be other setting.

For operation mode setting, MODE_REG(0x0100), and REFCLK_EN_REG(0x0108) change, clock logic software reset is always required after mode setting change. The 1st procedure is MODE_REG change. The 2nd procedure is FREF clock software reset, (0x0014/0x0054 0x08 write). The 3rd procedure is FCRX clock software reset(0x0010/0x0050 0x01 write). Of course those 1st to 3rd procedure should be held during PLL_SPD=1 (PLL Power down).

For particular mode may require R_READ_DELAY arrangement from default value. For example, Left/Right splitting and cropping mode of 1080p may be required to change R_READ_DELAY1 to 0d800 from default value 0d100. For example, aggregation mode of two 1920x720 may be required to change R_READ_DELAY0 to 0d16 from default value 0d100. For example, Left/Right splitting mode of 2160p with SYNCGEN_MODE=0x1 may be required to change R_READ_DELAY0 to 0d32 from default value 0d100.

The registers which must be changed during PLL_SPD=1 (PLL Power down) are summarized as below.

MODEREG（0x0100)
REFCLK_EN_REG（0x0108）
LINK_NUM
FPLL0_REFDIV (0x0291)
FPLL0_INTIN (0x0292, 0x0293)
FPLL0_FRACIN (0x0294, 0x0295, 0x0296)
FPLL0_POSTDIV1 (0x0297)
FPLL0_POSTDIV2 (0x0297)
FPLL0_DIRECTMODE (0x0298)
FPLL0_DIVVAL (0x02B0)
FPLL0_SPREAD (0x02B1)
FPLL0_DOWNSPREAD (0x02B2)
FPLL0_DISABLE_SSCG (0x02B3)
FPLL1_REFDIV (0x02A1)
FPLL1_INTIN (0x02A2, 0x02A3)
FPLL1_FRACIN (0x02A4, 0x02A5, 0x02A6)
FPLL1_POSTDIV1 (0x02A7)
FPLL1_POSTDIV2 (0x02A7)
FPLL1_DIRECTMODE (0x02A8)
FPLL1_DIVVAL (0x02C0)
FPLL1_SPREAD (0x02C1)
FPLL1_DOWNSPREAD (0x02C2)
FPLL1_DISABLE_SSCG (0x02C3)
INFORMAT_SEL0_REG (0x011A)
RXLANESEL0_REG (0x0109)
FPLL0_OLANE (0x0105)
FCTHRIO_MODE0 (0x0101)
DUPLICATED0_REG (0x0104)
INFORMAT_SEL1_REG (0x011A)
RXLANESEL1_REG (0x010A)
FPLL1_OLANE (0x0106)
FCTHRIO_MODE1 (0x0102)
DUPLICATED1_REG (0x0104)

7.4.2.1. Single MIPI DSI Input / Single V-by-One® HSII Output Operation

Single MIPI DSI Input / Single V-by-One® HS II Output mode supports frequency up to 116MHz for 24-bit video when paired with the compatible deserializer.

MODE_REG (0x0100[3:0]): 0x0, Pin Entry Index 1.

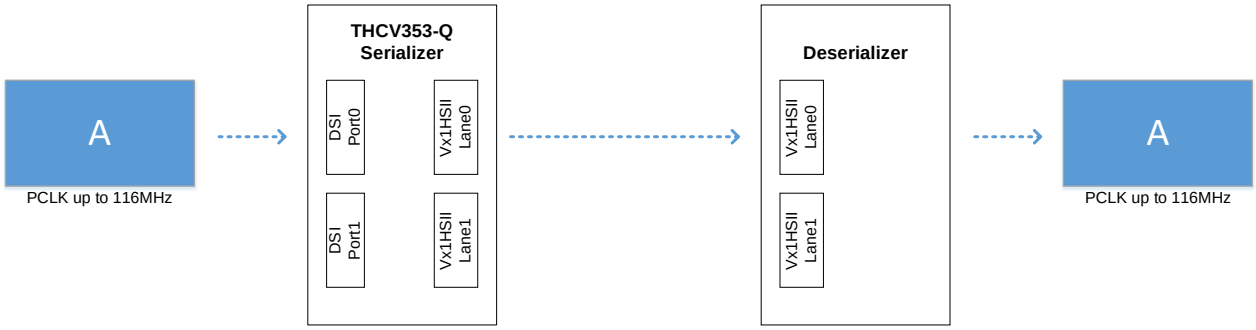


Figure 16. Single MIPI DSI Input / Single V-by-One® HSII Output Operation

7.4.2.2. Single MIPI DSI input / Dual Odd/Even V-by-One®HSII Output Operation

Single MIPI DSI Input / Dual Odd/Even V-by-One® HS II Output mode supports frequency up to 232MHz for 24-bit video when paired with the compatible deserializer. This allows support for full 1080p video.

MODE_REG (0x0100[3:0]): 0x1, Pin Entry Index 2.

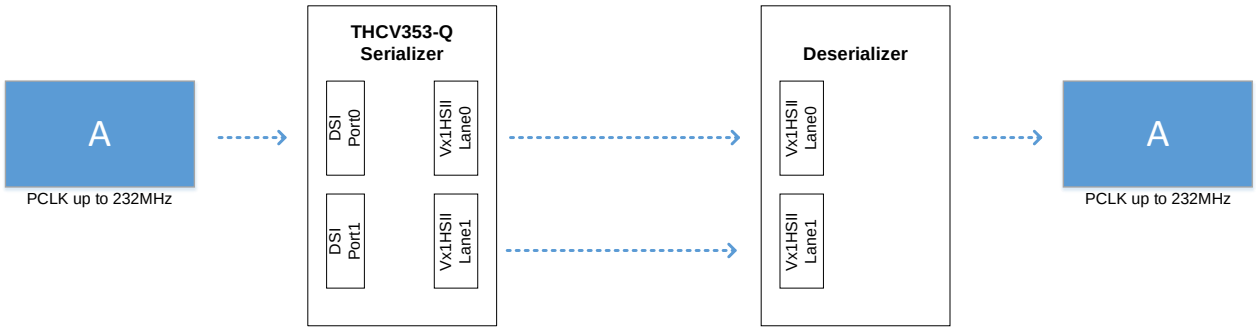


Figure 17. Single MIPI DSI Input / Dual Odd/Even V-by-One® HSII Output Operation

7.4.2.3. Single MIPI DSI input / Dual Odd/Even Splitting V-by-One®HSII output Operation

Single MIPI DSI Input / Dual Odd/Even Splitting V-by-One® HS II Output mode supports frequency up to each 116MHz for 24-bit video when paired with the compatible deserializers.

MODE_REG (0x0100[3:0]): 0x2.

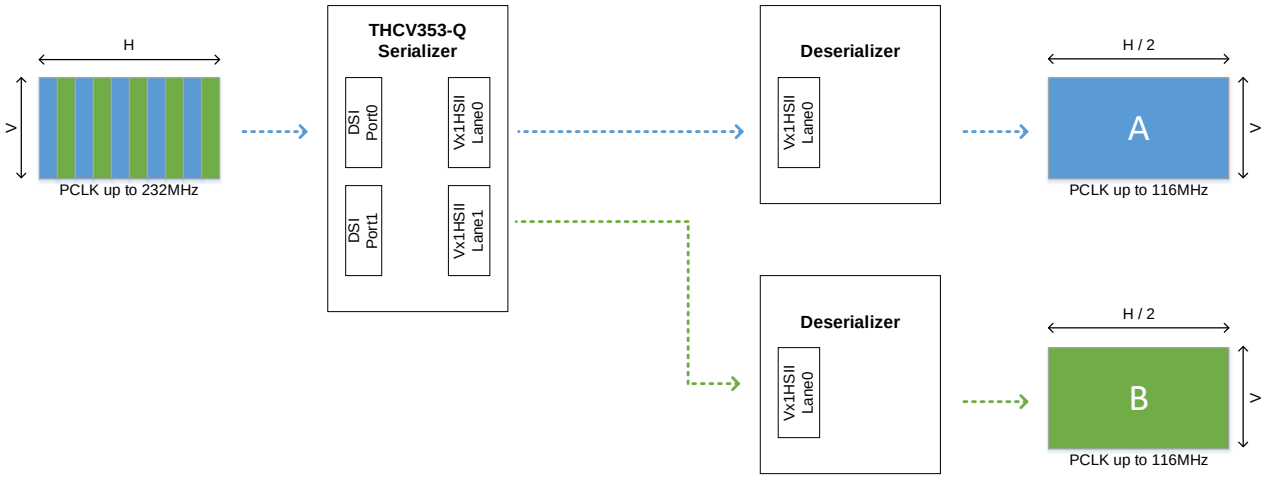


Figure 18. Single MIPI DSI input / Dual Odd/Even Splitting V-by-One®HSII output Operation

7.4.2.4. Single MIPI DSI input / Dual Left/Right Splitting V-by-One®HSII output Operation

Single MIPI DSI Input / Dual Left/Right Splitting V-by-One® HS II Output mode supports frequency up to each 116MHz for 24-bit video when paired with the compatible deserializers.

MODE_REG (0x0100[3:0]): 0x5, Pin Entry Index 3.

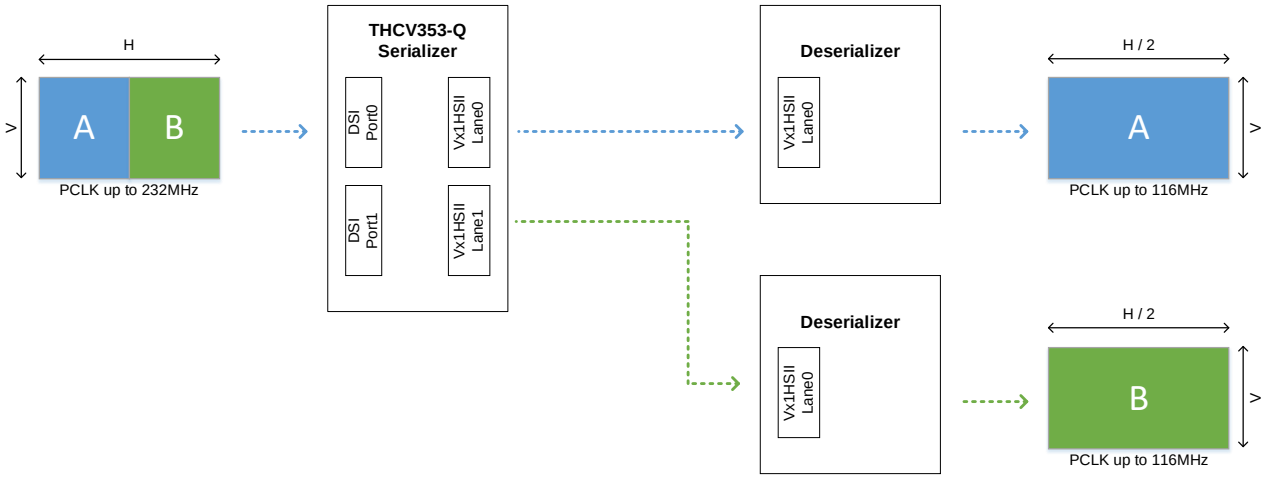


Figure 19. Single MIPI DSI input / Dual Left/Right Splitting V-by-One®HSII output Operation

For particular mode may require R_READ_DELAY arrangement from default value. For example, Left/Right splitting mode of 2160p with SYNCGEN_MODE=0x1 may be required to change R_READ_DELAY0 to 0d32 from default value 0d100.

7.4.2.5. Single MIPI DSI input / Dual Left/Right Splitting and Cropping V-by-One®HSII output Operation

Single MIPI DSI Input / Dual Left/Right Splitting and Cropping V-by-One® HS II Output mode supports frequency up to each 116MHz for 24-bit video when paired with the compatible deserializers.

MODE_REG (0x0100[3:0]): 0x6.

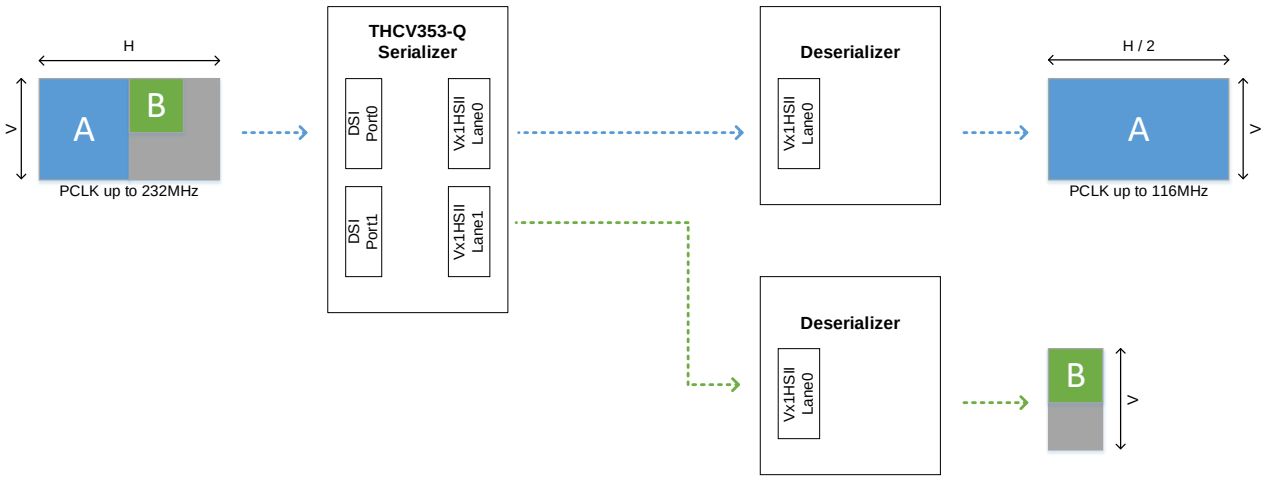


Figure 20. Single MIPI DSI input / Dual Left/Right Splitting and Cropping V-by-One®HSII output Operation

Cropping requires R_CROP_* (0x0808/0x0809/0x080A/0x080B) setting. Cropping arrangement is limited to small extent flexibility with preserved Htotal and Vtotal.

For particular mode may require R_READ_DELAY arrangement from default value. For example, Left/Right splitting and cropping mode of 1080p may be required to change R_READ_DELAY1 to 0d800 from default value 0d100.

7.4.2.6. Dual Left/Right MIPI DSI input / Dual Aggregation V-by-One®HSII output Operation

Dual Link MIPI DSI Input / Dual V-by-One® HS II Output mode supports frequency up to 232MHz for 24-bit video when paired with the compatible deserializer.

MODE_REG (0x0100[3:0]): 0xB.

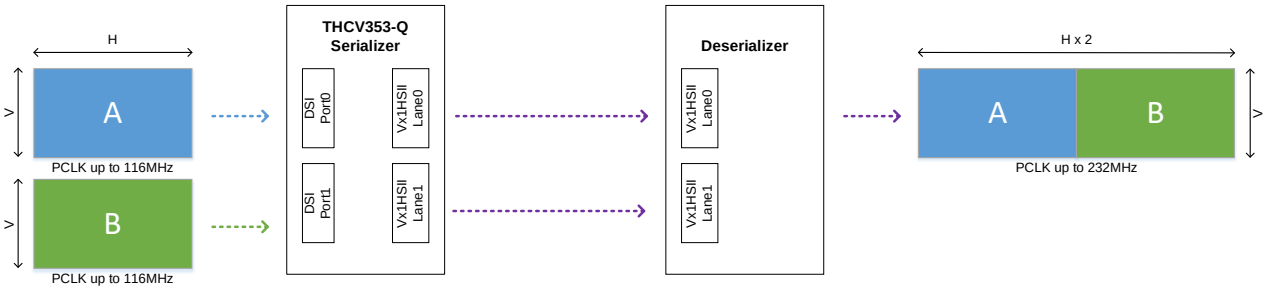


Figure 21. Dual Left/Right MIPI DSI input / Dual Aggregation V-by-One®HSII output Operation

For particular mode may require R_READ_DELAY arrangement from default value. For example, aggregation mode of two 1920x720 may be required to change R_READ_DELAY0 to 0d16 from default value 0d100.

7.4.2.7. Dual Asynchronous MIPI DSI input / Dual V-by-One®HSII output Operation

Dual Asynchronous MIPI DSI Input / Dual V-by-One® HS II Output mode supports frequency up to each 116MHz for 24-bit video when paired with the compatible deserializers.

MODE_REG (0x0100[3:0]): 0xC.

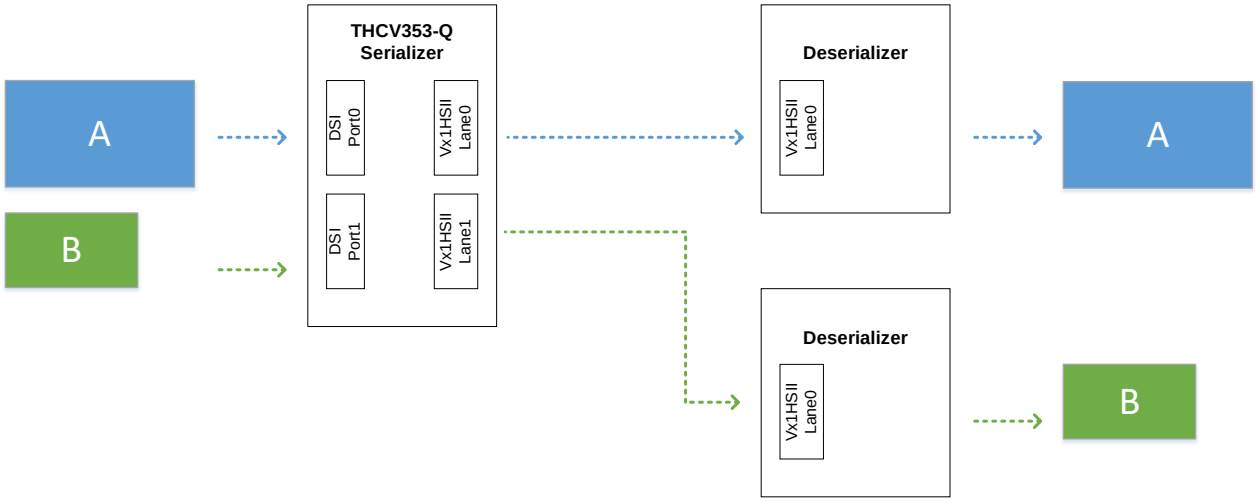


Figure 22. Dual Asynchronous MIPI DSI input / Dual V-by-One®HSII output Operation

7.4.2.8. Single MIPI DSI Input / Dual Distribution V-by-One® HSII output Operation

In this mode, the same video (up to 116MHz, 24-bit color) is delivered to each receiver.

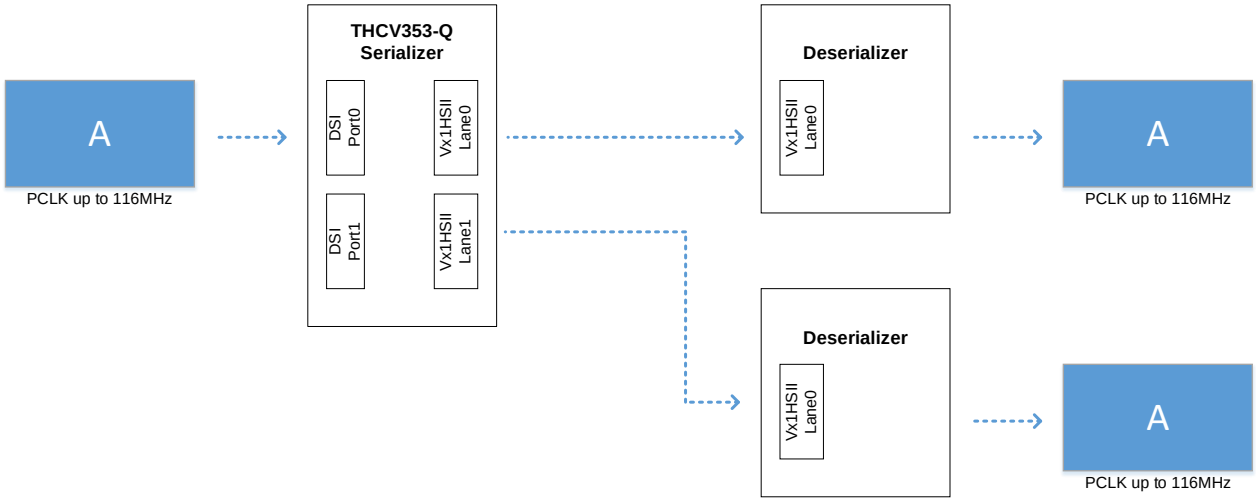


Figure 23. Single MIPI DSI Input / Dual Distribution V-by-One® HSII output Operation

Below are setting example.

// comment

//Vx1HSII Tx Lane Override Lane0 and Lane1 Enable

cmd: write devaddr: 0x0B regaddr: 0x0111 val: 0x15

// Vx1HSII Tx Lane Swap assignment: Lane1 output is assigned to Lane0 intended data for distribution

cmd: write devaddr: 0x0B regaddr: 0x0117 val: 0xA4

7.4.3. Low Frequency mode

Low Frequency mode speed up the Forward Channel data-rate x2 or x4 in order to support the situation in which Open-LDI input frequency is too low to excess minimum data-rate of Forward Channel by the use of normal speed. For usage of Low Frequency mode, counterpart V-by-One® HS II receiver must have installed Low Frequency mode format decoder.

7.4.4. Independent External FC and BC operation mode

BCC operation can be separated in Independent External FC and BC mode. Register EXTBC control can enable separated BC.

EXTBC_EN_REG must be set the same mode with the Deserializer side.

Its register address is 0x0118 val: 0x01 // VbyOneHSII BCC external input enable

Independent External FC and BC initialization is typically impossible with remote internal register access.

Serializer and Deserializer must be set independently by particular MCU or other measure.

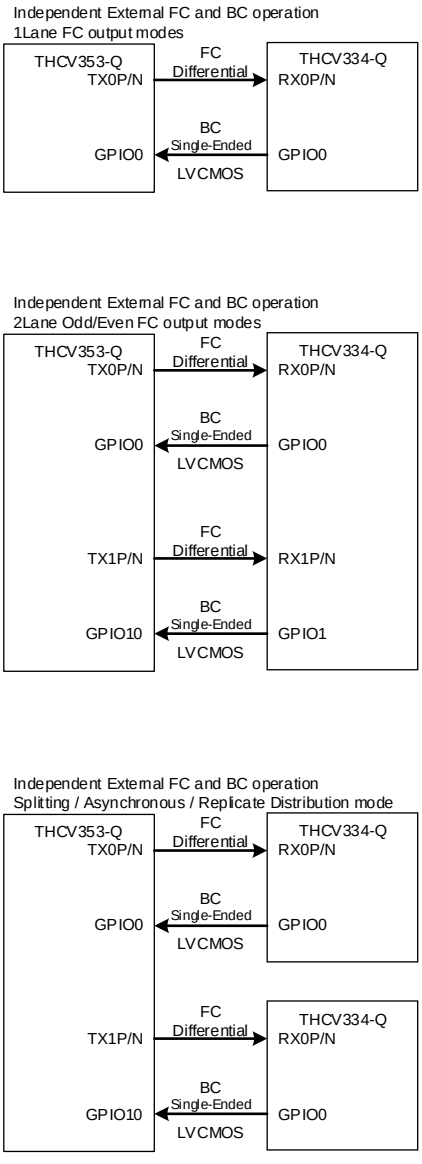


Figure 24. Independent External FC and BC operation mode

7.4.5. V-by-One® HS external LOCKN mode

V-by-One® HS behavior, in which FCTHRIO is disabled, is connectable to standard V-by-One® HS product with external LOCKN connection.

V-by-One® HS LOCKN inputs for respective lanes, Lane0 and Lane1, are supposed to be input separately, which may require external care on PCB.

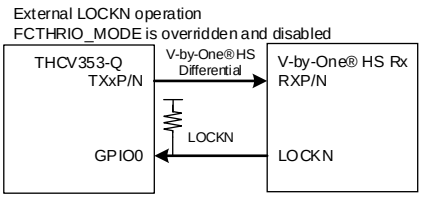


Figure 25. V-by-One® HS external LOCKN mode

Below are setting example.

External LOCKN initialization is impossible with remote internal register access. Serializer and Deserializer must be set independently by particular SoC or other measure.

// comment
//Single in Single out mode
cmd: write devaddr: 0x0B regaddr: 0x0100 val: 0x10
//Through IO Disable
cmd: write devaddr: 0x0B regaddr: 0x0101 val: 0x12
//Vx1HSII Output enable
cmd: write devaddr: 0x0B regaddr: 0x0103 val: 0x10
//RGBtoYUV Enable
cmd: write devaddr: 0x0B regaddr: 0x011B val: 0x01
//BC EXTBC separation
cmd: write devaddr: 0x0B regaddr: 0x0118 val: 0x01
//V-by-One® HSII control data through Disable
cmd: write devaddr: 0x0B regaddr: 0x1002 val: 0x00
//LOCKN input mode
cmd: write devaddr: 0x0B regaddr: 0x1C18 val: 0x01
//GPIO0 LOCKN for Lane0 input
cmd: write devaddr: 0x0B regaddr: 0x1C02 val: 0x01

7.5. Programming

7.5.1. Serial Control Bus

This serializer may also be configured by the use of a 2-wire interface serial control bus. Multiple devices may share the serial control bus (multiple device addresses supported). The device address (2-wire slave address) is set by AIN pin or register setting.

THCV353-Q has 2-wire serial slave function. BCC function of THCV353-Q realize 2-wire serial interface remote bridge from local 2-wire serial master to BCC compatible counterpart deserializer or remote 2-wire slave device.

7.5.2. Serial slave device ID

AIN pin determines 2-wire slave Device ID setting.

2-wire slave Device ID of BCC Slave device which is used for BCC communication is defined in register in THCV353-Q as BCC Master. 2-wire slave Device ID of BCC Slave device which is used for BCC communication may be different from 2-wire slave Device ID of BCC Slave device which is defined by AIN pin of BCC Slave device and is used for local access (NOT from BCC Master side) on BCC Slave device PCB board.

7.5.3. Serial Read/Write access to local Register

HOST MPU can directly access THCV353-Q local register by 2-wire serial I/F.

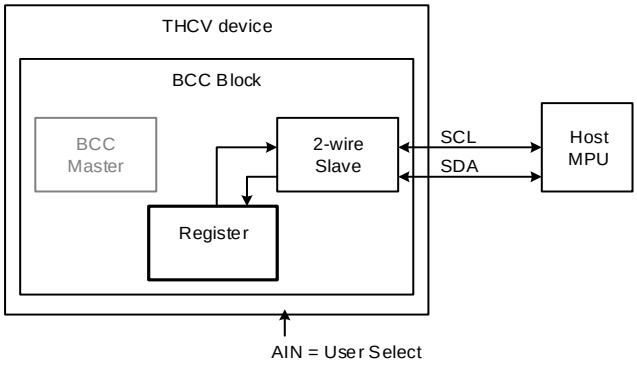


Figure 26. Host to local register access configuration

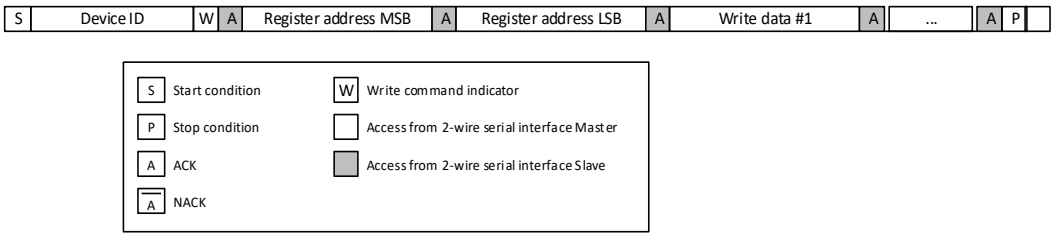


Figure 27. Serial I/F write to local register protocol

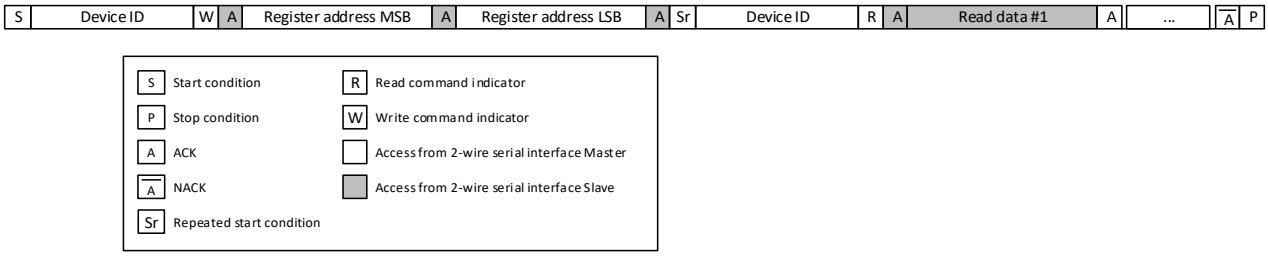


Figure 28. Serial I/F read to local register protocol

7.5.4. Bi-directional Control Channel bus

THCV353-Q has Bi-directional Control Channel (BCC) which enables bi-directional transmission of 2-wire serial interface signals, GPIO signals and also HTPDN/LOCKN signals for FC. THCV353-Q is BCC Master and connectable to BCC Slave device such as THCV334-Q.

To use GPIO (General Purpose Input/Output) pin, fault/error detection and interrupt function, “2-wire Set & Trigger mode”, “2-wire Pass Through mode” enables remote register access. THCV353-Q, BCC Master device has 2-wire serial slave block and can connect to HOST MPU. On the other hand, the counterpart BCC Slave device has 2-wire serial master block and can connect to remote side 2-wire serial slave devices.

HOST MPU can access register of BCC Master device, BCC Slave device and remote side 2-wire serial slave devices.

7.5.4.1. Serial Read/Write access to remote Register

The same serial access protocol as ones to local register are also available even in the case to remote register of BCC Slave device or remote-side 2-wire serial slave devices.

In addition, another read access protocol is available for remote read.

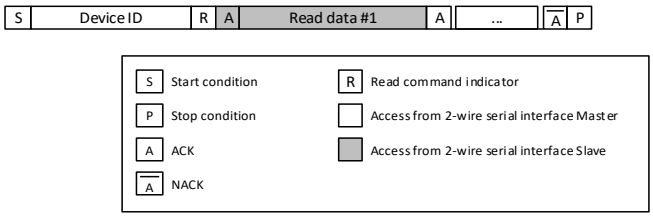


Figure 29. Serial I/F read to remote register protocol 2

7.5.4.2. BCC 2-wire Set and Trigger mode

HOST MPU can access to BCC Slave device register via THCV353-Q as BCC Master only by THCV353-Q internal local register control and monitoring on 2-wire Set&Trigger mode.

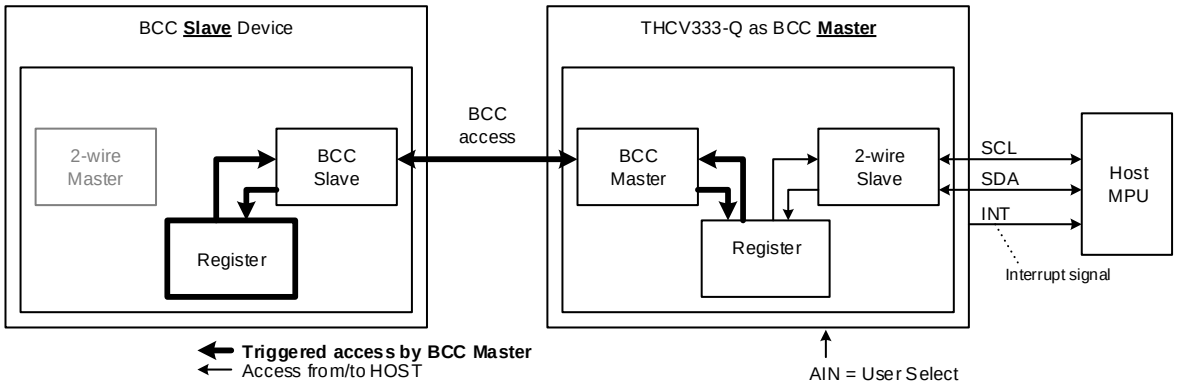


Figure 30. Host MPU to BCC Slave Register via THCV333-Q access configuration

HOST MPU can access to remote side 2-wire serial slave register via THCV353-Q as BCC Master only by THCV353-Q internal local register control and monitoring on 2-wire Set&Trigger mode.

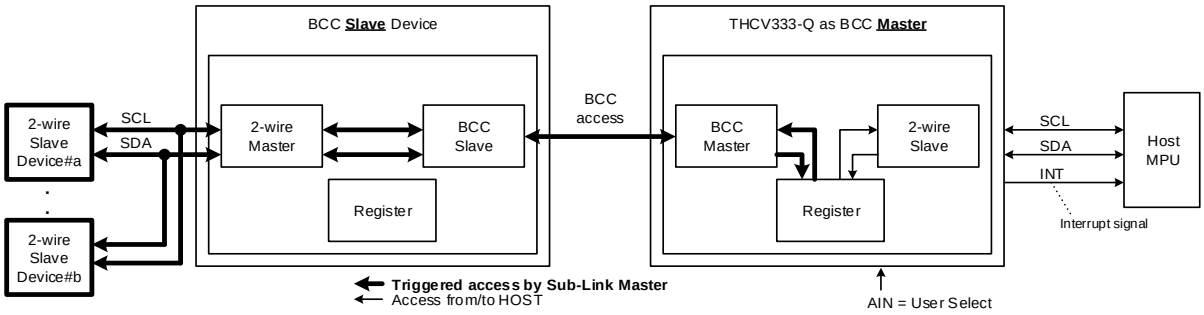


Figure 31. Host MPU to remote 2-wire slave devices via THCV242A access configuration

In principle, when BCC bridges 2-wire serial interface communication from BCC Master to BCC Slave or remote side 2-wire serial slave devices, time lag occurs between HOST MPU side 2-wire serial access and BCC Slave internal bus access or remote side 2-wire serial access.

When Set&Trigger mode is selected, 2-wire serial slave of BCC Master does not perform clock stretching. THCV353-Q, BCC Master device, informs HOST MPU that BCC Slave register access or remote side 2-wire serial register access has completed by interruption (detectable on INTN pin) without clock stretching.

7.5.4.3. BCC 2-wire Pass Through mode

BCC Master 2-wire Pass Through mode can bridge original local 2-wire commands to remote side. 2-wire Pass Through mode uses 2-wire slave clock stretching scheme at local BCC Master side. Host MCU 2-wire master must be no problem with clock stretching wait from 2-wire slave.

On address processing protocol “Assigned address & rename”, THCV353-Q 2-wire slave respond only to pre-defined-by-register particular 2-wire device address for remote Pass Through operation. Otherwise, 2-wire commands are ignored except THCV353-Q itself address. The device address can be renamed before remote send. The counterpart BCC Slave internal register access is available with separately defined another register setting.

On address processing protocol “All Through”, THCV353-Q 2-wire slave respond basically all 2-wire device address for remote Pass Through operation except THCV353-Q itself address. Additionally, Particular defined-by-register addresses can be ignored by THCV353-Q.

BCC Slave side processing protocol “Divided write/read” scheme divides 2-wire commands into determined data Byte groups. Each data Byte groups are sent separately on remote side. Burst write/read access target Sub-Address (Word-Address) is interpreted so that subsequent Sub-Address (Word-Address) from 2nd group is automatically and properly incremented. As shown below, remote side 2-wire accesses are independent each other by determined Byte, which are defined in R_2WIRE_PASS_ADR_BYTE_NUM and R_2WIRE_PASS_DATA_BYTE_NUM at R_2WIRE_PASS_MODE=0x00 or 0x01.

R_2WIRE_INTERMITTENT_MODE must be set the same mode with the BCC Slave (Deserializer) side. Its register address is 0x0B6A val: 0x00 //Default.

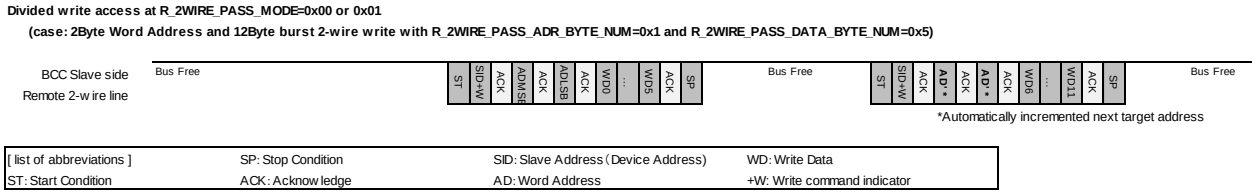


Figure 32. 2-wire Pass Through mode BCC Slave command Divided scheme

BCC Slave side processing protocol “Non-divided write/read” scheme divides 2-wire commands into determined data Byte groups. Each data Byte groups are also sent separately on remote side. However burst write/read access target Sub-Address (Word-Address) is NOT incremented, the access complete including SCL Low period.

R_2WIRE_INTERMITTENT_MODE must be set the same mode with the BCC Slave (Deserializer) side. Its register address is 0x0B6A val: 0x01 //Non-divided write/read mode enable

While R_2WIRE_INTERMITTENT_MODE is not the same mode under initialization temporary phase, 1 Byte remote internal register access read/write is possible with no failure.

When the local 2-wire communication ended with stop condition, however, still the remote 2-wire communication had not ended that time, the next 2-wire action driven from local external host is kept waiting right after start condition with clock-stretch until the remote 2-wire communication ended. This behavior may interfere the communication between host and another 2-wire device connected to the same local 2-wire bus.

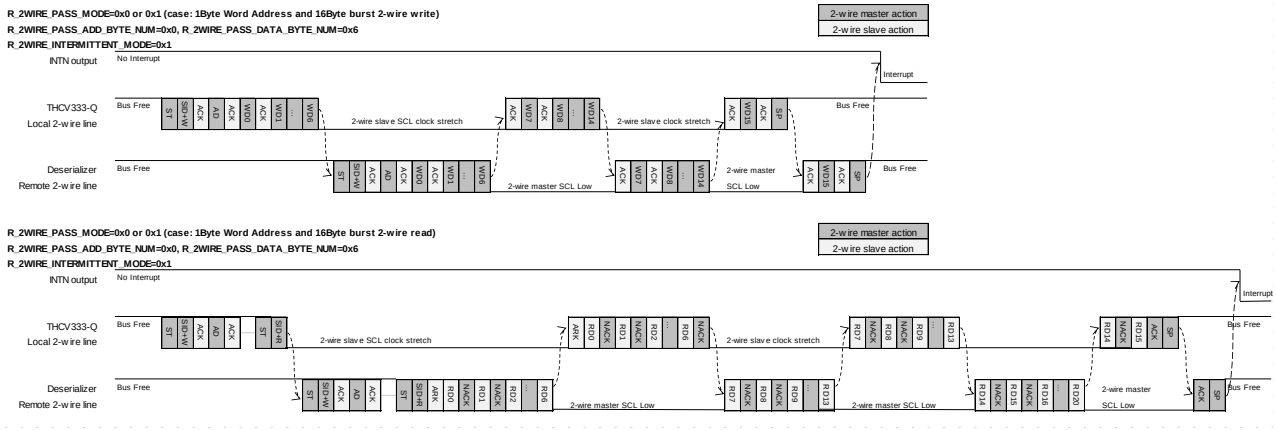


Figure 33. 2-wire Pass Through Non-divided mode BCC Slave command write/read scheme

7.5.5. Restrictions on Multi-Master Coexistence Operation

Only one 2-wire interface transaction should be active at any time across the Bidirectional Control Channel. If Multi-Master coexistence are required, some method of transferring control initiative and avoidance of control collision between 2-wire interface masters at local and remote should be implemented.

7.6. Register Maps

Register regions are sectioned as below.

Table 24. Register Regiions

Reg address		Assignment
Start	End	SER block
0x0000	0x00FF	RESET
0x0100	0x01FF	MODE
0x0200	0x02FF	CLOCK
0x0400	0x04FF	MIPIRX_PORT0
0x0500	0x05FF	MIPIRX_PORT1
0x0600	0x063F	FC_CTL
0x0640	0x067F	PATGEN_PORT0
0x0680	0x06FF	PATGEN_PORT1
0x0700	0x077F	PATCHK_PORT0
0x0780	0x07FF	PATCHK_PORT1
0x0800	0x08FF	IFIFO
0x0900	0x09FF	FCTX_BCRX_LANE0
0x0A00	0x0AFF	FCTX_BCRX_LANE1
0x0B00	0x0BFF	I2CBM
0x0C00	0x0CFF	I2SGPIO
0x0D00	0x0DFF	DSI_PORT0
0x0E00	0x0EFF	DSI_PORT1
0x1000	0x10FF	FC_TX_LANE0
0x1100	0x11FF	FC_TX_LANE1
0x1200	0x12FF	CHECKSUM
0x1300	0x13FF	INTN
0x1400	0x14FF	REM_INTN0
0x1500	0x15FF	REM_INTN1
0x1700	0x17FF	FC_THRIO_LANE0
0x1800	0x18FF	BC_THRIO_LANE0
0x1900	0x19FF	FC_THRIO_LANE1
0x1A00	0x1AFF	BC_THRIO_LANE1
0x1C00	0x1CFF	DEBUG

NOTE

Any registers, which are not explained in this Register Maps, must be left untouched (No write nor read are allowed.) as default.

Any reserved registers, which are explained in this Register Maps and its all bits of the register address is reserved, must be left untouched (No write nor read are allowed.) as default.

Any reserved bits, which are explained in this Register Maps and remained bits other than the reserved bits in the same address is available function bits, according to the instruction of function bits, reserved bits can be write or read as 1 Byte unit access of 2-wire communication.

Any Read Only registers, whose “R/W” classification column is “R” in this Register Maps, are prohibited to be written by Write access.

Address	bit	Register Name	width	R/W	Init	Description
0x0000	[7:2]	reserved	6	-	-	-
	[1]	I2SPLL_SPD_P0	1	R/W	1'h0	I2S PLL Power down for port0 0x0: Power on 0x1: Power down
	[0]	PLL_SPD_P0	1	R/W	1'h0	PLL Power down for port0 0x0: Power on 0x1: Power down Need power down while changing operation mode in Register Entry mode. See Register Entry Section.
0x0001	[7:1]	reserved	7	-	-	-
	[0]	FCRX_SPD_P0	1	WC	1'h0	MIPI DSI RX Power Down for port0 0x0: Power on 0x1: Power down
0x0002	[7:0]	reserved	8	-	-	-
0x0003	[7:0]	reserved	8	-	-	-
0x0004	[7:0]	reserved	8	-	-	-
0x0010	[7:1]	reserved	7	-	-	-
	[0]	FCRX_SRST_P0	1	WC	1'h0	MIPI DSI RX Reset for port0 0x0: Reset release 0x1: Reset, auto clear to 0
0x0011	[7:5]	reserved	3	-	-	-
	[4]	FIFO_FCTX_SRST	1	WC	1'h0	FIFO FCTX Logic Reset 0x0: Reset release 0x1: Reset, auto clear to 0
	[3]	reserved	1	-	-	-
	[2]	FIFO_MAIN_SRST	1	WC	1'h0	FIFO MAIN Logic Reset 0x0: Reset release 0x1: Reset, auto clear to 0
	[1]	reserved	1	-	-	-
	[0]	FIFO_FCRX_SRST	1	WC	1'h0	FIFO DSI RX Logic Reset 0x0: Reset release 0x1: Reset, auto clear to 0
0x0012	[7:5]	reserved	3	-	-	-
	[4]	FCTX_SRST	1	WC	1'h0	FCTX Logic Reset 0x0: Reset release 0x1: Reset, auto clear to 0
	3:0]	reserved	4	-	-	-
0x0013	[7:1]	reserved	7	-	-	-
	[0]	BC_SRST	1	WC	1'h0	BC Logic Reset 0x0: Reset release 0x1: Reset, auto clear to 0
0x0014	[7:4]	reserved	4	-	-	-
	[3]	FREF_SRST_P0	1	WC	1'h0	PLL Input Clock Detector Logic Reset for port0 0x0: Reset release 0x1: Reset, auto clear to 0
	[2]	I2CB_SRST_P0	1	WC	1'h0	I2CBM Logic Reset for port0 0x0: Reset release 0x1: Reset, auto clear to 0
	[1]	APB_SRST_P0	1	WC	1'h0	APB Logic Reset for port0 0x0: Reset release 0x1: Reset, auto clear to 0
	[0]	OSC_SRST_P0	1	WC	1'h0	Oscillator Logic Reset for port0 0x0: Reset release 0x1: Reset, auto clear to 0
0x0015	[7:0]	reserved	8	-	-	-
0x0016	[7:0]	reserved	8	-	-	-
0x0017	[7:0]	reserved	8	-	-	-
0x0018	[7:0]	reserved	8	-	-	-
0x0019	[7:0]	reserved	8	-	-	-
0x001A	[7:2]	reserved	6	-	-	-
	[1]	PLZLOCK_EN_P0	1	R/W	1'h1	PLL Lock Detect Enable for DSI port0. Must be set 0x1. 0x0: Reserved. 0x1: Enable
	[0]	RXLOCKN_EN_P0	1	R/W	1'h1	DSI Clock Detect Enable for DSI port0. When use REFCLK input, set disable. 0x0: Disable 0x1: Enable
0x001B	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0020	[7:1]	reserved	7	-	-	-
	[0]	CMN_SRST_P0	1	WC	1'h0	All Register clear for port0 0x1: Reset and automatic clear
0x0021	[7:0]	reserved	8	-	-	-
0x0022	[7:0]	reserved	8	-	-	-
0x0023	[7:0]	reserved	8	-	-	-
0x0024	[7:0]	reserved	8	-	-	-
0x0025	[7:0]	reserved	8	-	-	-
0x0026	[7:0]	reserved	8	-	-	-
0x0030	[7:0]	reserved	8	-	-	-
0x0040	[7:2]	reserved	6	-	-	-
	[1]	I2SPLL_SPD_P1	1	R/W	1'h0	I2S PLL Power down for port1 0x0: Power on 0x1: Power down
	[0]	PLL_SPD_P1	1	R/W	1'h0	PLL Power down for port1 0x0: Power on 0x1: Power down Need power down while changing operation mode in Register Entry mode. See Register Entry Section.
0x0041	[7:2]	reserved	6	-	-	-
	[1:0]	FCRX_SPD_P1	2	WC	2'h0	FC RX Power Down for port1 0x0: Power on 0x1: Power down Other: Reserved
0x0042	[7:0]	reserved	8	-	-	-
0x0043	[7:0]	reserved	8	-	-	-
0x0044	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0050	[7:2]	reserved	6	-	-	-
	[1:0]	FCRX_SRST_P1	2	WC	2'h0	FC RX Reset for port1 0x0: Reset release 0x1: Reset, auto clear to 0 Other: Reserved
0x0051	[7:0]	reserved	8	-	-	-
0x0052	[7:0]	reserved	8	-	-	-
0x0053	[7:0]	reserved	8	-	-	-
0x0054	[7:4]	reserved	4	-	-	-
	[3]	FREF_SRST_P1	1	WC	1'h0	PLL Input Clock Detector Logic Reset for port1 0x0: Reset release 0x1: Reset, auto clear to 0
	[2]	I2CB_SRST_P1	1	WC	1'h0	I2CBM Logic Reset for port1 0x0: Reset release 0x1: Reset, auto clear to 0
	[1]	APB_SRST_P1	1	WC	1'h0	APB Logic Reset for port1 0x0: Reset release 0x1: Reset, auto clear to 0
	[0]	OSC_SRST_P1	1	WC	1'h0	Oscillator Logic Reset for port1 0x0: Reset release 0x1: Reset, auto clear to 0
0x0055	[7:0]	reserved	8	-	-	-
0x0056	[7:0]	reserved	8	-	-	-
0x0057	[7:0]	reserved	8	-	-	-
0x0058	[7:0]	reserved	8	-	-	-
0x0059	[7:0]	reserved	8	-	-	-
0x005A	[7:2]	reserved	6	-	-	-
	[1]	PLZLOCK_EN_P1	1	R/W	1'h1	PLL Lock Detect Enable for DSI port1. Must be set 0x1. 0x0: Reserved. 0x1: Enable
	[0]	RXLOCKN_EN_P1	1	R/W	1'h1	DSI Clock Detect Enable for DSI port1. When use REFCLK input, set disable. 0x0: Disable 0x1: Enable
0x005B	[7:0]	reserved	8	-	-	-
0x0060	[7:1]	reserved	7	-	-	-
	[0]	CMN_SRST_P1	1	WC	1'h0	All Register clear for port1 0x1: Reset and automatic clear
0x0061	[7:0]	reserved	8	-	-	-
0x0062	[7:0]	reserved	8	-	-	-
0x0063	[7:0]	reserved	8	-	-	-
0x0064	[7:0]	reserved	8	-	-	-
0x0065	[7:0]	reserved	8	-	-	-
0x0066	[7:0]	reserved	8	-	-	-
0x0070	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0100	[7:5]	reserved	3	-	-	-
	[4]	MODE_REG_OVERRIDE	1	R/W	1'h0	MODE override enable. Can override operation mode without pin settings. 0x0: disable 0x1: enable
	[3:0]	MODE_REG	4	R/W	4'h0	<this regiseter is valid only when 0x0100[4]=1> Operation mode setting. See operation mode section for details. 0x0: Single MIPI DSI Input / Single V-by-One®HSII Output 0x1: Single MIPI DSI input / Dual Odd/Even V-by-One® HSII output 0x2: Single MIPI DSI input / Dual Odd/Even Splitting V-by-One®HSII output 0x3: Dual Odd/Eben MIPI DSI input / Dual Aggregation V-by-One®HSII output 0x5: Single MIPI DSI input / Dual Left/Right Splitting V-by-One®HSII output 0x6: Single MIPI DSI input / Dual Left/Right Splitting and Cropping V-by-One®HSII output 0xB: Dual Left/Right MIPI DSI input / Dual Aggregation V-by-One®HSII output 0xC: Dual Asynchronous MIPI DSI input / Dual V-by-One®HSII output Others: Reserved
0x0101	[7:5]	reserved	3	-	-	-
	[4]	FCTHRIO_MODE_OVERRIDE_L0	1	R/W	1'h1	Must be set 1.
	[3:2]	reserved	2	-	-	-
	[1]	FCTHRIO_MODE_DISABLE_L0	1	R/W	1'h0	FCTHRIO disable setting for VbyOneHS lane0. To connect with VbyOneHS Deserializer may set disable. 0x0: enable 0x1: disable
	[0]	FCTHRIO_MODE_REG_L0	1	R/W	1'h0	<this regiseter is valid only when 0x0101[4]=1> FCTHRIO MODE setting for VbyOneHS lane0. 0x0: 8cycle mode 0x1: 4cycle mode Need to set the same mode with Deserializer.
0x0102	[7:5]	reserved	3	-	-	-
	[4]	FCTHRIO_MODE_OVERRIDE_L1	1	R/W	1'h1	Must be set 1.
	[3:2]	reserved	2	-	-	-
	[1]	FCTHRIO_MODE_DISABLE_L1	1	R/W	1'h0	FCTHRIO disable setting for VbyOneHSII lane1. To connect with VbyOneHS Deserializer may set disable. 0x0: enable 0x1: disable
	[0]	FCTHRIO_MODE_REG_L1	1	R/W	1'h0	<this regiseter is valid only when 0x0101[4]=1> FCTHRIO MODE setting for VbyOneHS lane1 0x0: 8cycle mode 0x1: 4cycle mode Need to set the same mode with Deserializer.
0x0103	[7:5]	reserved	3	-	-	-
	[4]	OUTPUT_ENABLEN_OVERRIDE	1	R/W	1'h0	VbyOneHSII output override enable. Can override operation mode without BCMONP_OEN pin settings. 0x0: disable 0x1: enable
	[3:1]	reserved	3	-	-	-
	[0]	OUTPUT_ENABLEN_REG	1	R/W	1'h1	VbyOneHSII output control. 0x0: enable 0x1: disable
0x0104	[7:6]	reserved	2	-	-	-
	[5:4]	DUPLICATE_REG_L1	2	R/W	2'h0	Low frequency mode select for VbyOneHSII lane1. This register is used when the VbyOneHSII FC rate is too slow to meet the specification or to increase the sampling rate of the control signal. 0x0: FC data rate x1 mode 0x1: FC data rate x2 mode 0x2: FC data rate x4 mode 0x3: FC data rate x8 mode
	[3:2]	reserved	2	-	-	-
	[1:0]	DUPLICATE_REG_L0	2	R/W	2'h0	Low frequency mode select for VbyOneHSII lane0. This register is used when the VbyOneHSII FC rate is too slow to meet the specification or to increase the sampling rate of the control signal. 0x0: FC data rate x1 mode 0x1: FC data rate x2 mode 0x2: FC data rate x4 mode 0x3: FC data rate x8 mode
0x0105	[7:0]	FPLL0_OLANE	8	R/W	8'h0	Reserved: must be left default.
0x0106	[7:0]	FPLL1_OLANE	8	R/W	8'h0	Reserved: must be left default.

Address	bit	Register Name	width	R/W	Init	Description
0x0107	[7:5]	reserved	3	-	-	-
	[4]	HIGHFREQIN_REG_P1	1	R/W	1'h0	DSI clock frequency select for port1 Must be set 0
	[3:1]	reserved	3	-	-	-
	[0]	HIGHFREQIN_REG_P0	1	R/W	1'h0	DSI clock frequency select for port0 Must be set 0
0x0108	[7:1]	reserved	7	-	-	-
	[0]	REFCLK_EN_REG	1	R/W	1'h0	REFCLK Input Mode Enable. Also need to set enable for internal oscillator operation mode. 0x0: Disable 0x1: Enable
0x0109	[7:5]	reserved	3	-	-	-
	[4]	RXLANESEL_OVERRIDE_P0	1	R/W	1'h1	DSI lane setting override enable for port0. Can override operation mode without REM_INTN0_RXLANE pin settings. 0x0: disable 0x1: enable
	[3:2]	reserved	2	-	-	-
	[1:0]	RXLANESEL_REG_P0	2	R/W	1'h0	DSI lane setting for port0. Need to set before setting MODE_REG_OVERRIDE to 1. See register entry section for details. 0x0: 4lane mode 0x1: 2lane mode 0x2: 1lane mode 0x3: Reserved
0x010A	[7:5]	reserved	3	-	-	-
	[4]	RXLANESEL_OVERRIDE_P1	1	R/W	1'h1	DSI lane setting override enable for port1. Can override operation mode without REM_INTN0_RXLANE pin settings. 0x0: disable 0x1: enable
	[3:2]	reserved	2	-	-	-
	[1:0]	RXLANESEL_REG_P1	2	R/W	1'h0	DSI lane setting for port1. Need to set before setting MODE_REG_OVERRIDE to 1. See register entry section for details. 0x0: 4lane mode 0x1: 2lane mode 0x2: 1lane mode 0x3: Reserved
0x010B	[7:6]	RXLSWAP_L3_REG_P0	2	R/W	2'h3	DSI input lane swap select for lane3 or port0. Set lane number. It cannot be the same number as other lanes
	[5:4]	RXLSWAP_L2_REG_P0	2	R/W	2'h2	DSI input lane swap select for lane2 or port0. Set lane number. It cannot be the same number as other lanes
	[3:2]	RXLSWAP_L1_REG_P0	2	R/W	2'h1	DSI input lane swap select for lane1 or port0. Set lane number. It cannot be the same number as other lanes
	[1:0]	RXLSWAP_L0_REG_P0	2	R/W	2'h0	DSI input lane swap select for lane0 or port0. Set lane number. It cannot be the same number as other lanes
0x010C	[7:6]	RXLSWAP_L3_REG_P1	2	R/W	2'h3	DSI input lane swap select for lane3 or port1. Set lane number. It cannot be the same number as other lanes
	[5:4]	RXLSWAP_L2_REG_P1	2	R/W	2'h2	DSI input lane swap select for lane2 or port1. Set lane number. It cannot be the same number as other lanes
	[3:2]	RXLSWAP_L1_REG_P1	2	R/W	2'h1	DSI input lane swap select for lane1 or port1. Set lane number. It cannot be the same number as other lanes
	[1:0]	RXLSWAP_L0_REG_P1	2	R/W	2'h0	DSI input lane swap select for lane0 or port1. Set lane number. It cannot be the same number as other lanes
0x010D	[7:6]	reserved	2	-	-	-
	[5]	RX1VREFEN	1	R/W	1'h1	DSI Port1 Reference Voltege Enable 0x0:Disable 0x1:Enable
	[4]	RX1IREFEN	1	R/W	1'h1	DSI Port1 Reference Current Enable 0x0:Disable 0x1:Enable
	[3:2]	reserved	2	-	-	-
	[1]	RX0VREFEN	1	R/W	1'h1	DSI Port0 Reference Voltege Enable 0x0:Disable 0x1:Enable
	[0]	RX0IREFEN	1	R/W	1'h1	DSI Port0 Reference Current Enable 0x0:Disable 0x1:Enable
0x010E	[7:6]	reserved	2	-	-	-
	[5]	RXFLIPCLK_P1	1	R/W	1'h0	DSI Clock lane P/N Swap control for port1 0x0: Normal mode 0x1: P/N Swap
	[4]	RXFLIP_P1	1	R/W	1'h0	DSI Data lane P/N Swap control for port1 0x0: Normal mode 0x1: P/N Swap
	[3:2]	reserved	2	-	-	-
	[1]	RXFLIPCLK_P0	1	R/W	1'h0	DSI Clock lane P/N Swap control for port0 0x0: Normal mode 0x1: P/N Swap
	[0]	RXFLIP_P0	1	R/W	1'h0	DSI Data lane P/N Swap control for port0 0x0: Normal mode 0x1: P/N Swap
0x010F	[7:0]	reserved	8	-	-	-
0x0110	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0111	[7:0]	reserved	3	-	-	-
	[4]	TXLANE_EN_OVERRIDE	1	R/W	1'h0	Vx1HSII lane setting override enable. 0x0: Disable 0x1: Enable
	[3]	reserved	1	-	-	-
	[2]	TXLANE_EN_REG_L1	1	R/W	1'h0	Vx1HS II Tx Lane1 Enable 0x0:Disable 0x1:Enable
	[1]	reserved	1	-	-	-
	[0]	TXLANE_EN_REG_L0	1	R/W	1'h0	Vx1HS II Tx Lane0 Enable 0x0:Disable 0x1:Enable
0x0112	[7:6]	reserved	2	-	-	-
	[5:4]	SER_TXPRE_L1	2	R/W	2'h0	VbyOneHSII Pre-Emphasis control for lane1 0x0: 0% 0x1: 50% 0x2: 100% 0x3: reserved
	[3:2]	reserved	2	-	-	-
	[1:0]	SER_TXPRE_L0	2	R/W	2'h0	VbyOneHSII Pre-Emphasis control for lane0 0x0: 0% 0x1: 50% 0x2: 100% 0x3: reserved
0x0113	[7:6]	reserved	2	-	-	-
	[5:4]	SER_TXDRV_L1	2	R/W	2'h2	VbyOneHSII Drive Strength control for lane1 0x0: 200mV 0x1: 300mV 0x2: 400mV 0x3: 450mV (Only valid when SER_TXPRE_L1 = 0x0)
	[3:2]	reserved	2	-	-	-
	[1:0]	SER_TXDRV_L0	2	R/W	2'h2	VbyOneHSII Drive Strength control for lane0 0x0: 200mV 0x1: 300mV 0x2: 400mV 0x3: 450mV (Only valid when SER_TXPRE_L0 = 0x0)
0x0114	[7:5]	reserved	3	-	-	-
	[4]	SER_TXFLIP_L1	1	R/W	1'h0	VbyOneHSII P/N Swap control for lane1 0x0: Normal mode 0x1: P/N Swap
	[3:1]	reserved	3	-	-	-
	[0]	SER_TXFLIP_L0	1	R/W	1'h0	VbyOneHSII P/N Swap control for lane0 0x0: Normal mode 0x1: P/N Swap
0x0115	[7:0]	reserved	8	-	-	-
0x0116	[7:5]	reserved	3	-	-	-
	[4]	SER_TXBET_L1	1	R/W	1'h0	Field BET Mode enable setting for lane1 0x0: Disable 0x1: Enable
	[3:1]	reserved	3	-	-	-
	[0]	SER_TXBET_L0	1	R/W	1'h0	Field BET Mode enable setting for lane0 0x0: Disable 0x1: Enable
0x0117	[7:6]	reserved	2	R/W	2'h3	Must be left 0x3
	[5:4]	TXLANESWAP_L1	2	R/W	2'h2	Vx1HSII lane swap assignment. 0x0: Swap or Distribution assigned Vx1HS II Lane0 Data 0x2: Original assigned Vx1HS II Lane1 Data (default) others: reserved
	[3:2]	reserved	2	R/W	2'h1	Must be left 0x1
	[1:0]	TXLANESWAP_L0	2	R/W	2'h0	Vx1HSII lane swap assignment. 0x0: Original assigned Vx1HS II Lane0 Data (default) 0x2: Swap assigned Vx1HS II Lane1 Data others: reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0118	[7:1]	reserved	7	-	-	-
	[0]	EXTBC_EN_REG	1	R/W	1'h0	VbyOneHSII BCC external input select. It also should be set enable when connect to VbyOneHS protocol Deserializer. 0x0: Disable, Normal operation. 0x1: Enable
0x0119	[7:0]	reserved	8	-	-	-
0x011A	[7]	reserved	1	-	-	-
	[5:4]	INFORMAT_SEL_REG_P1	3	R/W	2'h0	DSI input format setting for port1 0x0: RGB888 0x1: RGB666 0x2: RGB565 0x3: YUV422 Others: Reserved
	[3]	reserved	1	-	-	-
	[2:0]	INFORMAT_SEL_REG_P0	3	R/W	2'h0	DSI input format setting for port0 0x0: RGB888 0x1: RGB666 0x2: RGB565 0x3: YUV422 Others: Reserved
0x011B	[7:1]	reserved	7	-	-	-
	[0]	OUTPUT_CONV_EN_REG	1	R/W	1'h0	RGB to YUV color space conversion select 0x0: Disable 0x1: Enable
0x011C	[7:0]	reserved	8	-	-	-
0x011D	[7]	PM_P012UP_EN	1	R/W	1'h0	VDD12P0 OverVoltage Power Monitor Enable, 0: Disable, 1: Enable
	[6]	PM_P012UN_EN	1	R/W	1'h0	VDD12P0 UnderVoltage Power Monitor Enable, 0: Disable, 1: Enable
	[5]	PM_TV12UP_EN	1	R/W	1'h0	VDD12TV OverVoltage Power Monitor Enable, 0: Disable, 1: Enable
	[4]	PM_TV12UN_EN	1	R/W	1'h0	VDD12TV UnderVoltage Power Monitor Enable, 0: Disable, 1: Enable
	[3]	PM_TVA12UP_EN	1	R/W	1'h0	VDD12TVA OverVoltage Power Monitor Enable, 0: Disable, 1: Enable
	[2]	PM_TVA12UN_EN	1	R/W	1'h0	VDD12TVA UnderVoltage Power Monitor Enable, 0: Disable, 1: Enable
	[1]	PM_L12UP_EN	1	R/W	1'h0	VDD12L OverVoltage Power Monitor Enable, 0: Disable, 1: Enable
	[0]	PM_IO33UN_EN	1	R/W	1'h0	VDDIO UnderVoltage Power Monitor Enable, 0: Disable, 1: Enable
0x011E	[7:6]	reserved	8	-	-	-
	[5]	PM_MBF12UP_EN	1	R/W	1'h0	VDD12MBF OverVoltage Power Monitor Enable, 0: Disable, 1: Enable
	[4]	PM_MBF12UN_EN	1	R/W	1'h0	VDD12MBF UnderVoltage Power Monitor Enable, 0: Disable, 1: Enable
	[3]	PM_MBG12UP_EN	1	R/W	1'h0	VDD12MBG OverVoltage Power Monitor Enable, 0: Disable, 1: Enable
	[2]	PM_MBG12UN_EN	1	R/W	1'h0	VDD12MBG UnderVoltage Power Monitor Enable, 0: Disable, 1: Enable
	[1]	PM_P112UP_EN	1	R/W	1'h0	VDD12P1 OverVoltage Power Monitor Enable, 0: Disable, 1: Enable
	[0]	PM_P112UN_EN	1	R/W	1'h0	VDD12P1 UnderVoltage Power Monitor Enable, 0: Disable, 1: Enable
0x011F	[7]	reserved	8	-	-	-
	[6]	REM_INTN1_MODE0_PE	1	R/W	1'h1	REM_INTN1_MODE0 IO Pull-down enable, 0: Disable, 1: Enable
	[5]	REM_INTN0_RXLANE_PE	1	R/W	1'h1	REM_INTN0_RXLANE IO Pull-down enable, 0: Disable, 1: Enable
	[4]	INTN_PE	1	R/W	1'h0	INTN IO Pull-down enable, 0: Disable, 1: Enable
	[3]	AIN_PE	1	R/W	1'h1	AIN IO Pull-down enable, 0: Disable, 1: Enable
	[2]	BCMONP_OEN_PE	1	R/W	1'h1	BCMONP_OEN IO Pull-down enable, 0: Disable, 1: Enable
	[1]	BCMONN_MODE1_PE	1	R/W	1'h1	BCMONN_MODE1 IO Pull-down enable, 0: Disable, 1: Enable
	[0]	REFCLK_PE	1	R/W	1'h1	REFCLK IO Pull-down enable, 0: Disable, 1: Enable

Address	bit	Register Name	width	R/W	Init	Description
0x0120	[7:2]	reserved	8	-	-	-
	[1]	MON1_PE	1	R/W	1'h1	MON1 IO Pull-down enable, 0: Disable, 1: Enable
	[0]	MON0_PE	1	R/W	1'h1	MON0 IO Pull-down enable, 0: Disable, 1: Enable
0x0121	[7:0]	reserved	8	-	-	-
0x0122	[7:0]	reserved	8	-	-	-
0x0123	[7:4]	reserved	4	-	-	-
	[3:0]	MODE_SET	4	RO	-	It can read operation mode number.
0x0124	[7:0]	reserved	8	-	-	-
0x0125	[7:5]	reserved	3	-	-	-
	[4]	THRIO_VALID_L1	1	RO	-	VbyOneHSII FC/BC Link status for lane1 0x0: Not ready, Unlock 0x1: Ready, Lock
	[3:1]	reserved	3	-	-	-
	[0]	THRIO_VALID_L0	1	RO	-	VbyOneHSII FC/BC Link status for lane0 0x0: Not ready, Unlock 0x1: Ready, Lock
0x0126	[7:1]	reserved	7	-	-	-
	[0]	LINK_NUM	1	R/W	1'h0	VbyOneHSII FC/BC Link THRIO Number, 0: 1Lane, 1: 2Lane
0x01F0	[7:0]	ID0	8	R	8'h74	ID code "t"
0x01F1	[7:0]	ID1	8	R	8'h68	ID code "h"
0x01F2	[7:0]	ID2	8	R	8'h63	ID code "c"
0x01F3	[7:0]	ID3	8	R	8'h76	ID code "v"
0x01F4	[7:0]	ID4	8	R	8'h33	ID code "3"
0x01F5	[7:0]	ID5	8	R	8'h35	ID code "5"
0x01F6	[7:0]	ID6	8	R	8'h33	ID code "3"
0x01F7	[7:0]	ID7	8	R	8'h00	ID code " "

Address	bit	Register Name	width	R/W	Init	Description
0x0290	[7:0]	reserved	8	-	-	-
0x0291	[7:6]	reserved	2	-	-	-
	[5:0]	FPLL0_REFDIV	6	R/W	6'h3	<this regiseter is valid only when 0x0298[0]=1> PLL Reference Diver setting. Must be not set 0x0.
0x0292	[7:4]	reserved	4	-	-	-
	[3:0]	FPLL0_INTIN_1	4	R/W	4'h0	<this regiseter is valid only when 0x0298[0]=1> PLL Feedback Divider integer part setting [11:8].
0x0293	[7:0]	FPLL0_INTIN_0	8	R/W	8'h18	<this regiseter is valid only when 0x0298[0]=1> PLL Feedback Divider integer part setting [7:0]. Only valid; Use interger: d'16~320 Use fractional: d'20~160
0x0294	[7:0]	FPLL0_FRACIN_2	8	R/W	8'h0	<this regiseter is valid only when 0x0298[0]=1> PLL Feedback Divider fractional part setting [23:16].
0x0295	[7:0]	FPLL0_FRACIN_1	8	R/W	8'h0	<this regiseter is valid only when 0x0298[0]=1> PLL Feedback Divider fractional part setting [15:8].
0x0296	[7:0]	FPLL0_FRACIN_0	8	R/W	8'h0	<this regiseter is valid only when 0x0298[0]=1> PLL Feedback Divider fractional part setting [7:0].
0x0297	[7]	reserved	1	-	-	-
	[6:4]	FPLL0_POSTDIV2	3	R/W	3'h1	<this regiseter is valid only when 0x0298[0]=1> PLL 2nd Post Divider setting.
	[3]	reserved	1	-	-	-
	[2:0]	FPLL0_POSTDIV1	3	R/W	3'h7	<this regiseter is valid only when 0x0298[0]=1> PLL 1nd Post Divider setting. POSTDIV1 value ≧POSTDIV2 value
0x0298	[7:1]	reserved	7	-	-	-
	[0]	FPLL0_DIRECTMODE	1	R/W	1'h0	PLL Manual setting enable 0x0: PLL auto configuration mode 0x1: Manual setting enable
0x02A0	[7:0]	reserved	8	-	-	-
0x02A1	[7:6]	reserved	2	-	-	-
	[5:0]	FPLL1_REFDIV	6	R/W	6'h3	<this regiseter is valid only when 0x0298[0]=1> PLL Reference Diver setting. Must be not set 0x0.
0x02A2	[7:4]	reserved	4	-	-	-
	[3:0]	FPLL1_INTIN_1	4	R/W	4'h0	<this regiseter is valid only when 0x0298[0]=1> PLL Feedback Divider integer part setting [11:8].
0x02A3	[7:0]	FPLL1_INTIN_0	8	R/W	8'h18	<this regiseter is valid only when 0x0298[0]=1> PLL Feedback Divider integer part setting [7:0]. Only valid; Use interger: d'16~320 Use fractional: d'20~160
0x02A4	[7:0]	FPLL1_FRACIN_2	8	R/W	8'h0	<this regiseter is valid only when 0x0298[0]=1> PLL Feedback Divider fractional part setting [23:16].
0x02A5	[7:0]	FPLL1_FRACIN_1	8	R/W	8'h0	<this regiseter is valid only when 0x0298[0]=1> PLL Feedback Divider fractional part setting [15:8].
0x02A6	[7:0]	FPLL1_FRACIN_0	8	R/W	8'h0	<this regiseter is valid only when 0x0298[0]=1> PLL Feedback Divider fractional part setting [7:0].
0x02A7	[7]	reserved	1	-	-	-
	[6:4]	FPLL1_POSTDIV2	3	R/W	3'h1	<this regiseter is valid only when 0x0298[0]=1> PLL 2nd Post Divider setting.
	[3]	reserved	1	-	-	-
	[2:0]	FPLL1_POSTDIV1	3	R/W	3'h7	<this regiseter is valid only when 0x0298[0]=1> PLL 1nd Post Divider setting. POSTDIV1 value ≧POSTDIV2 value
0x02A8	[7:1]	reserved	7	-	-	-
	[0]	FPLL1_DIRECTMODE	1	R/W	1'h0	PLL Manual setting enable 0x0: PLL auto configuration mode 0x1: Manual setting enable

Address	bit	Register Name	width	R/W	Init	Description
0x02B0	[7:4]	reserved	4	-	-	-
	[3:0]	FPLL0_DIVVAL	4	R/W	4'hC	<this regiseter is valid only when 0x02C3[0]=0> SSCG modulation frequency setting. Must be not set 0x0. FMOD = PCLK / (DIVVAL*128) ≦ 30kHz
0x02B1	[7:5]	reserved	3	-	-	-
	[4:0]	FPLL0_SPREAD	5	R/W	5'h3	<this regiseter is valid only when 0x02C3[0]=0> SSCG modulation depth select setting 0x0: 0% 0x1: 0.1% 0x2: 0.2% 0x3: 0.3% 0x4: 0.4% 0x5: 0.5% others: Reserved
0x02B2	[7:1]	reserved	7	-	-	-
	[0]	FPLL0_DOWNSPREAD	1	R/W	1'h0	<this regiseter is valid only when 0x02C3[0]=0> Spread mode select setting 0x0: Center Spread 0x1: Down Spread
0x02B3	[7:1]	reserved	7	-	-	-
	[0]	FPLL0_DISABLE_SSCG	1	R/W	1'h1	SSCG enable setting 0x0: Enable 0x1: Disable
0x02C0	[7:4]	reserved	4	-	-	-
	[3:0]	FPLL1_DIVVAL	4	R/W	4'hC	<this regiseter is valid only when 0x02C3[0]=0> SSCG modulation frequency setting. Must be not set 0x0. FMOD = PCLK / (DIVVAL*128) ≦ 30kHz
0x02C1	[7:5]	reserved	3	-	-	-
	[4:0]	FPLL1_SPREAD	5	R/W	5'h3	<this regiseter is valid only when 0x02C3[0]=0> SSCG modulation depth select setting 0x0: 0% 0x1: 0.1% 0x2: 0.2% 0x3: 0.3% 0x4: 0.4% 0x5: 0.5% others: Reserved
0x02C2	[7:1]	reserved	7	-	-	-
	[0]	FPLL1_DOWNSPREAD	1	R/W	1'h0	<this regiseter is valid only when 0x02C3[0]=0> Spread mode select setting 0x0: Center Spread 0x1: Down Spread
0x02C3	[7:1]	reserved	7	-	-	-
	[0]	FPLL1_DISABLE_SSCG	1	R/W	1'h1	SSCG enable setting 0x0: Enable 0x1: Disable

Address	bit	Register Name	width	R/W	Init	Description
0x0400	[7:0]	reserved	8	-	-	-
0x0401	[7:0]	reserved	8	-	-	-
0x0402	[7:0]	reserved	8	-	-	-
0x0403	[7:0]	reserved	8	-	-	-
0x0404	[7:0]	reserved	8	-	-	-
0x0405	[7:0]	reserved	8	-	-	-
0x0406	[7:5]	reserved	3	-	-	-
	[4:0]	THSSETTLE_P0	5	R/W	5'h6	DSI Grobal Timing Setting parameter for port0 THS-SETTLE (Preliminary value) 0x05: Over 1000Mbps/lane 0x06: 400 to 1000Mbps/lane 0x07: 250 to 400Mbps/lane 0x08 160 to 250Mbps/lane 0x09 130 to 160Mbps/lane 0x0B 90 to 130Mbps/lane 0x0C 80 to 90Mbps/lane
0x0407	[7:5]	reserved	3	-	-	-
	[4:0]	TCSETTLE_P0	5	R/W	5'h7	DSI Grobal Timing Setting parameter for port0 TCLK-SETTLE (Preliminary value) Must be set 0x07
0x0408	[7:0]	reserved	8	-	-	-
0x0409	[7:0]	reserved	8	-	-	-
0x040A	[7:0]	reserved	8	-	-	-
0x040B	[7:0]	reserved	8	-	-	-
0x040C	[7:0]	reserved	8	-	-	-
0x040D	[7:0]	reserved	8	-	-	-
0x040E	[7:0]	reserved	8	-	-	-
0x040F	[7:0]	reserved	8	-	-	-
0x0410	[7:0]	reserved	8	-	-	-
0x0411	[7:0]	reserved	8	-	-	-
0x0412	[7:0]	reserved	8	-	-	-
0x0413	[7:0]	reserved	8	-	-	-
0x0414	[7:0]	reserved	8	-	-	-
0x0415	[7:0]	reserved	8	-	-	-
0x0416	[7:0]	reserved	8	-	-	-
0x0417	[7:0]	reserved	8	-	-	-
0x0418	[7:0]	reserved	8	-	-	-
0x0419	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0500	[7:0]	reserved	8	-	-	-
0x0501	[7:0]	reserved	8	-	-	-
0x0502	[7:0]	reserved	8	-	-	-
0x0503	[7:0]	reserved	8	-	-	-
0x0504	[7:0]	reserved	8	-	-	-
0x0505	[7:0]	reserved	8	-	-	-
0x0506	[7:5]	reserved	3	-	-	-
	[4:0]	THSSETTLE_P1	5	R/W	5'h6	DSI Grobal Timing Setting parameter for port1 THS-SETTLE (Preliminary value) 0x05: Over 1000Mbps/lane 0x06: 400 to 1000Mbps/lane 0x07: 250 to 400Mbps/lane 0x08 160 to 250Mbps/lane 0x09 130 to 160Mbps/lane 0x0B 90 to 130Mbps/lane 0x0C 80 to 90Mbps/lane
0x0507	[7:5]	reserved	3	-	-	-
	[4:0]	TCSETTLE_P1	5	R/W	5'h7	DSI Grobal Timing Setting parameter for port1 TCLK-SETTLE (Preliminary value) Must be set 0x07
0x0508	[7:0]	reserved	8	-	-	-
0x0509	[7:0]	reserved	8	-	-	-
0x050A	[7:0]	reserved	8	-	-	-
0x050B	[7:0]	reserved	8	-	-	-
0x050C	[7:0]	reserved	8	-	-	-
0x050D	[7:0]	reserved	8	-	-	-
0x050E	[7:0]	reserved	8	-	-	-
0x050F	[7:0]	reserved	8	-	-	-
0x0510	[7:0]	reserved	8	-	-	-
0x0511	[7:0]	reserved	8	-	-	-
0x0512	[7:0]	reserved	8	-	-	-
0x0513	[7:0]	reserved	8	-	-	-
0x0514	[7:0]	reserved	8	-	-	-
0x0515	[7:0]	reserved	8	-	-	-
0x0516	[7:0]	reserved	8	-	-	-
0x0517	[7:0]	reserved	8	-	-	-
0x0518	[7:0]	reserved	8	-	-	-
0x0519	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0600	[7:1]	reserved	7	-	-	-
	[0]	DUMMY_DE	1	R/W	1'h0	Dummy DE Enable 0 : disable / 1: enable
0x0601	[7:1]	reserved	7	-	-	-
	[0]	PRE_DE_EN	1	R/W	1'h1	PRE_DE Enable 0:Disable 1:Enable
0x0602	[7:6]	reserved	2	-	-	-
	[5:0]	PRE_DE_POSITION_L0	6	R/W	0d40	Pre DE Position 0d8 : 8 cycle before DE 0d16 : 16 cycle before DE PRE_DE_POSITION must be a multiple of 8. PRE_DE_POSITION must be < 127.
0x0603	[7:6]	reserved	2	-	-	-
	[5:0]	PRE_DE_POSITION_L1	6	R/W	0d40	Pre DE Position 0d8 : 8 cycle before DE 0d16 : 16 cycle before DE PRE_DE_POSITION must be a multiple of 8. PRE_DE_POSITION must be < 127.
0x0604	[7:6]	reserved	2	-	-	-
	[5:0]	RP_DELAY_L0	6	R/W	0d48	Pre DE Position
0x0605	[7:6]	reserved	2	-	-	-
	[5:0]	RP_DELAY_L1	6	R/W	0d48	Pre DE Position
0x0606	[7:0]	reserved	8	-	-	-
0x0607	[7:0]	reserved	8	-	-	-
0x0608	[7:1]	reserved	7	-	-	-
	[0]	ITU709	1	R/W	1'h0	RGB to YUV Conversion Setting 0:ITU-R BT.601 1:ITU-R BT.709

Address	bit	Register Name	width	R/W	Init	Description
0x0640	[7:1]	reserved	7	-	-	-
	[0]	PATGENEN_P0	1	R/W	1'h0	Pattern Generator Enable setting for port0. 0x0: Disable, 0x1: Enable Need to set enable for internal oscillator operation mode.
0x0641	[7:1]	reserved	7	-	-	-
	[0]	LANESEL_P0	1	R/W	1'h0	Pattern Generator lane setting. 0x0: Set when DSI is Single link. 0x1: Set when DSI is Dual link.
0x0642	[7:4]	reserved	4	-	-	-
	[3:0]	HACTIVE_UPPER_P0	4	R/W	4'h7	H active period [11:8]. ([pixel])
0x0643	[7:0]	HACTIVE_LOWER_P0	8	R/W	8'h80	H active period [7:0]. ([pixel]) Default value is 1920 pixels.
0x0644	[7:3]	reserved	5	-	-	-
	[2:0]	VACTIVE_UPPER_P0	3	R/W	3'h4	V active period [10:8]. ([line])
0x0645	[7:0]	VACTIVE_LOWER_P0	8	R/W	8'h38	V active period [7:0]. ([line]) Default value is 1080 lines. If this setting is odd value, will automatically add 1 lines.
0x0646	[7:4]	reserved	4	-	-	-
	[3:0]	HBLANK_UPPER_P0	4	R/W	4'h1	H blank period [11:8]. ([pixel])
0x0647	[7:0]	HBLANK_LOWER_P0	8	R/W	8'h18	H blank period [7:0]. ([pixel]) Default value is 280 pixels.
0x0648	[7:2]	reserved	6	-	-	-
	[1:0]	VBLANK_UPPER_P0	2	R/W	2'h0	V blank period [9:8]. ([line])
0x0649	[7:0]	VBLANK_LOWER_P0	8	R/W	8'h2D	V blank period [7:0]. ([line]) Default value is 45 lines.
0x064A	[7:1]	reserved	7	-	-	-
	[0]	HSYNCWIDTH_UPPER_P0	1	R/W	1'h0	H active pluse width [8]. ([pixel])
0x064B	[7:0]	HSYNCWIDTH_LOWER_P0	8	R/W	8'h2C	H active pluse width [7:0]. ([pixel]) Default value is 44 pixels.
0x064C	[7:0]	VSYNCWIDTH_P0	8	R/W	8'h5	V active pluse width [7:0]. ([line]) Default value is 5 lines.
0x064D	[7:1]	reserved	7	-	-	-
	[0]	HBACKPORCH_UPPER_P0	1	R/W	1'h0	H back portch period [8]. ([pixel])
0x064E	[7:0]	HBACKPORCH_LOWER_P0	8	R/W	8'h94	H back portch period [7:0]. ([pixel]) Default value is 148 pixels.
0x064F	[7]	reserved	1	-	-	-
	[6:0]	VBACKPORCH_P0	7	R/W	7'h24	V back porch period [6:0]. ([line]) Default value is 36 lines.
0x0650	[7:0]	reserved	8	-	-	-
0x0651	[7:0]	reserved	8	-	-	-
0x0652	[7:0]	reserved	8	-	-	-
0x0653	[7:0]	reserved	8	-	-	-
0x0654	[7:0]	reserved	8	-	-	-
0x0655	[7:0]	reserved	8	-	-	-
0x0656	[7:1]	reserved	7	-	-	-
	[0]	HSYNCDIS_P0	1	R/W	1'h0	Generate HSYNC setting 0x0: Generate Hsync 0x1: Not generate Hsync
0x0657	[7:5]	reserved	3	-	-	-
	[4]	VSYNCPOL_P0	1	R/W	1'h1	VSYNC polality setting 0x0: Active low, idle high. 0x1: Active high, idle low.
	[3:1]	reserved	3	-	-	-
	[0]	HSYNCPOL_P0	1	R/W	1'h1	HSYNC polality setting 0x0: Active low, idle high. 0x1: Active high, idle low.

Address	bit	Register Name	width	R/W	Init	Description
0x0658	[7:6]	reserved	2	-	-	-
	[5:0]	PATGEN_PTN_P0	6	R/W	6'hB	Pattern select setting. 0x0: Automatic pattern switching repetition from 0x1 to 0xE. 0x1: White Raster 0x2: Black Raster 0x3: Red Raster 0x4: Green Raster 0x5: Blue Raster 0x6: Horizontal Clolor Bars 0x7: Vertical Clolor Bars 0x8: Horizontal Gray Ramp 0x9: Vertical Gray Ramp 0xA: Horizontal RGBW Ramp 0xB: Vertical RGBW Ramp 0xC: 16x16 Pixel Cheker 0xD: Frame 0xE: Sub Pixel Checker 0xF: Black Raster 0x10: Frame2 0x11: 4x1 Checker1 0x12: 4x1 Checker2 0x13: 2x1 Checker1 0x14: 2x1 Checker2 0x15: 1x1 Checker1 0x16: 1x1 Checker2 0x17: Cursor 0x18: CheckerA 0x19: CheckerB 0x1A: CheckerC 0x1B: Green Horizontal Stripe 0x1C: Green Vertical Stripe 0x1E: Frame3 0x1F: WindowA 0x20: WindowB 0x21: Dot pattern Others: Reserved
0x0659	[7:0]	GS_SEL_R_P0	8	R/W	8'hFF	Gradient Setting for Red. This register effects to the Raster, Color Bars and Dot Pattern. 00:Black <=> FF:Red
0x065A	[7:0]	GS_SEL_G_P0	8	R/W	8'hFF	Gradient Setting for Green. This register effects to the Raster, Color Bars and Dot Pattern. 00:Black <=> FF:Green
0x065B	[7:0]	GS_SEL_B_P0	8	R/W	8'hFF	Gradient Setting for Blue. This register effects to the Raster, Color Bars and Dot Pattern. 00:Black <=> FF:Blue
0x065C	[7:4]	reserved	4	-	-	-
	[3:0]	CURSOR_H_UPPER_P0	4	R/W	4'h3	Cursor position on horizontal direction [11:8]. This register effects to the cursor Pattern.
0x065D	[7:0]	CURSOR_H_LOWER_P0	8	R/W	8'hC0	Cursor position on horizontal direction [7:0]. This register effects to the cursor Pattern. Default value is 960 pixels.
0x065E	[7:4]	reserved	4	-	-	-
	[3:0]	CURSOR_V_UPPER_P0	4	R/W	4'h2	Cursor position on vertical direction [11:8]. This register effects to the cursor Pattern.
0x065F	[7:0]	CURSOR_V_LOWER_P0	8	R/W	8'h1C	Cursor position on vertical direction [7:0]. This register effects to the cursor Pattern. Default value is 540 lines.
0x0660	[7:4]	reserved	4	-	-	-
	[3:0]	DOT_H_UPPER_P0	4	R/W	4'h3	Dot position on horizontal direction [11:8]. This register effects to the cursor Pattern.
0x0661	[7:0]	DOT_H_LOWER_P0	8	R/W	8'hC0	Dot position on horizontal direction [7:0]. This register effects to the cursor Pattern. Default value is 960 pixels.
0x0662	[7:4]	reserved	4	-	-	-
	[3:0]	DOT_V_UPPER_P0	4	R/W	4'h2	Dot position on vertical direction [11:8]. This register effects to the cursor Pattern.
0x0663	[7:0]	DOT_V_LOWER_P0	8	R/W	8'h1C	Dot position on vertical direction [7:0]. This register effects to the cursor Pattern. Default value is 540 lines.
0x0664	[7:0]	DOT_COL_R_P0	8	R/W	8'hFF	Dot Gradient Setting for Red. This register effects to the Dot Pattern. 00:Black <=> FF:Red
0x0665	[7:0]	DOT_COL_G_P0	8	R/W	8'hFF	Dot Gradient Setting for Green. This register effects to the Dot Pattern. 00:Black <=> FF:Green
0x0666	[7:0]	DOT_COL_B_P0	8	R/W	8'hFF	Dot Gradient Setting for Blue. This register effects to the Dot Pattern. 00:Black <=> FF:Blue
0x0667	[7:1]	reserved	7	-	-	-
	[0]	DOT_INV_P0	1	R/W	1'h0	Invert Dot color setting. 0x0: Not invert, 0x1: Invert

Address	bit	Register Name	width	R/W	Init	Description
0x0680	[7:1]	reserved	7	-	-	-
	[0]	PATGENEN_P1	1	R/W	1'h0	Pattern Generator Enable setting for port1. 0x0: Disable, 0x1: Enable Need to set enable for internal oscillator operation mode.
0x0681	[7:1]	reserved	7	-	-	-
	[0]	LANESEL_P1	1	R/W	1'h0	Pattern Generator lane setting. 0x0: Set when DSI is Single link. 0x1: Set when DSI is Dual link.
0x0682	[7:4]	reserved	4	-	-	-
	[3:0]	HACTIVE_UPPER_P1	4	R/W	4'h7	H active period [11:8]. ([pixel])
0x0683	[7:0]	HACTIVE_LOWER_P1	8	R/W	8'h80	H active period [7:0]. ([pixel]) Default value is 1920 pixels.
0x0684	[7:3]	reserved	5	-	-	-
	[2:0]	VACTIVE_UPPER_P1	3	R/W	3'h4	V active period [10:8]. ([line])
0x0685	[7:0]	VACTIVE_LOWER_P1	8	R/W	8'h38	V active period [7:0]. ([line]) Default value is 1080 lines. If this setting is odd value, will automatically add 1 lines.
0x0686	[7:4]	reserved	4	-	-	-
	[3:0]	HBLANK_UPPER_P1	4	R/W	4'h1	H blank period [11:8]. ([pixel])
0x0687	[7:0]	HBLANK_LOWER_P1	8	R/W	8'h18	H blank period [7:0]. ([pixel]) Default value is 280 pixels.
0x0688	[7:2]	reserved	6	-	-	-
	[1:0]	VBLANK_UPPER_P1	2	R/W	2'h0	V blank period [9:8]. ([line])
0x0689	[7:0]	VBLANK_LOWER_P1	8	R/W	8'h2D	V blank period [7:0]. ([line]) Default value is 45 lines.
0x068A	[7:1]	reserved	7	-	-	-
	[0]	HSYNCWIDTH_UPPER_P1	1	R/W	1'h0	H active pluse width [8]. ([pixel])
0x068B	[7:0]	HSYNCWIDTH_LOWER_P1	8	R/W	8'h2C	H active pluse width [7:0]. ([pixel]) Default value is 44 pixels.
0x068C	[7:0]	VSYNCWIDTH_P1	8	R/W	8'h5	V active pluse width [7:0]. ([line]) Default value is 5 lines.
0x068D	[7:1]	reserved	7	-	-	-
	[0]	HBACKPORCH_UPPER_P1	1	R/W	1'h0	H back portch period [8]. ([pixel])
0x068E	[7:0]	HBACKPORCH_LOWER_P1	8	R/W	8'h94	H back portch period [7:0]. ([pixel]) Default value is 148 pixels.
0x068F	[7]	reserved	1	-	-	-
	[6:0]	VBACKPORCH_P1	7	R/W	7'h24	V back porch period [6:0]. ([line]) Default value is 36 lines.
0x0690	[7:0]	reserved	8	-	-	-
0x0691	[7:0]	reserved	8	-	-	-
0x0692	[7:0]	reserved	8	-	-	-
0x0693	[7:0]	reserved	8	-	-	-
0x0694	[7:0]	reserved	8	-	-	-
0x0695	[7:0]	reserved	8	-	-	-
0x0696	[7:1]	reserved	7	-	-	-
	[0]	HSYNCDIS_P1	1	R/W	1'h0	Generate HSYNC setting 0x0: Generate Hsync 0x1: Not generate Hsync
0x0697	[7:5]	reserved	3	-	-	-
	[4]	VSYNCPOL_P1	1	R/W	1'h1	VSYNC polality setting 0x0: Active low, idle high. 0x1: Active high, idle low.
	[3:1]	reserved	3	-	-	-
	[0]	HSYNCPOL_P1	1	R/W	1'h1	HSYNC polality setting 0x0: Active low, idle high. 0x1: Active high, idle low.

Address	bit	Register Name	width	R/W	Init	Description
0x0698	[7:6]	reserved	2	-	-	-
	[5:0]	PATGEN_PTN_P1	6	R/W	6'hB	Pattern select setting. 0x0: Automatic pattern switching repetition from 0x1 to 0xE. 0x1: White Raster 0x2: Black Raster 0x3: Red Raster 0x4: Green Raster 0x5: Blue Raster 0x6: Horizontal Clolor Bars 0x7: Vertical Clolor Bars 0x8: Horizontal Gray Ramp 0x9: Vertical Gray Ramp 0xA: Horizontal RGBW Ramp 0xB: Vertical RGBW Ramp 0xC: 16x16 Pixel Cheker 0xD: Frame 0xE: Sub Pixel Checker 0xF: Black Raster 0x10: Frame2 0x11: 4x1 Checker1 0x12: 4x1 Checker2 0x13: 2x1 Checker1 0x14: 2x1 Checker2 0x15: 1x1 Checker1 0x16: 1x1 Checker2 0x17: Cursor 0x18: CheckerA 0x19: CheckerB 0x1A: CheckerC 0x1B: Green Horizontal Stripe 0x1C: Green Vertical Stripe 0x1E: Frame3 0x1F: WindowA 0x20: WindowB 0x21: Dot pattern Others: Reserved
0x0699	[7:0]	GS_SEL_R_P1	8	R/W	8'hFF	Gradient Setting for Red. This register effects to the Raster, Color Bars and Dot Pattern. 00:Black <=> FF:Red
0x069A	[7:0]	GS_SEL_G_P1	8	R/W	8'hFF	Gradient Setting for Green. This register effects to the Raster, Color Bars and Dot Pattern. 00:Black <=> FF:Green
0x069B	[7:0]	GS_SEL_B_P1	8	R/W	8'hFF	Gradient Setting for Blue. This register effects to the Raster, Color Bars and Dot Pattern. 00:Black <=> FF:Blue
0x069C	[7:4]	reserved	4	-	-	-
	[3:0]	CURSOR_H_UPPER_P1	4	R/W	4'h3	Cursor position on horizontal direction [11:8]. This register effects to the cursor Pattern.
0x069D	[7:0]	CURSOR_H_LOWER_P1	8	R/W	8'hC0	Cursor position on horizontal direction [7:0]. This register effects to the cursor Pattern. Default value is 960 pixels.
0x069E	[7:4]	reserved	4	-	-	-
	[3:0]	CURSOR_V_UPPER_P1	4	R/W	4'h2	Cursor position on vertical direction [11:8]. This register effects to the cursor Pattern.
0x069F	[7:0]	CURSOR_V_LOWER_P1	8	R/W	8'h1C	Cursor position on vertical direction [7:0]. This register effects to the cursor Pattern. Default value is 540 lines.
0x06A0	[7:4]	reserved	4	-	-	-
	[3:0]	DOT_H_UPPER_P1	4	R/W	4'h3	Dot position on horizontal direction [11:8]. This register effects to the cursor Pattern.
0x06A1	[7:0]	DOT_H_LOWER_P1	8	R/W	8'hC0	Dot position on horizontal direction [7:0]. This register effects to the cursor Pattern. Default value is 960 pixels.
0x06A2	[7:4]	reserved	4	-	-	-
	[3:0]	DOT_V_UPPER_P1	4	R/W	4'h2	Dot position on vertical direction [11:8]. This register effects to the cursor Pattern.
0x06A3	[7:0]	DOT_V_LOWER_P1	8	R/W	8'h1C	Dot position on vertical direction [7:0]. This register effects to the cursor Pattern. Default value is 540 lines.
0x06A4	[7:0]	DOT_COL_R_P1	8	R/W	8'hFF	Dot Gradient Setting for Red. This register effects to the Dot Pattern. 00:Black <=> FF:Red
0x06A5	[7:0]	DOT_COL_G_P1	8	R/W	8'hFF	Dot Gradient Setting for Green. This register effects to the Dot Pattern. 00:Black <=> FF:Green
0x06A6	[7:0]	DOT_COL_B_P1	8	R/W	8'hFF	Dot Gradient Setting for Blue. This register effects to the Dot Pattern. 00:Black <=> FF:Blue
0x06A7	[7:1]	reserved	7	-	-	-
	[0]	DOT_INV_P1	1	R/W	1'h0	Invert Dot color setting. 0x0: Not invert, 0x1: Invert

Address	bit	Register Name	width	R/W	Init	Description
0x0800	[7:0]	R_READ_DELAY0_L	8	R/W	8'h64	FC Port0 Read Delay Lower bits
0x0801	[7:5]	reserved	3	-	-	-
	[4:0]	R_READ_DELAY0_U	5	R/W	5'h00	FC Port0 Read Delay Upper bits
0x0802	[7:0]	R_READ_DELAY1_L	8	R/W	8'h64	FC Port1 Read Delay Lower bits
0x0803	[7:5]	reserved	3	-	-	-
	[4:0]	R_READ_DELAY1_U	5	R/W	5'h00	FC Port1 Read Delay Upper bits
0x0804	[7:0]	reserved	8	-	-	-
0x0805	[7:0]	reserved	8	-	-	-
0x0806	[7:0]	reserved	8	-	-	-
0x0807	[7:0]	reserved	8	-	-	-
0x0808	[7:0]	R_CROP_HACTIVE_L	8	R/W	8'h00	Crop Hactive Lower bits
0x0809	[7:5]	reserved	3	-	-	-
	[4:0]	R_CROP_HACTIVE_U	5	R/W	5'h00	Crop Hactive Upper bits
0x080A	[7:0]	R_CROP_VACTIVE_L	8	R/W	8'h00	Crop Vactive Lower bits
0x080B	[7:5]	reserved	3	-	-	-
	[4:0]	R_CROP_VACTIVE_U	5	R/W	5'h00	Crop Vactive Upper bits
0x080C	[7:3]	reserved	5	-	-	-
	[2:0]	R_SYNCGEN_MODE	3	R/W	3'h0	SYNC Generation method select 0x0:DSI input VSS and HSS with Vsync/Hsync width register setting 0x1:DSI input VSS, VSE, HSS and WC (no register setting) 0x2:DSI input VSS with Vsync/Hsync related registers setting 0x3:DSI input VSS, VSE, HSS and HSE (no register setting) Others:reserved
0x080D	[7:1]	reserved	7	-	-	-
	[0]	R_VSYNC_POL	1	R/W	1'h0	Vsync active polarity 0x0: Low active 0x1: High active
0x080E	[7:1]	reserved	7	-	-	-
	[0]	R_HSYNC_POL	1	R/W	1'h0	Hsync active polarity 0x0: Low active 0x1: High active
0x080F	[7:0]	R_HTOTAL0_L	8	R/W	8'h98	Horizontal Total[7:0] (pixel) lower 8bit for DSI port0 default: Htotal[11:0]=0d2200 pixels
0x0810	[7:4]	reserved	4	-	-	-
	[3:0]	R_HTOTAL0_U	4	R/W	4'h8	Horizontal Total[11:8] (pixel) upper 4bit for DSI port0 default: Htotal[11:0]=0d2200 pixels
0x0811	[7:0]	R_HSYNC_WIDTH0	8	R/W	8'h14	Hsync width (pixel) for DSI port0 default: Hsync[7:0]=0d20 pixels
0x0812	[7:0]	R_HBACK_PORCH0	8	R/W	8'h8C	Horizontal Back Porch (pixel) for DSI port0 default: HBackPorch[7:0]=0d140 pixels
0x0813	[7:0]	R_VSYNC_WIDTH0	8	R/W	8'h02	Vsync width (line) for DSI port0 default: Vsync[7:0]=0d02 lines
0x0814	[7:0]	R_VACTIVE_LINE0_L	8	R/W	8'h38	Vertical Active[7:0] (line) lower 8bit for DSI port0 default: Vactive[15:0]=0d1080 lines
0x0815	[7:0]	R_VACTIVE_LINE0_U	8	R/W	8'h04	Vertical Active[7:0] (line) upper 8bit for DSI port0 default: Vactive[15:0]=0d1080 lines
0x0816	[7:0]	R_VBLANK_LINE0	8	R/W	8'h2D	Vblank (line) for DSI port0 default: Vblank[7:0]=0d45 lines
0x0817	[7:0]	R_HTOTAL1_L	8	R/W	8'h98	Horizontal Total[7:0] (pixel) lower 8bit for DSI port1 default: Htotal[11:0]=0d2200 pixels
0x0818	[7:4]	reserved	4	-	-	-
	[3:0]	R_HTOTAL1_U	4	R/W	4'h8	Horizontal Total[11:8] (pixel) upper 4bit for DSI port1 default: Htotal[11:0]=0d2200 pixels
0x0819	[7:0]	R_HSYNC_WIDTH1	8	R/W	8'h14	Hsync width (pixel) for DSI port1 default: Hsync[7:0]=0d20 pixels
0x081A	[7:0]	R_HBACK_PORCH1	8	R/W	8'h8C	Horizontal Back Porch (pixel) for DSI port1 default: HBackPorch[7:0]=0d140 pixels
0x081B	[7:0]	R_VSYNC_WIDTH1	8	R/W	8'h02	Vsync width (line) for DSI port1 default: Vsync[7:0]=0d02 lines
0x081C	[7:0]	R_VACTIVE_LINE1_L	8	R/W	8'h38	Vertical Active[7:0] (line) lower 8bit for DSI port1 default: Vactive[15:0]=0d1080 lines
0x081D	[7:0]	R_VACTIVE_LINE1_U	8	R/W	8'h04	Vertical Active[7:0] (line) upper 8bit for DSI port1 default: Vactive[15:0]=0d1080 lines
0x081E	[7:0]	R_VBLANK_LINE1	8	R/W	8'h2D	Vblank (line) for DSI port1 default: Vblank[7:0]=0d45 lines
0x081F	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0900	[7:1]	reserved	7	-	-	-
	[0]	BC_XEYE_LSEL_L0	1	R/W	1'h0	BC Eye Jitter Monitor lane select. 0x0: Lane0. 0x1: reserved
0x0901	[7:1]	reserved	7	-	-	-
	[0]	BC_XEYE_EN_L0	1	W	1'h0	BC Eye Jitter Monitor Enable (1shot). 0x1: Enable (1shot).
0x0902	[7:1]	reserved	7	-	-	-
	[0]	BC_XEYE_CLR_L0	1	W	1'h0	BC Eye Jitter Monitor Clear. 0x1: Clear.
0x0903	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE0_L0	6	R	-	BC Eye Jitter Monitor Result
0x0904	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE1_L0	6	R	-	BC Eye Jitter Monitor Result
0x0905	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE2_L0	6	R	-	BC Eye Jitter Monitor Result
0x0906	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE3_L0	6	R	-	BC Eye Jitter Monitor Result
0x0907	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE4_L0	6	R	-	BC Eye Jitter Monitor Result
0x0908	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE5_L0	6	R	-	BC Eye Jitter Monitor Result
0x0909	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE6_L0	6	R	-	BC Eye Jitter Monitor Result
0x090A	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE7_L0	6	R	-	BC Eye Jitter Monitor Result
0x090B	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE8_L0	6	R	-	BC Eye Jitter Monitor Result
0x090C	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE9_L0	6	R	-	BC Eye Jitter Monitor Result
0x090D	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE10_L0	6	R	-	BC Eye Jitter Monitor Result
0x090E	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE11_L0	6	R	-	BC Eye Jitter Monitor Result
0x090F	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE12_L0	6	R	-	BC Eye Jitter Monitor Result
0x0910	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE13_L0	6	R	-	BC Eye Jitter Monitor Result
0x0911	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE14_L0	6	R	-	BC Eye Jitter Monitor Result
0x0912	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE15_L0	6	R	-	BC Eye Jitter Monitor Result
0x0913	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE16_L0	6	R	-	BC Eye Jitter Monitor Result
0x0914	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE17_L0	6	R	-	BC Eye Jitter Monitor Result
0x0915	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE18_L0	6	R	-	BC Eye Jitter Monitor Result
0x0916	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE19_L0	6	R	-	BC Eye Jitter Monitor Result
0x0917	[7:0]	reserved	8	-	-	-
0x0918	[7:0]	reserved	8	-	-	-
0x0919	[7:0]	reserved	8	-	-	-
0x091A	[7:4]	reserved	4	-	-	-
	[3:0]	FILTSEL_L0	4	R/W	4'h0	VbyOneHSII BC RX Filter setting for lane0. (Preliminary value) 0x0: Set when VbyOneHSII FC rate 1.6Gbps to 4.0Gbps 0x8: Set when VbyOneHSII FC rate 1.0Gbps to 1.6Gbps Other: Reserved
0x091B	[7:0]	reserved	8	-	-	-
0x091C	[7:0]	reserved	8	-	-	-
0x091D	[7:0]	reserved	8	-	-	-
0x091E	[7:0]	reserved	8	-	-	-
0x091F	[7:0]	reserved	8	-	-	-
0x0920	[7:0]	reserved	8	-	-	-
0x0921	[7:0]	reserved	8	-	-	-
0x0922	[7:0]	reserved	8	-	-	-
0x0923	[7:0]	reserved	8	-	-	-
0x0924	[7:0]	reserved	8	-	-	-
0x0925	[7:0]	reserved	8	-	-	-
0x0926	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0A00	[7:1]	reserved	7	-	-	-
	[0]	BC_XEYE_LSEL_L1	1	R/W	1'h0	BC Eye Jitter Monitor lane select. 0x0: Lane1. 0x1: reserved
0x0A01	[7:1]	reserved	7	-	-	-
	[0]	BC_XEYE_EN_L1	1	W	1'h0	BC Eye Jitter Monitor Enable (1shot). 0x1: Enable (1shot).
0x0A02	[7:1]	reserved	7	-	-	-
	[0]	BC_XEYE_CLR_L1	1	W	1'h0	BC Eye Jitter Monitor Clear. 0x1: Clear.
0x0A03	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE0_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A04	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE1_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A05	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE2_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A06	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE3_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A07	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE4_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A08	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE5_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A09	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE6_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A0A	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE7_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A0B	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE8_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A0C	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE9_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A0D	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE10_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A0E	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE11_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A0F	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE12_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A10	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE13_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A11	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE14_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A12	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE15_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A13	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE16_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A14	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE17_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A15	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE18_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A16	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE19_L1	6	R	-	BC Eye Jitter Monitor Result
0x0A17	[7:0]	reserved	8	-	-	-
0x0A18	[7:0]	reserved	8	-	-	-
0x0A19	[7:0]	reserved	8	-	-	-
0x0A1A	[7:4]	reserved	4	-	-	-
	[3:0]	FILTSEL_L1	4	R/W	4'h0	VbyOneHSII BC RX Filter setting for lane1. (Preliminary value) 0x0: Set when VbyOneHSII FC rate 1.6Gbps to 4.0Gbps 0x8: Set when VbyOneHSII FC rate 1.0Gbps to 1.6Gbps Other: Reserved
0x0A1B	[7:0]	reserved	8	-	-	-
0x0A1C	[7:0]	reserved	8	-	-	-
0x0A1D	[7:0]	reserved	8	-	-	-
0x0A1E	[7:0]	reserved	8	-	-	-
0x0A1F	[7:0]	reserved	8	-	-	-
0x0A20	[7:0]	reserved	8	-	-	-
0x0A21	[7:0]	reserved	8	-	-	-
0x0A22	[7:0]	reserved	8	-	-	-
0x0A23	[7:0]	reserved	8	-	-	-
0x0A24	[7:0]	reserved	8	-	-	-
0x0A25	[7:0]	reserved	8	-	-	-
0x0A26	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0B00	[7:2]	reserved	6	-	-	-
	[1:0]	R_2WIRE_PASS_MODE	2	R/W	2'h0	BCC 2-wire basic protocol setting as BCC Master. In BCC 2-wire Pass Through mode1, the specified device IDs are passed through. In BCC 2-wire Pass Through mode2, all device IDs are passed through by default. It can set IDs that are not pass through. In BCC 2-wire Set & Trigger mode, only 2-wire access to the THCV333 is performed to provide remote side register access. It does not require clock stretching, so may be used when the Host 2-write controller does not support clock stretching. 0x0: BCC 2-wire Pass Through mode1 (Address rename) 0x1: BCC 2-wire Pass Through mode2 (All pass through) 0x2: BCC 2-wire Set & Trigger mode 0x3: Reserved
0x0B04	[7:1]	reserved	7	-	-	-
	[0]	R_2WIRE_PASS_RESEND_EN	1	R/W	1'h0	BCC 2-wire retransmission Enable 0x0:Disable 0x1:Enable
0x0B08	[7:0]	R_2WIRE_PASS_L0_DES_ID	8	R/W	8'hEE	<this regiseters is valid only when 0x0B00=0x0, 0x2> Deserializer 2-wire Device ID for VbyOneHSIII Lane0. Default ID is 7'h77 [7:1]: 7bit ID [0] Reserved *It is not allowed the same ID with VbyOneHSIII lane1 (R_2WIRE_PASS_L1_DES_ID).
0x0B09	[7:0]	R_2WIRE_PASS_L1_DES_ID	8	R/W	8'hCA	<this regiseters is valid only when 0x0B00=0x0, 0x2> Deserializer 2-wire Device ID for VbyOneHSIII Lane1. Default ID is 7'h65 [7:1]: 7bit ID [0] Reserved *It is not allowed the same ID with VbyOneHSIII lane0 (R_2WIRE_PASS_L0_DES_ID).
0x0B0A	[7:0]	R_2WIRE_PASS_ADR_BYTE_NUM	8	R/W	8'h1	BCC 2-wire Pass Through Sub Address (Word Address) unit Byte number setting. 0x0: 1Byte Sub Address 0x1: 2Byte Sub Address ,,, 0x6: 7Byte Sub Address Others : Reserved [Setting Restriction for remote write is that Unit Address + Unit Data Byte must be at most 8Byte] (R_2WIRE_PASS_ADR_BYTE_NUM +1) + (R_2WIRE_PASS_DATA_BYTE_NUM +1) < 'd(8+1) [Setting Restriction for remote read is that Unit Address or Unit Data Byte must be at most 8Byte respectively] (R_2WIRE_PASS_ADR_BYTE_NUM +1)< 'd(8+1) (R_2WIRE_PASS_DATA_BYTE_NUM +1)< 'd(8+1)
0x0B0B	[7:0]	R_2WIRE_PASS_DATA_BYTE_NUM	8	R/W	8'h0	BCC 2-wire Pass Through Divided Write/Read Data unit Byte number setting. Larger unit Byte reduces transaction time of burst read/write operation. Unit Byte Number = R_2WIRE_PASS_DATA_BYTE_NUM +1 0x0: 1Byte Data 0x1: 2Byte Data ,,, 0x6: 7Byte Data 0x7: 8Byte Data Others : Reserved [Setting Restriction for remote w rite is that Unit Address + Unit Data Byte must be at most 8Byte] (R_2WIRE_PASS_ADR_BYTE_NUM +1) + (R_2WIRE_PASS_DATA_BYTE_NUM +1) < 'd(8+1) [Setting Restriction for remote read is that Unit Address or Unit Data Byte must be at most 8Byte respectively] (R_2WIRE_PASS_ADR_BYTE_NUM +1)< 'd(8+1) (R_2WIRE_PASS_DATA_BYTE_NUM +1)< 'd(8+1)

Address	bit	Register Name	width	R/W	Init	Description
0x0B10	[7:0]	R_2WIRE_PASS1_L0_IN_ID0	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "before rename ID0" of the attached to the remote Deselializer for BCC lane0. This ID will be renamed to "after renamed ID0" before passing the Deserializer. If "before rename ID0" and "after renamed ID0" are the same, the ID will not be renamed. [7:1] 7bit ID [0] Reserved
0x0B11	[7:0]	R_2WIRE_PASS1_L0_OUT_ID0	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "after renamed ID0" of the attached to the remote Deselializer for BCC lane0. [7:1] 7bit ID [0] Reserved
0x0B12	[7:0]	R_2WIRE_PASS1_L0_IN_ID1	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "before rename ID1" of the attached to the remote Deselializer for BCC lane0. This ID will be renamed to "after renamed ID1" before passing the Deserializer. If "before rename ID1" and "after renamed ID1" are the same, the ID will not be renamed. [7:1] 7bit ID [0] Reserved
0x0B13	[7:0]	R_2WIRE_PASS1_L0_OUT_ID1	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "after renamed ID1" of the attached to the remote Deselializer for BCC lane0. [7:1] 7bit ID [0] Reserved
0x0B14	[7:0]	R_2WIRE_PASS1_L0_IN_ID2	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "before rename ID2" of the attached to the remote Deselializer for BCC lane0. This ID will be renamed to "after renamed ID2" before passing the Deserializer. If "before rename ID2" and "after renamed ID2" are the same, the ID will not be renamed. [7:1] 7bit ID [0] Reserved
0x0B15	[7:0]	R_2WIRE_PASS1_L0_OUT_ID2	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "after renamed ID2" of the attached to the remote Deselializer for BCC lane0. [7:1] 7bit ID [0] Reserved
0x0B16	[7:0]	R_2WIRE_PASS1_L0_IN_ID3	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "before rename ID3" of the attached to the remote Deselializer for BCC lane0. This ID will be renamed to "after renamed ID3" before passing the Deserializer. If "before rename ID3" and "after renamed ID3" are the same, the ID will not be renamed. [7:1] 7bit ID [0] Reserved
0x0B17	[7:0]	R_2WIRE_PASS1_L0_OUT_ID3	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "after renamed ID3" of the attached to the remote Deselializer for BCC lane0. [7:1] 7bit ID [0] Reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0B18	[7:0]	R_2WIRE_PASS1_L1_IN_ID0	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "before rename ID0" of the attached to the remote Deselializer for BCC lane1. This ID will be renamed to "after renamed ID0" before passing the Deserializer. If "before rename ID0" and "after renamed ID0" are the same, the ID will not be renamed. [7:1] 7bit ID [0] Reserved * This ID is not allowed the same ID with the before rename IDX for lane0. If these are the same ID, will work only lane0.
0x0B19	[7:0]	R_2WIRE_PASS1_L1_OUT_ID0	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "after renamed ID0" of the attached to the remote Deselializer for BCC lane1. [7:1] 7bit ID [0] Reserved
0x0B1A	[7:0]	R_2WIRE_PASS1_L1_IN_ID1	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "before rename ID1" of the attached to the remote Deselializer for BCC lane1. This ID will be renamed to "after renamed ID1" before passing the Deserializer. If "before rename ID1" and "after renamed ID1" are the same, the ID will not be renamed. [7:1] 7bit ID [0] Reserved *This ID is not allowed the same ID with the before rename IDX for lane0. If these are the same ID, will work only lane0.
0x0B1B	[7:0]	R_2WIRE_PASS1_L1_OUT_ID1	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "after renamed ID1" of the attached to the remote Deselializer for BCC lane1. [7:1] 7bit ID [0] Reserved
0x0B1C	[7:0]	R_2WIRE_PASS1_L1_IN_ID2	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "before rename ID2" of the attached to the remote Deselializer for BCC lane1. This ID will be renamed to "after renamed ID2" before passing the Deserializer. If "before rename ID2" and "after renamed ID2" are the same, the ID will not be renamed. [7:1] 7bit ID [0] Reserved *This ID is not allowed the same ID with the before rename IDX for lane0. If these are the same ID, will work only lane0.
0x0B1D	[7:0]	R_2WIRE_PASS1_L1_OUT_ID2	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "after renamed ID2" of the attached to the remote Deselializer for BCC lane1. [7:1] 7bit ID [0] Reserved
0x0B1E	[7:0]	R_2WIRE_PASS1_L1_IN_ID3	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "before rename ID3" of the attached to the remote Deselializer for BCC lane1. This ID will be renamed to "after renamed ID3" before passing the Deserializer. If "before rename ID3" and "after renamed ID3" are the same, the ID will not be renamed. [7:1] 7bit ID [0] Reserved *This ID is not allowed the same ID with the before rename IDX for lane0. If these are the same ID, will work only lane0.
0x0B1F	[7:0]	R_2WIRE_PASS1_L1_OUT_ID3	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "after renamed ID3" of the attached to the remote Deselializer for BCC lane1. [7:1] 7bit ID [0] Reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0B24	[7:0]	R_2WIRE_PASS2_L0_BLOCK_ID0	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x1> This "Ignore ID0" will be not pass though in BCC 2-wire Pass Through mode2 (All Through) mode for VbyOneHSIII lane0. [7:1] 7bit ID [0]Reserved
0x0B25	[7:0]	R_2WIRE_PASS2_L0_BLOCK_ID1	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x1> This "Ignore ID1" will be not pass though in BCC 2-wire Pass Through mode2 (All Through) mode for VbyOneHSIII lane0. [7:1] 7bit ID [0]Reserved
0x0B26	[7:0]	R_2WIRE_PASS2_L0_BLOCK_ID2	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x1> This "Ignore ID2" will be not pass though in BCC 2-wire Pass Through mode2 (All Through) mode for VbyOneHSIII lane0. [7:1] 7bit ID [0]Reserved
0x0B27	[7:0]	R_2WIRE_PASS2_L0_BLOCK_ID3	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x1> This "Ignore ID3" will be not pass though in BCC 2-wire Pass Through mode2 (All Through) mode for VbyOneHSIII lane0. [7:1] 7bit ID [0]Reserved
0x0B28	[7:0]	R_2WIRE_PASS2_L1_BLOCK_ID0	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x1> This "Ignore ID0" will be not pass though in BCC 2-wire Pass Through mode2 (All Through) mode for VbyOneHSIII lane1. [7:1] 7bit ID [0]Reserved
0x0B29	[7:0]	R_2WIRE_PASS2_L1_BLOCK_ID1	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x1> This "Ignore ID1" will be not pass though in BCC 2-wire Pass Through mode2 (All Through) mode for VbyOneHSIII lane1. [7:1] 7bit ID [0]Reserved
0x0B2A	[7:0]	R_2WIRE_PASS2_L1_BLOCK_ID2	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x1> This "Ignore ID2" will be not pass though in BCC 2-wire Pass Through mode2 (All Through) mode for VbyOneHSIII lane1. [7:1] 7bit ID [0]Reserved
0x0B2B	[7:0]	R_2WIRE_PASS2_L1_BLOCK_ID3	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x1> This "Ignore ID3" will be not pass though in BCC 2-wire Pass Through mode2 (All Through) mode for VbyOneHSIII lane1. [7:1] 7bit ID [0]Reserved
0x0B2C	[7:0]	R_2WIRE_PASS2_LANE_SEL	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x1> BCC 2-wire Pass Through mode2 (All Through) mode Target VbyOneHSII lane select 0x0: lane0 0x1: lane1 Others: Reserved
0x0B30	[7:0]	R_2WIRE_SETTRIG_DATA0	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote WRITE DATA0 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B31	[7:0]	R_2WIRE_SETTRIG_DATA1	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote WRITE DATA1 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B32	[7:0]	R_2WIRE_SETTRIG_DATA2	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote WRITE DATA2 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B33	[7:0]	R_2WIRE_SETTRIG_DATA3	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote WRITE DATA3 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B34	[7:0]	R_2WIRE_SETTRIG_DATA4	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote WRITE DATA4 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B35	[7:0]	R_2WIRE_SETTRIG_DATA5	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote WRITE DATA5 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B36	[7:0]	R_2WIRE_SETTRIG_DATA6	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote WRITE DATA6 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B37	[7:0]	R_2WIRE_SETTRIG_DATA7	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote WRITE DATA7 in BCC 2-wire Set & Trigger mode [7:0] 8bit data

Address	bit	Register Name	width	R/W	Init	Description
0x0B38	[7:0]	R_2WIRE_SETTRIG_DEVID_WR	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> Target remote device address in BCC 2-wire Set & Trigger mode. [7:1] 7bit ID [0] read/write select 0x0: Write 0x1: Read
0x0B39	[7:0]	R_2WIRE_SETTRIG_START	8	W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> "Trigger" option in BCC 2-wire Set & Trigger mode. 0x01: 2-wire remote access start for "Write" and "Read with Sub-Address" for VbyOneHSII lane0 0x02: 2-wire remote access start for "Read without Sub-Address" for VbyOneHSII lane0 0x03: 2-wire remote access start for "Write" and "Read with Sub-Address" for VbyOneHSII lane1 0x04: 2-wire remote access start for "Read without Sub-Address" for VbyOneHSII lane1 Others: Reserved *It is not allowed to set 0x02 or 0x04 even when 0xB38[0]=0x0.
0x0B40	[7:0]	R_2WIRE_SETTRIG_RDATA0	8	R	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote READ DATA0 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B41	[7:0]	R_2WIRE_SETTRIG_RDATA1	8	R	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote READ DATA1 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B42	[7:0]	R_2WIRE_SETTRIG_RDATA2	8	R	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote READ DATA2 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B43	[7:0]	R_2WIRE_SETTRIG_RDATA3	8	R	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote READ DATA3 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B44	[7:0]	R_2WIRE_SETTRIG_RDATA4	8	R	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote READ DATA4 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B45	[7:0]	R_2WIRE_SETTRIG_RDATA5	8	R	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote READ DATA5 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B46	[7:0]	R_2WIRE_SETTRIG_RDATA6	8	R	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote READ DATA6 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B47	[7:0]	R_2WIRE_SETTRIG_RDATA7	8	R	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote READ DATA7 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B50	[7:0]	reserved	8	-	-	-
0x0B51	[7:0]	reserved	8	-	-	-
0x0B60	[7:0]	reserved	8	-	-	-
0x0B61	[7:0]	reserved	8	-	-	-
0x0B68	[7:0]	reserved	8	-	-	-
0x0B69	[7:0]	reserved	8	-	-	-
0x0B6A	[7:1]	reserved	7	-	-	-
	[0]	R_2WIRE_INTERMITTENT_MODE	1	R/W	1'h0	BCC 2-wire Non-divided write/read mode enable. Must be set the same mode with the BCC Slave (Deserializer) side. 0x0: Disable 0x1: Enable

Address	bit	Register Name	width	R/W	Init	Description
0x0C00	[7:6]	reserved	2	-	-	-
	[5]	GPIO0_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C00[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	GPIO0_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C00[2:0]=0x1, 0x7> GPIO0 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO0_MODE	3	R/W	3'h0	GPIO0 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programable GPO (To output GPIO0_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to GPIO0_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C01	[7:6]	reserved	2	-	-	-
	[5]	GPIO1_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C01[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	GPIO1_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C01[2:0]=0x1, 0x7> GPIO1 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO1_MODE	3	R/W	3'h0	GPIO1 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programable GPO (To output GPIO1_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to GPIO1_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C02	[7:6]	reserved	2	-	-	-
	[5]	I2SD2_GPIO2_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C02[2:0]=0x0, 0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	I2SD2_GPIO2_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C02[2:0]=0x1, 0x7> GPIO2 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	I2SD2_GPIO2_MODE	3	R/W	3'h2	I2SD2_GPIO2 I/O Mode setting. 0x0: I2SD2 input mode 0x1: Programable GPO (To output I2SD2_GPIO2_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI and Through GPI Mode 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to I2SD2_GPIO2_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C03	[7:6]	reserved	2	-	-	-
	[5]	I2SD3_GPIO3_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C03[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	I2SD3_GPIO3_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C03[2:0]=0x1, 0x7> GPIO3 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	I2SD3_GPIO3_MODE	3	R/W	3'h2	I2SD3_GPIO3 I/O Mode setting. 0x0: I2SD3 input mode 0x1: Programable GPO (To output I2SD3_GPIO3_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI and Through GPI Mode 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to I2SD3_GPIO3_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0C04	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	I2SD1_GPIO5_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C04[2:0]=0x1> GPIO5 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	I2SD1_GPIO5_MODE	3	R/W	3'h2	I2SD1_GPIO5 I/O Mode setting. 0x0: I2SD1 input mode 0x1: Programable GPO (To output I2SD1_GPIO5_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI Others: Reserved
0x0C05	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	I2SD0_GPIO6_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C05[2:0]=0x1> I2SD0_GPIO6 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	I2SD0_GPIO6_MODE	3	R/W	3'h2	I2SD0_GPIO6 I/O Mode setting. 0x0: I2S_D0 input mode 0x1: Programable GPO (To output GPIO6_REG_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI Others: Reserved
0x0C06	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	I2SWC_GPIO7_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C06[2:0]=0x1> I2SWC_GPIO7 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	I2SWC_GPIO7_MODE	3	R/W	3'h2	I2SWC_GPIO7 I/O Mode setting. 0x0: I2S_WC input mode 0x1: Programable GPO (To output GPIO7_REG_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI Others: Reserved
0x0C07	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	I2SCLK_GPIO8_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C07[2:0]=0x1> I2SCLK_GPIO8 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	I2SCLK_GPIO8_MODE	3	R/W	3'h2	I2SCLK_GPIO8 I/O Mode setting. 0x0: I2S_CLK input mode 0x1: Programable GPO (To output GPIO8_REG_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI Others: Reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0C08	[7:6]	reserved	2	-	-	-
	[5]	D_GPIO0_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C08[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	D_GPIO0_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C08[2:0]=0x1, 0x7> D_GPIO0 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	D_GPIO0_MODE	3	R/W	3'h0	D_GPIO0 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programable GPO (To output D_GPIO0_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to D_GPIO0_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C09	[7:6]	reserved	2	-	-	-
	[5]	D_GPIO1_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C09[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	D_GPIO1_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C09[2:0]=0x1, 0x7> D_GPIO1 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	D_GPIO1_MODE	3	R/W	3'h0	D_GPIO1 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programable GPO (To output D_GPIO1_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to D_GPIO1_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C0A	[7:6]	reserved	2	-	-	-
	[5]	D_GPIO2_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C0A[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	D_GPIO2_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C0A[2:0]=0x1, 0x7> D_GPIO2 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	D_GPIO2_MODE	3	R/W	3'h0	D_GPIO2 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programable GPO (To output D_GPIO2_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to D_GPIO2_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C0B	[7:6]	reserved	2	-	-	-
	[5]	D_GPIO3_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C0B[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	D_GPIO3_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C0B[2:0]=0x1, 0x7> D_GPIO3 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	D_GPIO3_MODE	3	R/W	3'h0	D_GPIO3 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programable GPO (To output D_GPIO3_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to D_GPIO3_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C0C	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0C0D	[7:1]	reserved	7	-	-	-
	[0]	GPIO0_IMON	1	R	1'h0	GPIO0 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C0E	[7:1]	reserved	7	-	-	-
	[0]	GPIO1_IMON	1	R	1'h0	GPIO1 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C0F	[7:1]	reserved	7	-	-	-
	[0]	GPIO2_IMON	1	R	1'h0	I2SD2_GPIO2 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C10	[7:1]	reserved	7	-	-	-
	[0]	GPIO3_IMON	1	R	1'h0	I2SD3_GPIO3 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C11	[7:1]	reserved	7	-	-	-
	[0]	GPIO5_IMON	1	R	1'h0	I2SD1_GPIO5 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C12	[7:1]	reserved	7	-	-	-
	[0]	GPIO6_IMON	1	R	1'h0	I2SD0_GPIO6 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C13	[7:1]	reserved	7	-	-	-
	[0]	GPIO7_IMON	1	R	1'h0	I2SWC_GPIO7 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C14	[7:1]	reserved	7	-	-	-
	[0]	GPIO8_IMON	1	R	1'h0	I2SWC_GPIO8 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C15	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO0_IMON	1	R	1'h0	D_GPIO0 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C16	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO1_IMON	1	R	1'h0	D_GPIO1 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C17	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO2_IMON	1	R	1'h0	D_GPIO2 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C18	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO3_IMON	1	R	1'h0	D_GPIO3 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C19	[7:0]	reserved	8	-	-	-
0x0C1A	[7:0]	reserved	8	-	-	-
0x0C1B	[7:0]	reserved	8	-	-	-
0x0C1C	[7:0]	reserved	8	-	-	-
0x0C1D	[7:0]	reserved	8	-	-	-
0x0C1E	[7:0]	reserved	8	-	-	-
0x0C1F	[7:0]	reserved	8	-	-	-
0x0C20	[7:0]	reserved	8	-	-	-
0x0C21	[7:0]	reserved	8	-	-	-
0x0C22	[7:0]	reserved	8	-	-	-
0x0C23	[7:0]	reserved	8	-	-	-
0x0C24	[7:0]	reserved	8	-	-	-
0x0C25	[7:0]	reserved	8	-	-	-
0x0C26	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0C27	[7:1]	reserved	7	-	-	-
	[0]	GPIO0_OD_MODE	1	R/W	1'h0	GPIO0 outpu buffer type select 0x0: Push pull, 0x1: Open drain
0x0C28	[7:1]	reserved	7	-	-	-
	[0]	GPIO1_OD_MODE	1	R/W	1'h0	GPIO1 outpu buffer type select 0x0: Push pull, 0x1: Open drain
0x0C29	[7:1]	reserved	7	-	-	-
	[0]	GPIO2_OD_MODE	1	R/W	1'h0	I2SD2_GPIO2 outpu buffer type select 0x0: Push pull, 0x1: Open drain
0x0C2A	[7:1]	reserved	7	-	-	-
	[0]	GPIO3_OD_MODE	1	R/W	1'h0	I2SD3_GPIO3 outpu buffer type select 0x0: Push pull, 0x1: Open drain
0x0C2B	[7:1]	reserved	7	-	-	-
	[0]	GPIO5_OD_MODE	1	R/W	1'h0	I2SD1_GPIO5 outpu buffer type select 0x0: Push pull, 0x1: Open drain
0x0C2C	[7:1]	reserved	7	-	-	-
	[0]	GPIO6_OD_MODE	1	R/W	1'h0	I2SD0_GPIO6 outpu buffer type select 0x0: Push pull, 0x1: Open drain
0x0C2D	[7:1]	reserved	7	-	-	-
	[0]	GPIO7_OD_MODE	1	R/W	1'h0	I2SWC_GPIO7 outpu buffer type select 0x0: Push pull, 0x1: Open drain
0x0C2E	[7:1]	reserved	7	-	-	-
	[0]	GPIO8_OD_MODE	1	R/W	1'h0	I2SWC_GPIO8 outpu buffer type select 0x0: Push pull, 0x1: Open drain
0x0C2F	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO0_OD_MODE	1	R/W	1'h0	D_GPIO0 outpu buffer type select 0x0: Push pull, 0x1: Open drain
0x0C30	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO1_OD_MODE	1	R/W	1'h0	D_GPIO1 outpu buffer type select 0x0: Push pull, 0x1: Open drain
0x0C31	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO2_OD_MODE	1	R/W	1'h0	D_GPIO2 outpu buffer type select 0x0: Push pull, 0x1: Open drain
0x0C32	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO3_OD_MODE	1	R/W	1'h0	D_GPIO3 outpu buffer type select 0x0: Push pull, 0x1: Open drain
0x0C33	[7:0]	reserved	8	-	-	-
0x0C34	[7:0]	reserved	8	-	-	-
0x0C35	[7:0]	reserved	8	-	-	-
0x0C36	[7:0]	reserved	8	-	-	-
0x0C37	[7:0]	reserved	8	-	-	-
0x0C38	[7:0]	reserved	8	-	-	-
0x0C39	[7:0]	reserved	8	-	-	-
0x0C3A	[7:0]	reserved	8	-	-	-
0x0C3B	[7:0]	reserved	8	-	-	-
0x0C3C	[7:0]	reserved	8	-	-	-
0x0C3D	[7:1]	reserved	7	-	-	-
	[0]	SMP_NUM_FIXMODE_L0	1	R/W	1'h1	BCC Lane0 Through GPIO select 0x0: Flexible, depending on SMP_GPIOx. 0x1: Fixed, depending on SMP_NUM.

Address	bit	Register Name	width	R/W	Init	Description
0x0C3E	[7:1]	reserved	7	-	-	-
	[0]	SMP_NUM_L0	1	R/W	1'h1	BCC Lane0 Through GPIO select 0x0: Enable GPIO0-3 only. Sampling rate will be double but disable D_GPIO0-3. 0x1: Enable GPIO0-3 and D_GPIO0-3.
0x0C3F	[7:4]	SMP_GPIO7_L0	4	R/W	4'h0	BCC Lane0 GPIO_ENCOUT[7] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[7] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[7] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[7] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[7] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[7] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[7] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[7] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[7] output others:reserved
	[3:0]	SMP_GPIO6_L0	4	R/W	4'h0	BCC Lane0 GPIO_ENCOUT[6] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[6] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[6] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[6] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[6] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[6] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[6] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[6] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[6] output others:reserved
0x0C40	[7:4]	SMP_GPIO5_L0	4	R/W	4'h0	BCC Lane0 GPIO_ENCOUT[5] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[5] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[5] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[5] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[5] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[5] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[5] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[5] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[5] output others:reserved
	[3:0]	SMP_GPIO4_L0	4	R/W	4'h0	BCC Lane0 GPIO_ENCOUT[4] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[4] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[4] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[4] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[4] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[4] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[4] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[4] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[4] output others:reserved
0x0C41	[7:4]	SMP_GPIO3_L0	4	R/W	4'h0	BCC Lane0 GPIO_ENCOUT[3] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[3] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[3] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[3] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[3] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[3] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[3] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[3] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[3] output others:reserved
	[3:0]	SMP_GPIO2_L0	4	R/W	4'h0	BCC Lane0 GPIO_ENCOUT[2] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[2] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[2] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[2] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[2] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[2] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[2] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[2] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[2] output others:reserved
0x0C42	[7:4]	SMP_GPIO1_L0	4	R/W	4'h0	BCC Lane0 GPIO_ENCOUT[1] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[1] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[1] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[1] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[1] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[1] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[1] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[1] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[1] output others:reserved
	[3:0]	SMP_GPIO0_L0	4	R/W	4'h0	BCC Lane0 GPIO_ENCOUT[0] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[0] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[0] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[0] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[0] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[0] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[0] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[0] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[0] output others:reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0C43	[7:4]	DESMP_GPIO7_L0	4	R/W	4'h0	BCC Lane0 GPIO_DECIN[7] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[7] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[7] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[7] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[7] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[7] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[7] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[7] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[7] is Decodeded to D_GPIO3 output others:reserved
	[3:0]	DESMP_GPIO6_L0	4	R/W	4'h0	BCC Lane0 GPIO_DECIN[6] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[6] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[6] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[6] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[6] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[6] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[6] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[6] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[6] is Decodeded to D_GPIO3 output others:reserved
0x0C44	[7:4]	DESMP_GPIO5_L0	4	R/W	4'h0	BCC Lane0 GPIO_DECIN[5] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[5] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[5] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[5] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[5] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[5] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[5] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[5] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[5] is Decodeded to D_GPIO3 output others:reserved
	[3:0]	DESMP_GPIO4_L0	4	R/W	4'h0	BCC Lane0 GPIO_DECIN[4] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[4] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[4] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[4] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[4] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[4] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[4] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[4] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[4] is Decodeded to D_GPIO3 output others:reserved
0x0C45	[7:4]	DESMP_GPIO3_L0	4	R/W	4'h0	BCC Lane0 GPIO_DECIN[3] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[3] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[3] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[3] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[3] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[3] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[3] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[3] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[3] is Decodeded to D_GPIO3 output others:reserved
	[3:0]	DESMP_GPIO2_L0	4	R/W	4'h0	BCC Lane0 GPIO_DECIN[2] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[2] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[2] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[2] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[2] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[2] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[2] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[2] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[2] is Decodeded to D_GPIO3 output others:reserved
0x0C46	[7:4]	DESMP_GPIO1_L0	4	R/W	4'h0	BCC Lane0 GPIO_DECIN[1] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[1] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[1] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[1] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[1] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[1] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[1] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[1] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[1] is Decodeded to D_GPIO3 output others:reserved
	[3:0]	DESMP_GPIO0_L0	4	R/W	4'h0	BCC Lane0 GPIO_DECIN[0] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[0] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[0] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[0] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[0] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[0] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[0] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[0] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[0] is Decodeded to D_GPIO3 output others:reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0C47	[7:5]	reserved	3	-	-	-
	[4]	ERR8B10B_ERRDET_EN	1	R/W	1'h0	FC 8b10b Error Detection Enable 0x0: Disable, 0x01: Enable
	[3]	WDTEN_ERRDET_EN	1	R/W	1'h0	BC WDT Error Detection Enable 0x0: Disable, 0x01: Enable
	[2]	MC_ERRDET_EN	1	R/W	1'h1	BC Manchester Code Error Detection Enable 0x0: Disable, 0x01: Enable
	[1]	LOCK_ERRDET_EN	1	R/W	1'h1	FC and BC Lock Error Detection Enable 0x0: Disable, 0x01: Enable
	[0]	CRC_ERRDET_EN	1	R/W	1'h1	FC and BC CRC Error Detection Enable 0x0: Disable, 0x01: Enable
0x0C48	[7:4]	D_GPIO3_IN_FILTER_RANGE_L0	4	R/W	4'h4	D_GPIO3 Input Filter Range 0:Filter OFF others:tOSC x2 xD_GPIO3_IN_FILTER_RANGE_L0
	[3:0]	D_GPIO2_IN_FILTER_RANGE_L0	4	R/W	4'h4	D_GPIO2 Input Filter Range 0:Filter OFF others:tOSC x2 xD_GPIO2_IN_FILTER_RANGE_L0
0x0C49	[7:4]	D_GPIO1_IN_FILTER_RANGE_L0	4	R/W	4'h4	D_GPIO1 Input Filter Range 0:Filter OFF others:tOSC x2 xD_GPIO1_IN_FILTER_RANGE_L0
	[3:0]	D_GPIO0_IN_FILTER_RANGE_L0	4	R/W	4'h4	D_GPIO0 Input Filter Range 0:Filter OFF others:tOSC x2 xD_GPIO0_IN_FILTER_RANGE_L0
0x0C4A	[7:4]	GPIO3_IN_FILTER_RANGE_L0	4	R/W	4'h4	GPIO3 Input Filter Range 0:Filter OFF others:tOSC x2 xD_GPIO3_IN_FILTER_RANGE_L0
	[3:0]	GPIO2_IN_FILTER_RANGE_L0	4	R/W	4'h4	GPIO2 Input Filter Range 0:Filter OFF others:tOSC x2 xD_GPIO2_IN_FILTER_RANGE_L0
0x0C4B	[7:4]	GPIO1_IN_FILTER_RANGE_L0	4	R/W	4'h4	GPIO1 Input Filter Range 0:Filter OFF others:tOSC x2 xD_GPIO1_IN_FILTER_RANGE_L0
	[3:0]	GPIO0_IN_FILTER_RANGE_L0	4	R/W	4'h4	GPIO0 Input Filter Range 0:Filter OFF others:tOSC x2 xD_GPIO0_IN_FILTER_RANGE_L0
0x0C4C	[7:4]	D_GPIO_3_OUT_FILTER_RANGE_L0	4	R/W	4'h1	D_GPIO3 Output Filter Range 0:Filter OFF others:1/fSMPL_GPI2FC xD_GPIO3_OUT_FILTER_RANGE_L0
	[3:0]	D_GPIO_2_OUT_FILTER_RANGE_L0	4	R/W	4'h1	D_GPIO2 Output Filter Range 0:Filter OFF others:1/fSMPL_GPI2FC xD_GPIO2_OUT_FILTER_RANGE_L0
0x0C4D	[7:4]	D_GPIO_1_OUT_FILTER_RANGE_L0	4	R/W	4'h1	D_GPIO1 Output Filter Range 0:Filter OFF others:1/fSMPL_GPI2FC xD_GPIO1_OUT_FILTER_RANGE_L0
	[3:0]	D_GPIO_0_OUT_FILTER_RANGE_L0	4	R/W	4'h1	D_GPIO0 Output Filter Range 0:Filter OFF others:1/fSMPL_GPI2FC xD_GPIO0_OUT_FILTER_RANGE_L0
0x0C4E	[7:4]	GPIO_3_OUT_FILTER_RANGE_L0	4	R/W	4'h1	GPIO3 Output Filter Range 0:Filter OFF others:1/fSMPL_GPI2FC xGPIO3_OUT_FILTER_RANGE_L0
	[3:0]	GPIO_2_OUT_FILTER_RANGE_L0	4	R/W	4'h1	GPIO2 Output Filter Range 0:Filter OFF others:1/fSMPL_GPI2FC xGPIO2_OUT_FILTER_RANGE_L0
0x0C4F	[7:4]	GPIO_1_OUT_FILTER_RANGE_L0	4	R/W	4'h1	GPIO1 Output Filter Range 0:Filter OFF others:1/fSMPL_GPI2FC xGPIO1_OUT_FILTER_RANGE_L0
	[3:0]	GPIO_0_OUT_FILTER_RANGE_L0	4	R/W	4'h1	GPIO0 Output Filter Range 0:Filter OFF others:1/fSMPL_GPI2FC xGPIO0_OUT_FILTER_RANGE_L0

Address	bit	Register Name	Global	Addres	Addr(h)	Local
0x0C50	[7:2]	reserved	6	-	-	-
	[1]	I2S_LOCK_ERRDET_EN_L0	1	R/W	1'h1	Lock Error Detection Enable 0:Disable 1:Enable
	[0]	I2S_CRC_ERRDET_EN_L0	1	R/W	1'h1	CRC Error Detection Enable 0:Disable 1:Enable
0x0C51	[7:1]	reserved	7	-	-	-
	[0]	I2S_CORRECT_EN_L0	1	R/W	1'h1	I2S Output Correction Enable 0:Disable 1:Enable
0x0C52	[7:0]	reserved	8	-	-	-
0x0C53	[7:0]	reserved	8	-	-	-
0x0C54	[7:0]	reserved	8	-	-	-
0x0C55	[7:0]	reserved	8	-	-	-
0x0C56	[7:5]	reserved	3	-	-	-
	[4:0]	GPIO_PULLDOWN_UPPER	5	R/W	5'h1F	GPIO Pull down setting-1. 0x0: Disable, 0x1: Enable [4]: Reserved [3]: D_GPIO3 [2]: D_GPIO2 [1]: D_GPIO1 [0]: D_GPIO0
0x0C57	[7:0]	GPIO_PULLDOWN_LOWER	8	R/W	8'hFF	GPIO Pull down setting-2. 0x0: Disable, 0x1: Enable [7]: I2SWC_GPIO8 [6]: I2SWC_GPIO7 [5]: I2SD0_GPIO6 [4]: I2SD1_GPIO5 [3]: I2SD3_GPIO3 [2]: I2SD2_GPIO2 [1]: GPIO1 [0]: GPIO0
0x0C58	[7:0]	reserved	8	-	-	-
0x0C59	[7:0]	reserved	8	-	-	-
0x0C5A	[7:0]	reserved	8	-	-	-
0x0C5B	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0C80	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	GPIO10_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C80[2:0]=0x1, 0x7> GPIO10 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO10_MODE	3	R/W	3'h0	GPIO10 I/O Mode setting. Compatible with "GPIO0" of Deserializer in VbyOneHSII Lane1 when used as Through GPIO. 0x0: Disable (Hi-Z) 0x1: Programable GPO (To output GPIO10_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode. 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to GPIO0_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C81	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	GPIO11_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C81[2:0]=0x1, 0x7> GPIO11 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO11_MODE	3	R/W	3'h0	GPIO11 I/O Mode setting. Compatible with "GPIO1" of Deserializer in VbyOneHSII Lane1 when used as Through GPIO. 0x0: Disable (Hi-Z) 0x1: Programable GPO (To output GPIO11_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode. 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to GPIO0_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C82	[7:0]	reserved	8	-	-	-
0x0C83	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0C84	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	reserved	1	-	-	
	[2:0]	D_GPIO0_MODE_L1I2S	3	R/W	3'h2	D_GPIO0 Mode setting.for VbyOneHSII lane1 I2S enable in Asynchronize I2S transport mode. 0x0: I2S D1 input mode for VbyOneHSII lane1. 0x2: Disable. Allways set to Disable except when used as I2S D1 for VbyOneHSII lane1 Others: Reserved
0x0C85	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	reserved	1	-	-	
	[2:0]	D_GPIO1_MODE_L1I2S	3	R/W	3'h2	D_GPIO1 Mode setting.for VbyOneHSII lane1 I2S enable in Asynchronize I2S transport mode. 0x0: I2S D0 input mode for VbyOneHSII lane1. 0x2: Disable. Allways set to Disable except when used as I2S D1 for VbyOneHSII lane1 Others: Reserved
0x0C86	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	reserved	1	-	-	
	[2:0]	D_GPIO2_MODE_L1I2S	3	R/W	3'h2	D_GPIO2 Mode setting.for VbyOneHSII lane1 I2S enable in Asynchronize I2S transport mode. 0x0: I2S WC input mode for VbyOneHSII lane1. 0x2: Disable. Allways set to Disable except when used as I2S WC for VbyOneHSII lane1 Others: Reserved
0x0C87	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	reserved	1	-	-	
	[2:0]	D_GPIO3_MODE_L1I2S	3	R/W	3'h2	D_GPIO3 Mode setting.for VbyOneHSII lane1 I2S enable in Asynchronize I2S transport mode. 0x0: I2S CLK input mode for VbyOneHSII lane1. 0x2: Disable. Allways set to Disable except when used as I2S CLK for VbyOneHSII lane1 Others: Reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0C88	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	reserved	1	-	-	
	[2:0]	I2SD1_GPIO5_MODE_L1	3	R/W	3'h0	I2SD1_GPIO5 Mode setting.for VbyOneHSII lane1 Through GPIO. Compatible with "D_GPIO0" of Deserializer in VbyOneHSII Lane1 when used as Through GPIO. In this mode, 0x0C04 needs to set disable (0x02). 0x0: Disable (Hi-Z) 0x3: Through GPI Mode 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to D_GPIO1_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C89	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	reserved	1	-	-	
	[2:0]	I2SD0_GPIO6_MODE_L1	3	R/W	3'h0	I2SD0_GPIO6 Mode setting.for VbyOneHSII lane1 Through GPIO. Compatible with "D_GPIO1" of Deserializer in VbyOneHSII Lane1 when used as Through GPIO. In this mode, 0x0C05 needs to set disable (0x02). 0x0: Disable (Hi-Z) 0x3: Through GPI Mode 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to D_GPIO1_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C8A	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	reserved	1	-	-	
	[2:0]	I2SWC_GPIO7_MODE_L1	3	R/W	3'h0	I2SWC_GPIO7 Mode setting.for VbyOneHSII lane1 Through GPIO. Compatible with "D_GPIO2" of Deserializer in VbyOneHSII Lane1 when used as Through GPIO. In this mode, 0x0C06 needs to set disable (0x02). 0x0: Disable (Hi-Z) 0x3: Through GPI Mode 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to D_GPIO1_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C8B	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	reserved	1	-	-	
	[2:0]	I2SCLK_GPIO8_MODE_L1	3	R/W	3'h0	I2SCLK_GPIO8 Mode setting.for VbyOneHSII lane1 Through GPIO. Compatible with "D_GPIO3" of Deserializer in VbyOneHSII Lane1 when used as Through GPIO. In this mode, 0x0C07 needs to set disable (0x02). 0x0: Disable (Hi-Z) 0x3: Through GPI Mode 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to D_GPIO1_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C8C	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0C8D	[7:1]	reserved	7	-	-	-
	[0]	GPIO10_IMON	1	R	1'h0	GPIO10 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C8E	[7:1]	reserved	7	-	-	-
	[0]	GPIO11_IMON	1	R	1'h0	GPIO11 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C8F	[7:0]	reserved	8	-	-	-
0x0C90	[7:0]	reserved	8	-	-	-
0x0C91	[7:0]	reserved	8	-	-	-
0x0C92	[7:0]	reserved	8	-	-	-
0x0C93	[7:0]	reserved	8	-	-	-
0x0C94	[7:0]	reserved	8	-	-	-
0x0C95	[7:0]	reserved	8	-	-	-
0x0C96	[7:0]	reserved	8	-	-	-
0x0C97	[7:0]	reserved	8	-	-	-
0x0C98	[7:0]	reserved	8	-	-	-
0x0C99	[7:0]	reserved	8	-	-	-
0x0C9A	[7:0]	reserved	8	-	-	-
0x0C9B	[7:0]	reserved	8	-	-	-
0x0C9C	[7:0]	reserved	8	-	-	-
0x0C9D	[7:0]	reserved	8	-	-	-
0x0C9E	[7:0]	reserved	8	-	-	-
0x0C9F	[7:0]	reserved	8	-	-	-
0x0CA0	[7:0]	reserved	8	-	-	-
0x0CA1	[7:0]	reserved	8	-	-	-
0x0CA2	[7:0]	reserved	8	-	-	-
0x0CA3	[7:0]	reserved	8	-	-	-
0x0CA4	[7:0]	reserved	8	-	-	-
0x0CA5	[7:0]	reserved	8	-	-	-
0x0CA6	[7:0]	reserved	8	-	-	-
0x0CA7	[7:1]	reserved	7	-	-	-
	[0]	GPIO10_OD_MODE	1	R/W	1'h0	GPIO10 outpu buffer type select 0x0: Push pull, 0x1: Open drain
0x0CA8	[7:1]	reserved	7	-	-	-
	[0]	GPIO11_OD_MODE	1	R/W	1'h0	GPIO11 outpu buffer type select 0x0: Push pull, 0x1: Open drain
0x0CA9	[7:0]	reserved	8	-	-	-
0x0CAA	[7:0]	reserved	8	-	-	-
0x0CAB	[7:0]	reserved	8	-	-	-
0x0CAC	[7:0]	reserved	8	-	-	-
0x0CAD	[7:0]	reserved	8	-	-	-
0x0CAE	[7:0]	reserved	8	-	-	-
0x0CAF	[7:0]	reserved	8	-	-	-
0x0CB0	[7:0]	reserved	8	-	-	-
0x0CB1	[7:0]	reserved	8	-	-	-
0x0CB2	[7:0]	reserved	8	-	-	-
0x0CB3	[7:0]	reserved	8	-	-	-
0x0CB4	[7:0]	reserved	8	-	-	-
0x0CB5	[7:0]	reserved	8	-	-	-
0x0CB6	[7:0]	reserved	8	-	-	-
0x0CB7	[7:0]	reserved	8	-	-	-
0x0CB8	[7:0]	reserved	8	-	-	-
0x0CB9	[7:0]	reserved	8	-	-	-
0x0CBA	[7:0]	reserved	8	-	-	-
0x0CBB	[7:0]	reserved	8	-	-	-
0x0CBC	[7:0]	reserved	8	-	-	-
0x0CBD	[7:1]	reserved	7	-	-	-
	[0]	SMP_NUM_FIXMODE_L1	1	R/W	1'h1	BCC Lane1 Through GPIO select 0x0: Flexible, depending on SMP_GPIOx. 0x1: Fixed, depending on SMP_NUM.

Address	bit	Register Name	width	R/W	Init	Description
0x0CBE	[7:1]	reserved	7	-	-	-
	[0]	SMP_NUM_L1	1	R/W	1'h1	BCC Lane1 Through GPIO select 0x0: Enable GPIO0-3 only. Sampling rate will be double but disable D_GPIO0-3. 0x1: Enable GPIO0-3 and D_GPIO0-3.
0x0CBF	[7:4]	SMP_GPIO7_L1	4	R/W	4'h0	BCC Lane1 GPIO_ENCOUT[7] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[7] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[7] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[7] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[7] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[7] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[7] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[7] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[7] output others:reserved
	[3:0]	SMP_GPIO6_L1	4	R/W	4'h0	BCC Lane1 GPIO_ENCOUT[6] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[6] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[6] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[6] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[6] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[6] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[6] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[6] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[6] output others:reserved
0x0CC0	[7:4]	SMP_GPIO5_L1	4	R/W	4'h0	BCC Lane1 GPIO_ENCOUT[5] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[5] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[5] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[5] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[5] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[5] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[5] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[5] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[5] output others:reserved
	[3:0]	SMP_GPIO4_L1	4	R/W	4'h0	BCC Lane1 GPIO_ENCOUT[4] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[4] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[4] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[4] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[4] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[4] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[4] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[4] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[4] output others:reserved
0x0CC1	[7:4]	SMP_GPIO3_L1	4	R/W	4'h0	BCC Lane1 GPIO_ENCOUT[3] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[3] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[3] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[3] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[3] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[3] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[3] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[3] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[3] output others:reserved
	[3:0]	SMP_GPIO2_L1	4	R/W	4'h0	BCC Lane1 GPIO_ENCOUT[2] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[2] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[2] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[2] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[2] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[2] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[2] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[2] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[2] output others:reserved
0x0CC2	[7:4]	SMP_GPIO1_L1	4	R/W	4'h0	BCC Lane1 GPIO_ENCOUT[1] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[1] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[1] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[1] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[1] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[1] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[1] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[1] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[1] output others:reserved
	[3:0]	SMP_GPIO0_L1	4	R/W	4'h0	BCC Lane1 GPIO_ENCOUT[0] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[0] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[0] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[0] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[0] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[0] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[0] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[0] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[0] output others:reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0CC3	[7:4]	DESMP_GPIO7_L1	4	R/W	4'h0	BCC Lane1 GPIO_DECIN[7] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[7] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[7] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[7] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[7] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[7] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[7] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[7] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[7] is Decodeded to D_GPIO3 output others:reserved
	[3:0]	DESMP_GPIO6_L1	4	R/W	4'h0	BCC Lane1 GPIO_DECIN[6] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[6] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[6] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[6] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[6] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[6] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[6] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[6] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[6] is Decodeded to D_GPIO3 output others:reserved
0x0CC4	[7:4]	DESMP_GPIO5_L1	4	R/W	4'h0	BCC Lane1 GPIO_DECIN[5] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[5] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[5] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[5] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[5] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[5] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[5] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[5] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[5] is Decodeded to D_GPIO3 output others:reserved
	[3:0]	DESMP_GPIO4_L1	4	R/W	4'h0	BCC Lane1 GPIO_DECIN[4] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[4] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[4] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[4] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[4] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[4] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[4] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[4] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[4] is Decodeded to D_GPIO3 output others:reserved
0x0CC5	[7:4]	DESMP_GPIO3_L1	4	R/W	4'h0	BCC Lane1 GPIO_DECIN[3] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[3] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[3] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[3] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[3] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[3] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[3] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[3] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[3] is Decodeded to D_GPIO3 output others:reserved
	[3:0]	DESMP_GPIO2_L1	4	R/W	4'h0	BCC Lane1 GPIO_DECIN[2] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[2] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[2] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[2] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[2] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[2] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[2] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[2] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[2] is Decodeded to D_GPIO3 output others:reserved
0x0CC6	[7:4]	DESMP_GPIO1_L1	4	R/W	4'h0	BCC Lane1 GPIO_DECIN[1] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[1] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[1] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[1] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[1] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[1] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[1] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[1] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[1] is Decodeded to D_GPIO3 output others:reserved
	[3:0]	DESMP_GPIO0_L1	4	R/W	4'h0	BCC Lane1 GPIO_DECIN[0] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[0] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[0] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[0] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[0] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[0] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[0] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[0] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[0] is Decodeded to D_GPIO3 output others:reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0CC7	[7:5]	reserved	3	-	-	-
	[4]	ERR8B10B_ERRDET_EN_L1	1	R/W	1'h0	FC 8b10b Error Detection Enable 0x0: Disable, 0x01: Enable
	[3]	WDTEN_ERRDET_EN_L1	1	R/W	1'h0	BC WDT Error Detection Enable 0x0: Disable, 0x01: Enable
	[2]	MC_ERRDET_EN_L1	1	R/W	1'h1	BC Manchester Code Error Detection Enable 0x0: Disable, 0x01: Enable
	[1]	LOCK_ERRDET_EN_L1	1	R/W	1'h1	FC and BC Lock Error Detection Enable 0x0: Disable, 0x01: Enable
	[0]	CRC_ERRDET_EN_L1	1	R/W	1'h1	FC and BC CRC Error Detection Enable 0x0: Disable, 0x01: Enable
0x0CC8	[7:0]	reserved	8	-	-	-
0x0CC9	[7:0]	reserved	8	-	-	-
0x0CCA	[7:0]	reserved	8	-	-	-
0x0CCB	[7:0]	reserved	8	-	-	-
0x0CCC	[7:0]	reserved	8	-	-	-
0x0CCD	[7:0]	reserved	8	-	-	-
0x0CCE	[7:0]	reserved	8	-	-	-
0x0CCF	[7:0]	reserved	8	-	-	-
0x0CD0	[7:2]	reserved	8	-	-	-
	[1]	I2S_LOCK_ERRDET_EN_L1	1	R/W	1'h1	Lock Error Detection Enable 0:Disable 1:Enable
	[0]	I2S_CRC_ERRDET_EN_L1	1	R/W	1'h1	CRC Error Detection Enable 0:Disable 1:Enable
0x0CD1	[7:1]	reserved	7	-	-	-
	[0]	I2S_CORRECT_EN_L1	1	R/W	1'h1	I2S Output Correction Enable 0:Disable 1:Enable

Address	bit	Register Name	width	R/W	Init	Description
0x1000	[7:0]	reserved	8	-	-	-
0x1001	[7:0]	reserved	8	-	-	-
0x1002	[7:1]	reserved	8	-	-	-
	[0]	FSBP_DTH_EN_L0	1	R/W	1'h1	VbyOneHSII Controll Data Through Select. It also should be set disable when connect to VbyOneHS protocol Deserializer. 0x0: Disable 0x1: Enable, Normal operation

Address	bit	Register Name	width	R/W	Init	Description
0x1100	[7:0]	reserved	8	-	-	-
0x1101	[7:0]	reserved	8	-	-	-
0x1102	[7:1]	reserved	8	-	-	-
	[0]	FSBP_DTH_EN_L1	1	R/W	1'h1	VbyOneHSII Controll Data Through Select for lane1. It also should be set disable when connect to VbyOneHS protocol Deserializer. 0x0: Disable 0x1: Enable, Normal operation

Address	bit	Register Name	width	R/W	Init	Description
0x1300	[7:6]	reserved	2	-	-	-
	[5:4]	INTN_BYPASS	2	R/W	2'h2	INTN pin output select. INTN pin will mirror the status of INTN_IN on the Deserializer when set 0x0 and 0x1. It also outputs the enabled Interrupt signal when set to 0x2. 0x0: Mirror VbyOneHSII lane0 INTN_IN 0x1: Mirror VbyOneHSII lane1 INTN_IN 0x2: Intrrupt output 0x3: Reserved
	[3:2]	reserved	2	-	-	-
	[1:0]	INTN_MODE	2	R/W	2'h1	INTN pin output mode select 0x0: Disable 0x1: Open drain 0x2: Push pull, Low Active 0x3: Push pull, High Active
0x1301	[7:0]	reserved	8	-	-	-
0x1302	[7:0]	reserved	8	-	-	-
0x1303	[7:0]	reserved	8	-	-	-
0x1304	[7:5]	reserved	6	-	-	-
	[4]	INTN_M_CLEAR	1	W	-	INTN Mask all clear. Interrupt Mask settings will be disable. 0x1: clear
	[3:1]	reserved	3	-	-	-
	[0]	INTN_S_CLEAR	1	W	-	INTN Interrupt all clear. Interrupt statuses will be clear. 0x1: clear

Address	bit	Register Name	width	R/W	Init	Description
0x1310	[7:5]	reserved	3	-	-	-
	[4]	INTN_UNLOCK_L1	1	R/W1C	1'h0	PLL Unlock Detect for VbyOneHSII lane1 0x0: No interrupt, 0x1: Interrupt
	[3:1]	reserved	3	-	-	-
	[0]	INTN_UNLOCK_L0	1	R/W1C	1'h0	PLL Unlock Detect for VbyOneHSII lane0 0x0: No interrupt, 0x1: Interrupt
0x1311	[7]	INTN_ERR_TX1CHU	1	R/W1C	1'h0	PLL Output Clock Upper Error for VbyOneHSII lane1 0x0: No interrupt, 0x1: Interrupt
	[6]	INTN_ERR_TX1CHL	1	R/W1C	1'h0	PLL Output Clock Low er Error for VbyOneHSII lane1 0x0: No interrupt, 0x1: Interrupt
	[5]	INTN_ERR_TX0CHU	1	R/W1C	1'h0	PLL Output Clock Upper Error for VbyOneHSII lane0 0x0: No interrupt, 0x1: Interrupt
	[4]	INTN_ERR_TX0CHL	1	R/W1C	1'h0	PLL Output Clock Low er Error for VbyOneHSII lane0 0x0: No interrupt, 0x1: Interrupt
	[3]	INTN_ERR_RX1CHU	1	R/W1C	1'h0	DSI Byte Clock and REFCLK Upper Error for port1 0x0: No interrupt, 0x1: Interrupt
	[2]	INTN_ERR_RX1CHL	1	R/W1C	1'h0	DSI Byte Clock and REFCLK Lower Error for port1 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_ERR_RX0CHU	1	R/W1C	1'h0	DSI Byte Clock and REFCLK Upper Error for port0 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_RX0CHL	1	R/W1C	1'h0	DSI Byte Clock and REFCLK Lower Error for port0 0x0: No interrupt, 0x1: Interrupt
0x1312	[7:6]	reserved	2	-	-	-
	[5]	INTN_ERR_FPLL1CHU	1	R/W1C	1'h0	PLL Input Clock Upper Error for VbyOneHSII lane0 0x0: No interrupt, 0x1: Interrupt
	[4]	INTN_ERR_FPLL1CHL	1	R/W1C	1'h0	PLL Input Clock Low er Error for VbyOneHSII lane0 0x0: No interrupt, 0x1: Interrupt
	[3]	INTN_ERR_FPLL0CHU	1	R/W1C	1'h0	PLL Input Clock Upper Error for port1 0x0: No interrupt, 0x1: Interrupt
	[2]	INTN_ERR_FPLL0CHL	1	R/W1C	1'h0	PLL Input Clock Lower Error for port1 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_ERR_OSCU	1	R/W1C	1'h0	Internal Oscillator Clock Upper Error 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_OSCL	1	R/W1C	1'h0	Internal Oscillator Clock Lower Error 0x0: No interrupt, 0x1: Interrupt

Address	bit	Register Name	width	R/W	Init	Description
0x1320	[7:4]	reserved	4	-	-	-
	[3]	INTN_ERR_PATCHK_P0L0	1	R/W1C	1'h0	Pattern Check Error for DSI port0 data lane0 0x0: No interrupt, 0x1: Interrupt
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_FIFO_P0L0	1	R/W1C	1'h0	FIFO Error signal for DSI port0 data lane0 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_SOT_P0L0	1	R/W1C	1'h0	SOT 1bit Error for DSI port0 data lane0 0x0: No interrupt, 0x1: Interrupt
0x1321	[7:4]	reserved	4	-	-	-
	[3]	INTN_ERR_PATCHK_P0L1	1	R/W1C	1'h0	Pattern Check Error for DSI port0 data lane1 0x0: No interrupt, 0x1: Interrupt
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_FIFO_P0L1	1	R/W1C	1'h0	FIFO Error signal for DSI port0 data lane1 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_SOT_P0L1	1	R/W1C	1'h0	SOT 1bit Error for DSI port0 data lane1 0x0: No interrupt, 0x1: Interrupt
0x1322	[7:4]	reserved	4	-	-	-
	[3]	INTN_ERR_PATCHK_P0L2	1	R/W1C	1'h0	Pattern Check Error for DSI port0 data lane2 0x0: No interrupt, 0x1: Interrupt
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_FIFO_P0L2	1	R/W1C	1'h0	FIFO Error signal for DSI port0 data lane2 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_SOT_P0L2	1	R/W1C	1'h0	SOT 1bit Error for DSI port0 data lane2 0x0: No interrupt, 0x1: Interrupt
0x1323	[7:4]	reserved	4	-	-	-
	[3]	INTN_ERR_PATCHK_P0L3	1	R/W1C	1'h0	Pattern Check Error for DSI port0 data lane3 0x0: No interrupt, 0x1: Interrupt
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_FIFO_P0L3	1	R/W1C	1'h0	FIFO Error signal for DSI port0 data lane3 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_SOT_P0L3	1	R/W1C	1'h0	SOT 1bit Error for DSI port0 data lane3 0x0: No interrupt, 0x1: Interrupt
0x1324	[7:4]	reserved	4	-	-	-
	[3]	INTN_ERR_PATCHK_P1L0	1	R/W1C	1'h0	Pattern Check Error for DSI port1 data lane0 0x0: No interrupt, 0x1: Interrupt
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_FIFO_P1L0	1	R/W1C	1'h0	FIFO Error signal for DSI port1 data lane0 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_SOT_P1L0	1	R/W1C	1'h0	SOT 1bit Error for DSI port1 data lane0 0x0: No interrupt, 0x1: Interrupt
0x1325	[7:4]	reserved	4	-	-	-
	[3]	INTN_ERR_PATCHK_P1L1	1	R/W1C	1'h0	Pattern Check Error for DSI port1 data lane1 0x0: No interrupt, 0x1: Interrupt
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_FIFO_P1L1	1	R/W1C	1'h0	FIFO Error signal for DSI port1 data lane1 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_SOT_P1L1	1	R/W1C	1'h0	SOT 1bit Error for DSI port1 data lane1 0x0: No interrupt, 0x1: Interrupt
0x1326	[7:4]	reserved	4	-	-	-
	[3]	INTN_ERR_PATCHK_P1L2	1	R/W1C	1'h0	Pattern Check Error for DSI port1 data lane2 0x0: No interrupt, 0x1: Interrupt
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_FIFO_P1L2	1	R/W1C	1'h0	FIFO Error signal for DSI port1 data lane2 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_SOT_P1L2	1	R/W1C	1'h0	SOT 1bit Error for DSI port1 data lane2 0x0: No interrupt, 0x1: Interrupt
0x1327	[7:4]	reserved	4	-	-	-
	[3]	INTN_ERR_PATCHK_P1L3	1	R/W1C	1'h0	Pattern Check Error for DSI port1 data lane3 0x0: No interrupt, 0x1: Interrupt
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_FIFO_P1L3	1	R/W1C	1'h0	FIFO Error signal for DSI port1 data lane3 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_SOT_P1L3	1	R/W1C	1'h0	SOT 1bit Error for DSI port1 data lane3 0x0: No interrupt, 0x1: Interrupt

Address	bit	Register Name	width	R/W	Init	Description
0x1330	[7:2]	reserved	6	-	-	-
	[1]	INTN_ERR_ECC_TWO_BIT_P0	1	R/W1C	1'h0	PH double bit error interrupt for DSI port0. 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_ECC_ONE_BIT_P0	1	R/W1C	1'h0	PH single bit error interrupt for DSI port0. This error wii be corrected. 0x0: No interrupt, 0x1: Interrupt
0x1331	[7]	INTN_ERR_INVALID_LENGTH_P0	1	R/W1C	1'h0	Payload Data Length Error for port0. Interrupt when payload data and WC do not match. 0x0: No interrupt, 0x1: Interrupt
	[6]	INTN_ERR_DATA_TYPE_P0	1	R/W1C	1'h0	Non-support Data Type Error for port0 0x0: No interrupt, 0x1: Interrupt
	[5]	reserved	1	-	-	-
	[4]	INTN_ERR_FIFO_WRITE_DC_P0	1	R/W1C	1'h0	FIFO Write Error for port0 0x0: No interrupt, 0x1: Interrupt
	[3]	INTN_ERR_FIFO_OVF_P0	1	R/W1C	1'h0	FIFO Over Flow Error for port0 0x0: No interrupt, 0x1: Interrupt
	[2]	INTN_ERR_VC_INVALID_P0	1	R/W1C	1'h0	INVALID VC Error for port0. Interrupt when Input VC ID other than the ID registered in CFG_VC_P0 (0x0D00). 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_ERR_UNCORRECT_P0	1	R/W1C	1'h0	DSI Uncorrect Error for port0 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_CRC_P0	1	R/W1C	1'h0	DSI CRC Error for port0 0x0: No interrupt, 0x1: Interrupt
0x1332	[7:1]	reserved	7	-	-	-
	[0]	INTN_TIMEOUT_HS_RX_P0	1	R/W1C	1'h0	DSI HS Time Out Error for port0. Interrupt when HS time exceeds CFG_HRX_TO_COUNT_X_P0 [23:0]. 0x0: No interrupt, 0x1: Interrupt
0x1333	[7:2]	reserved	6	-	-	-
	[1]	INTN_ERR_ECC_TWO_BIT_P1	1	R/W1C	1'h0	PH double bit error interrupt for DSI port1. 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_ECC_ONE_BIT_P1	1	R/W1C	1'h0	PH single bit error interrupt for DSI port1. This error wii be corrected. 0x0: No interrupt, 0x1: Interrupt
0x1334	[7]	INTN_ERR_INVALID_LENGTH_P1	1	R/W1C	1'h0	Payload Data Length Error for port1. Interrupt when payload data and WC do not match. 0x0: No interrupt, 0x1: Interrupt
	[6]	INTN_ERR_DATA_TYPE_P1	1	R/W1C	1'h0	Non-support Data Type Error for port1 0x0: No interrupt, 0x1: Interrupt
	[5]	reserved	1	-	-	-
	[4]	INTN_ERR_FIFO_WRITE_DC_P1	1	R/W1C	1'h0	FIFO Write Error for port1 0x0: No interrupt, 0x1: Interrupt
	[3]	INTN_ERR_FIFO_OVF_P1	1	R/W1C	1'h0	FIFO Over Flow Error for port1 0x0: No interrupt, 0x1: Interrupt
	[2]	INTN_ERR_VC_INVALID_P1	1	R/W1C	1'h0	INVALID VC Error for port1. Interrupt when Input VC ID other than the ID registered in CFG_VC_P1 (0x0E00). 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_ERR_UNCORRECT_P1	1	R/W1C	1'h0	DSI Uncorrect Error for port1 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_CRC_P1	1	R/W1C	1'h0	DSI CRC Error for port1 0x0: No interrupt, 0x1: Interrupt
0x1335	[7:1]	reserved	7	-	-	-
	[0]	INTN_TIMEOUT_HS_RX_P1	1	R/W1C	1'h0	DSI HS Time Out Error for port1. Interrupt when HS time exceeds CFG_HRX_TO_COUNT_X_P1 [23:0]. 0x0: No interrupt, 0x1: Interrupt
0x1344	[7:0]	reserved	8	-	-	-
0x1345	[7:0]	reserved	8	-	-	-
0x1346	[7:0]	reserved	8	-	-	-
0x1347	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1350	[7:5]	reserved	3	-	-	-
	[4]	INTN_UNLOCK_VX1_L0	1	R/W1C	1'h0	VbyOneHSII FC Unlock Error for lane0 0x0: No interrupt, 0x1: Interrupt
	[3]	INTN_ERR_MC_L0	1	R/W1C	1'h0	VbyOneHSII BC Manchester Code Error for lane0 0x0: No interrupt, 0x1: Interrupt
	[2]	INTN_LOST_ALIVE_CMD_L0	1	R/W1C	1'h0	VbyOneHSII BC Alive CMD Lost Error for lane0 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_LOST_1ST_ALIVE_CMD_L0	1	R/W1C	1'h0	VbyOneHSII BC 1st Alive CMD Lost Error for lane0 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_WDT_L0	1	R/W1C	1'h0	VbyOneHSII BC WDT Error for lane0 0x0: No interrupt, 0x1: Interrupt
0x1351	[7:0]	reserved	8	-	-	-
0x1352	[7:5]	reserved	3	-	-	-
	[4]	INTN_UNLOCK_VX1_L1	1	R/W1C	1'h0	VbyOneHSII FC Unlock Error for lane1 0x0: No interrupt, 0x1: Interrupt
	[3]	INTN_ERR_MC_L1	1	R/W1C	1'h0	VbyOneHSII BC Manchester Code Error for lane1 0x0: No interrupt, 0x1: Interrupt
	[2]	INTN_LOST_ALIVE_CMD_L1	1	R/W1C	1'h0	VbyOneHSII BC Alive CMD Lost Error for lane1 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_LOST_1ST_ALIVE_CMD_L1	1	R/W1C	1'h0	VbyOneHSII BC 1st Alive CMD Lost Error for lane1 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_WDT_L1	1	R/W1C	1'h0	VbyOneHSII BC WDT Error for lane1 0x0: No interrupt, 0x1: Interrupt
0x1353	[7:0]	reserved	8	-	-	-
0x1360	[7:1]	reserved	7	-	-	-
	[0]	INTN_THRIO_VALID_L0	1	R/W1C	1'h0	VbyOneHSII Through IO status for lane0. Interrupt when both FC and BC link are Valid. 0x0: No interrupt, 0x1: Interrupt
0x1361	[7:1]	reserved	7	-	-	-
	[0]	INTN_THRIO_VALID_L1	1	R/W1C	1'h0	VbyOneHSII Through IO status for lane1. Interrupt when both FC and BC link are Valid. Available only in Dual Splitting and Dual Asynchronous output mode. 0x0: No interrupt, 0x1: Interrupt
0x1362	[7:1]	reserved	7	-	-	-
	[0]	INTN_FC_GPIO_VALID_L0	1	R/W1C	1'h0	VbyOneHSII FC Through GPIO data valid for lane0. 0x0: No interrupt, 0x1: Interrupt
0x1363	[7:1]	reserved	7	-	-	-
	[0]	INTN_FC_GPIO_VALID_L1	1	R/W1C	1'h0	VbyOneHSII FC Through GPIO data valid for lane1. Available only in Dual Splitting and Dual Asynchronous output mode. 0x0: No interrupt, 0x1: Interrupt
0x1364	[7:3]	reserved	5	-	-	-
	[2]	INTN_ERR_WRITE_L0	1	R/W1C	1'h0	VbyOneHSII BC Ring Buffer Write Error for lane0 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_ERR_CRC_OCLK_L0	1	R/W1C	1'h0	VbyOneHSII BC OCLK domain CRC Error for lane0 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_CRC_VCLK_L0	1	R/W1C	1'h0	VbyOneHSII BC VCLK domain CRC Error for lane0 0x0: No interrupt, 0x1: Interrupt
0x1365	[7:3]	reserved	5	-	-	-
	[2]	INTN_ERR_WRITE_L1	1	R/W1C	1'h0	VbyOneHSII BC Ring Buffer Write Error for lane1 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_ERR_CRC_OCLK_L1	1	R/W1C	1'h0	VbyOneHSII BC OCLK domain CRC Error for lane1 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_CRC_VCLK_L1	1	R/W1C	1'h0	VbyOneHSII BC VCLK domain CRC Error for lane1 0x0: No interrupt, 0x1: Interrupt
0x1366	[7:4]	reserved	4	-	-	-
	[3]	INTN_FC_BC_LINK_L0	1	R	-	VbyOneHSII FC/BC Link Error at deserializer side for lane0. This value is updated in real time. 0x0: No Error, 0x1: Error
	[2]	INTN_CTRL_THRIO_FCDATA_L0	1	R	-	VbyOneHSII Video Error at deserializer side for lane0. This value is updated in real time. 0x0: No Error, 0x1: Error
	[1]	INTN_GPIO_VALID0_L0	1	R	-	VbyOneHSII FC Through GPIO data valid for lane0. This value is updated in real time. 0x0: No valid, 0x1: Valid
	[0]	reserved	1	-	-	-
0x1367	[7:4]	reserved	4	-	-	-
	[3]	INTN_FC_BC_LINK_L1	1	R	-	VbyOneHSII FC/BC Link Error at deserializer side for lane1. This value is updated in real time. 0x0: No error, 0x1: Error
	[2]	INTN_CTRL_THRIO_FCDATA_L1	1	R	-	VbyOneHSII Video Error at deserializer side for lane1. This value is updated in real time. 0x0: No error, 0x1: Error
	[1]	INTN_GPIO_VALID0_L1	1	R	-	VbyOneHSII FC Through GPIO data valid for lane1. This value is updated in real time. 0x0: No valid, 0x1: Valid
	[0]	reserved	1	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1370	[7]	INTN_ERR_FCCRC	1	R/W1C	1'h0	VbyOneHSII FC CRC error 0x0: No interrupt, 0x1: Interrupt
	[6]	INTN_ERR_NACK	1	R/W1C	1'h0	Remote side 2-wire slave device NACK error 0x0: No interrupt, 0x1: Interrupt
	[5]	INTN_TIMEOUT	1	R/W1C	1'h0	Remote side 2-wire slave device time out error. Interrupt when SCL may be fixed low. 0x0: No interrupt, 0x1: Interrupt
	[4]	INTN_DONE_TRANS	1	R/W1C	1'h0	Remote side 2-wire access complete flag 0x0: No interrupt, 0x1: Interrupt
	[3]	INTN_FAIL_TRANS	1	R/W1C	1'h0	Remote side 2-wire access fail flag 0x0: No interrupt, 0x1: Interrupt
	[2]	INTN_ERR_BCCRC	1	R/W1C	1'h0	VbyOneHSII BC CRC Error 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_TIMEOUT_BRIDGE	1	R/W1C	1'h0	2-wire access time out error for remote side access 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_TIMEOUT_SLAVE	1	R/W1C	1'h0	Local side 2-wire time out error. Interrupt when SCL may be fixed low. 0x0: No interrupt, 0x1: Interrupt
0x1371	[7:1]	reserved	7	-	-	-
	[0]	INTN_REG_CHKSUM_ERR	1	R/W1C	1'h0	Register Check Sum Error 0x0: No interrupt, 0x1: Interrupt
0x1372	[7:0]	reserved	8	-	-	-
0x1373	[7:0]	reserved	8	-	-	-
0x1374	[7:0]	reserved	8	-	-	-
0x1375	[7:0]	reserved	8	-	-	-
0x1376	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1390	[7:5]	reserved	3	-	-	-
	[4]	INTN_UNLOCK_L1_M	1	R/W	1'h1	INTN_UNLOCK_L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3:1]	reserved	3	-	-	-
	[0]	INTN_UNLOCK_L0_M	1	R/W	1'h1	INTN_UNLOCK_L0_M Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1391	[7]	INTN_ERR_TX1CHU_M	1	R/W	1'h1	INTN_ERR_TX1CHU Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[6]	INTN_ERR_TX1CHL_M	1	R/W	1'h1	INTN_ERR_TX1CHL Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[5]	INTN_ERR_TX0CHU_M	1	R/W	1'h1	INTN_ERR_TX0CHU Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[4]	INTN_ERR_TX0CHL_M	1	R/W	1'h1	INTN_ERR_TX0CHL Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3]	INTN_ERR_RX1CHU_M	1	R/W	1'h1	INTN_ERR_RX1CHU Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	INTN_ERR_RX1CHL_M	1	R/W	1'h1	INTN_ERR_RX1CHL Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	INTN_ERR_RX0CHU_M	1	R/W	1'h1	INTN_ERR_RX0CHU Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_RX0CHL_M	1	R/W	1'h1	INTN_ERR_RX0CHL Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1392	[7:6]	reserved	2	-	-	-
	[5]	INTN_ERR_FPLL1CHU_M	1	R/W	1'h1	INTN_ERR_FPLL1CHU Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[4]	INTN_ERR_FPLL1CHL_M	1	R/W	1'h1	INTN_ERR_FPLL1CHL Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3]	INTN_ERR_FPLL0CHU_M	1	R/W	1'h1	INTN_ERR_FPLL0CHU Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	INTN_ERR_FPLL0CHL_M	1	R/W	1'h1	INTN_ERR_FPLL0CHL Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	INTN_ERR_OSCU_M	1	R/W	1'h1	INTN_ERR_OSCU Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_OSCL_M	1	R/W	1'h1	INTN_ERR_OSCL Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor

Address	bit	Register Name	width	R/W	Init	Description
0x13A0	[7:4]	reserved	4	-	-	-
	[3]	INTN_ERR_PATCHK_P0L0_M	1	R/W	1'h1	INTN_ERR_PATCHK_P0L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_FIFO_P0L0_M	1	R/W	1'h1	INTN_ERR_FIFO_P0L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_SOT_P0L0_M	1	R/W	1'h1	INTN_ERR_SOT_P0L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13A1	[7:4]	reserved	4	-	-	-
	[3]	INTN_ERR_PATCHK_P0L1_M	1	R/W	1'h1	INTN_ERR_PATCHK_P0L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_FIFO_P0L1_M	1	R/W	1'h1	INTN_ERR_FIFO_P0L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_SOT_P0L1_M	1	R/W	1'h1	INTN_ERR_SOT_P0L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13A2	[7:4]	reserved	4	-	-	-
	[3]	INTN_ERR_PATCHK_P0L2_M	1	R/W	1'h1	INTN_ERR_PATCHK_P0L2 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_FIFO_P0L2_M	1	R/W	1'h1	INTN_ERR_FIFO_P0L2 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_SOT_P0L2_M	1	R/W	1'h1	INTN_ERR_SOT_P0L2 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13A3	[7:4]	reserved	4	-	-	-
	[3]	INTN_ERR_PATCHK_P0L3_M	1	R/W	1'h1	INTN_ERR_PATCHK_P0L3 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_FIFO_P0L3_M	1	R/W	1'h1	INTN_ERR_FIFO_P0L3 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_SOT_P0L3_M	1	R/W	1'h1	INTN_ERR_SOT_P0L3 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13A4	[7:4]	reserved	4	-	-	-
	[3]	INTN_ERR_PATCHK_P1L0_M	1	R/W	1'h1	INTN_ERR_PATCHK_P1L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_FIFO_P1L0_M	1	R/W	1'h1	INTN_ERR_FIFO_P1L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_SOT_P1L0_M	1	R/W	1'h1	INTN_ERR_SOT_P1L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13A5	[7:4]	reserved	4	-	-	-
	[3]	INTN_ERR_PATCHK_P1L1_M	1	R/W	1'h1	INTN_ERR_PATCHK_P1L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_FIFO_P1L1_M	1	R/W	1'h1	INTN_ERR_FIFO_P1L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_SOT_P1L1_M	1	R/W	1'h1	INTN_ERR_SOT_P1L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13A6	[7:4]	reserved	4	-	-	-
	[3]	INTN_ERR_PATCHK_P1L2_M	1	R/W	1'h1	INTN_ERR_PATCHK_P1L2 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_FIFO_P1L2_M	1	R/W	1'h1	INTN_ERR_FIFO_P1L2 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_SOT_P1L2_M	1	R/W	1'h1	INTN_ERR_SOT_P1L2 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13A7	[7:4]	reserved	4	-	-	-
	[3]	INTN_ERR_PATCHK_P1L3_M	1	R/W	1'h1	INTN_ERR_PATCHK_P1L3 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_FIFO_P1L3_M	1	R/W	1'h1	INTN_ERR_FIFO_P1L3 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_SOT_P1L3_M	1	R/W	1'h1	INTN_ERR_SOT_P1L3 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor

Address	bit	Register Name	width	R/W	Init	Description
0x13B0	[7:2]	reserved	6	-	-	-
	[1]	INTN_ERR_ECC_TWO_BIT_P0_M	1	R/W	1'h1	INTN_ERR_ECC_TWO_BIT_P0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_ECC_ONE_BIT_P0_M	1	R/W	1'h1	INTN_ERR_ECC_ONE_BIT_P0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13B1	[7]	INTN_ERR_INVALID_LENGTH_P0_M	1	R/W	1'h1	INTN_ERR_INVALID_LENGTH_P0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[6]	INTN_ERR_DATA_TYPE_P0_M	1	R/W	1'h1	INTN_ERR_DATA_TYPE_P0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[5]	reserved	1	-	-	-
	[4]	INTN_ERR_FIFO_WRITE_DC_P0_M	1	R/W	1'h1	INTN_ERR_FIFO_WRITE_DC_P0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3]	INTN_ERR_FIFO_OVF_P0_M	1	R/W	1'h1	INTN_ERR_FIFO_OVF_P0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	INTN_ERR_VC_INVALID_P0_M	1	R/W	1'h1	INTN_ERR_VC_INVALID_P0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	INTN_ERR_UNCORRECT_P0_M	1	R/W	1'h1	INTN_ERR_UNCORRECT_P0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_CRC_P0_M	1	R/W	1'h1	INTN_ERR_CRC_P0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13B2	[7:1]	reserved	7	-	-	-
	[0]	INTN_TIMEOUT_HS_RX_P0_M	1	R/W	1'h1	INTN_TIMEOUT_HS_RX_P0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13B3	[7:2]	reserved	6	-	-	-
	[1]	INTN_ERR_ECC_TWO_BIT_P1_M	1	R/W	1'h1	INTN_ERR_ECC_TWO_BIT_P1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_ECC_ONE_BIT_P1_M	1	R/W	1'h1	INTN_ERR_ECC_ONE_BIT_P1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13B4	[7]	INTN_ERR_INVALID_LENGTH_P1_M	1	R/W	1'h1	INTN_ERR_INVALID_LENGTH_P1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[6]	INTN_ERR_DATA_TYPE_P1_M	1	R/W	1'h1	INTN_ERR_DATA_TYPE_P1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[5]	reserved	1	-	-	-
	[4]	INTN_ERR_FIFO_WRITE_DC_P1_M	1	R/W	1'h1	INTN_ERR_FIFO_WRITE_DC_P1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3]	INTN_ERR_FIFO_OVF_P1_M	1	R/W	1'h1	INTN_ERR_FIFO_OVF_P1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	INTN_ERR_VC_INVALID_P1_M	1	R/W	1'h1	INTN_ERR_VC_INVALID_P1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	INTN_ERR_UNCORRECT_P1_M	1	R/W	1'h1	INTN_ERR_UNCORRECT_P1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_CRC_P1_M	1	R/W	1'h1	INTN_ERR_CRC_P1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13B5	[7:1]	reserved	7	-	-	-
	[0]	INTN_TIMEOUT_HS_RX_P1_M	1	R/W	1'h1	INTN_TIMEOUT_HS_RX_P1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor

Address	bit	Register Name	width	R/W	Init	Description
0x13D0	[7:5]	reserved	3	-	-	-
	[4]	INTN_UNLOCK_VX1_L0_M	1	R/W	1'h1	INTN_UNLOCK_VX1_L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3]	INTN_ERR_MC_L0_M	1	R/W	1'h1	INTN_ERR_MC_L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	INTN_LOST_ALIVE_CMD_L0_M	1	R/W	1'h1	INTN_LOST_ALIVE_CMD_L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	INTN_LOST_1ST_ALIVE_CMD_L0_M	1	R/W	1'h1	INTN_LOST_1ST_ALIVE_CMD_L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_WDT_L0_M	1	R/W	1'h1	INTN_ERR_WDT_L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13D1	[7:0]	reserved	8	-	-	-
0x13D2	[7:5]	reserved	3	-	-	-
	[4]	INTN_UNLOCK_VX1_L1_M	1	R/W	1'h1	INTN_UNLOCK_VX1_L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3]	INTN_ERR_MC_L1_M	1	R/W	1'h1	INTN_ERR_MC_L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	INTN_LOST_ALIVE_CMD_L1_M	1	R/W	1'h1	INTN_LOST_ALIVE_CMD_L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	INTN_LOST_1ST_ALIVE_CMD_L1_M	1	R/W	1'h1	INTN_LOST_1ST_ALIVE_CMD_L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_WDT_L1_M	1	R/W	1'h1	INTN_ERR_WDT_L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13D3	[7:0]	reserved	8	-	-	-
0x13E0	[7:1]	reserved	7	-	-	-
	[0]	INTN_THRIO_VALID_L0_M	1	R/W	1'h1	INTN_THRIO_VALID_L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13E1	[7:1]	reserved	7	-	-	-
	[0]	INTN_THRIO_VALID_L1_M	1	R/W	1'h1	INTN_THRIO_VALID_L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13E2	[7:1]	reserved	7	-	-	-
	[0]	INTN_FC_GPIO_VALID_L0_M	1	R/W	1'h1	INTN_FC_GPIO_VALID_L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13E3	[7:1]	reserved	7	-	-	-
	[0]	INTN_FC_GPIO_VALID_L1_M	1	R/W	1'h1	INTN_FC_GPIO_VALID_L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13E4	[7:3]	reserved	5	-	-	-
	[2]	INTN_ERR_WRITE_L0_M	1	R/W	1'h1	INTN_ERR_WRITE_L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	INTN_ERR_CRC_OCLK_L0_M	1	R/W	1'h1	INTN_ERR_CRC_OCLK_L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_CRC_VCLK_L0_M	1	R/W	1'h1	INTN_ERR_CRC_VCLK_L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13E5	[7:3]	reserved	5	-	-	-
	[2]	INTN_ERR_WRITE_L1_M	1	R/W	1'h1	INTN_ERR_WRITE_L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	INTN_ERR_CRC_OCLK_L1_M	1	R/W	1'h1	INTN_ERR_CRC_OCLK_L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_CRC_VCLK_L1_M	1	R/W	1'h1	INTN_ERR_CRC_VCLK_L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13E6	[7:4]	reserved	4	-	-	-
	[3]	INTN_FC_BC_LINK_L0_M	1	R/W	1'h1	INTN_FC_BC_LINK_L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	INTN_CTRL_THRIO_FCDATA_L0_M	1	R/W	1'h1	INTN_CTRL_THRIO_FCDATA_L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	INTN_GPIO_VALID0_L0_M	1	R/W	1'h1	INTN_GPIO_VALID0_L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_REMORT_L0_M	1	R/W	1'h1	INTN_REMORT_L0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13E7	[7:4]	reserved	4	-	-	-
	[3]	INTN_FC_BC_LINK_L1_M	1	R/W	1'h1	INTN_FC_BC_LINK_L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	INTN_CTRL_THRIO_FCDATA_L1_M	1	R/W	1'h1	INTN_CTRL_THRIO_FCDATA_L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	INTN_GPIO_VALID0_L1_M	1	R/W	1'h1	INTN_GPIO_VALID0_L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_REMORT_L1_M	1	R/W	1'h1	INTN_REMORT_L1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor

Address	bit	Register Name	width	R/W	Init	Description
0x13F0	[7]	INTN_ERR_FCCRC_M	1	R/W	1'h1	INTN_ERR_FCCRC Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[6]	INTN_ERR_NACK_M	1	R/W	1'h1	INTN_ERR_NACK Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[5]	INTN_TIMEOUT_M	1	R/W	1'h1	INTN_TIMEOUT Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[4]	INTN_DONE_TRANS_M	1	R/W	1'h1	INTN_DONE_TRANS Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3]	INTN_FAIL_TRANS_M	1	R/W	1'h1	INTN_FAIL_TRANS Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	INTN_ERR_BCCRC_M	1	R/W	1'h1	INTN_ERR_BCCRC Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	INTN_TIMEOUT_BRIDGE_M	1	R/W	1'h1	INTN_TIMEOUT_BRIDGE Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_TIMEOUT_SLAVE_M	1	R/W	1'h1	INTN_TIMEOUT_SLAVE Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x13F1	[7:1]	reserved	7			
	[0]	INTN_REG_CHKSUM_ERR_M	1	R/W	1'h1	INTN_REG_CHKSUM_ERR Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor

Address	bit	Register Name	width	R/W	Init	Description
0x1400	[7:6]	reserved	2	-	-	-
	[5:4]	REM_INTN0_BYPASS	2	R/W	2'h2	REM_INTN0 pin output select. REM_INTN0 pin will mirror the status of INTN_IN on the Deserializer when set 0x0 and 0x1. It also outputs the enabled Interrupt signal when set to 0x2. 0x0: Mirror VbyOneHSII lane0 INTN_IN 0x1: Mirror VbyOneHSII lane1 INTN_IN 0x2: Intrrupt output 0x3: Reserved
	[3:2]	reserved	2	-	-	-
	[1:0]	REM_INTN0_MODE	2	R/W	2'h1	REM_INTN0 pin output mode select 0x0: Disable 0x1: Open drain 0x2: Push pull, Low Active 0x3: Push pull, High Active
0x1466	[7:1]	reserved	7	-	-	-
	[0]	REMOTE_L0	1	-	-	VbyOneHSII remote side interrupt error at deserializer side for lane0. This value is updated in real time. 0x0: No Error, 0x1: Error
0x1467	[7:1]	reserved	7	-	-	-
	[0]	REMOTE_L1	1	-	-	VbyOneHSII remote side interrupt error at deserializer side for lane1. This value is updated in real time. 0x0: No Error, 0x1: Error

Address	bit	Register Name	width	R/W	Init	Description
0x1500	[7:6]	reserved	2	-	-	-
	[5:4]	REM_INTN1_BYPASS	2	R/W	2'h2	REM_INTN1 pin output select. REM_INTN1 pin will mirror the status of INTN_IN on the Deserializer when set 0x0 and 0x1. It also outputs the enabled Interrupt signal when set to 0x2. 0x0: Mirror VbyOneHSII lane0 INTN_IN 0x1: Mirror VbyOneHSII lane1 INTN_IN 0x2: Intrrupt output 0x3: Reserved
	[3:2]	reserved	2	-	-	-
	[1:0]	REM_INTN1_MODE	2	R/W	2'h1	REM_INTN1 pin output mode select 0x0: Disable 0x1: Open drain 0x2: Push pull, Low Active 0x3: Push pull, High Active

Address	bit	Register Name	width	R/W	Init	Description
0x1830	[7:0]	FC_ERROR_COUNT_UPPER_L0	8	R	0	VbyOneHSII BC CRC Error Count upper bit.
0x1834	[7:0]	FC_ERROR_COUNT_LOWER_L0	8	R	0	VbyOneHSII BC CRC Error Count lower bit.
0x1838	[7:1]	reserved	7	-	-	-
	[0]	FC_ERROR_CLEAR_1-4_L0	1	R/W	0	VbyOneHSII BC CRC Error Count Clear for V-by-One HSII Lane0. After set 0x1, need to return 0x0 for restart CRC Error Count. Clear acccess should be multi-address burst access of 0x1838, 0x1839, 0x183A and 0x183B in series. 0x0: Count CRC Error 0x1: Error count set 0
0x1839	[7:1]	reserved	7	-	-	-
	[0]	FC_ERROR_CLEAR_2-4_L0	1	R/W	0	VbyOneHSII BC CRC Error Count Clear for V-by-One HSII Lane0. After set 0x1, need to return 0x0 for restart CRC Error Count. Clear acccess should be multi-address burst access of 0x1838, 0x1839, 0x183A and 0x183B in series. 0x0: Count CRC Error 0x1: Error count set 0
0x183A	[7:1]	reserved	7	-	-	-
	[0]	FC_ERROR_CLEAR_3-4_L0	1	R/W	0	VbyOneHSII BC CRC Error Count Clear for V-by-One HSII Lane0. After set 0x1, need to return 0x0 for restart CRC Error Count. Clear acccess should be multi-address burst access of 0x1838, 0x1839, 0x183A and 0x183B in series. 0x0: Count CRC Error 0x1: Error count set 0
0x183B	[7:1]	reserved	7	-	-	-
	[0]	FC_ERROR_CLEAR_4-4_L0	1	R/W	0	VbyOneHSII BC CRC Error Count Clear for V-by-One HSII Lane0. After set 0x1, need to return 0x0 for restart CRC Error Count. Clear acccess should be multi-address burst access of 0x1838, 0x1839, 0x183A and 0x183B in series. 0x0: Count CRC Error 0x1: Error count set 0

Address	bit	Register Name	width	R/W	Init	Description
0x1A30	[7:0]	FC_ERROR_COUNT_UPPER_L1	8	R	0	VbyOneHSII BC CRC Error Count upper bit.
0x1A34	[7:0]	FC_ERROR_COUNT_LOWER_L1	8	R	0	VbyOneHSII BC CRC Error Count lower bit.
0x1A38	[7:1]	reserved	7	-	-	-
	[0]	FC_ERROR_CLEAR_1-4_L1	1	R/W	0	VbyOneHSII BC CRC Error Count Clear for V-by-OneHSII Lane1. After set 0x1, need to return 0x0 for restart CRC Error Count. Clear acccess should be multi-address burst access of 0x1A38, 0x1A39, 0x1A3A and 0x1A3B in series. 0x0: Count CRC Error 0x1: Error count set 0
0x1A39	[7:1]	reserved	7	-	-	-
	[0]	FC_ERROR_CLEAR_2-4_L1	1	R/W	0	VbyOneHSII BC CRC Error Count Clear for V-by-OneHSII Lane1. After set 0x1, need to return 0x0 for restart CRC Error Count. Clear acccess should be multi-address burst access of 0x1A38, 0x1A39, 0x1A3A and 0x1A3B in series. 0x0: Count CRC Error 0x1: Error count set 0
0x1A3A	[7:1]	reserved	7	-	-	-
	[0]	FC_ERROR_CLEAR_3-4_L1	1	R/W	0	VbyOneHSII BC CRC Error Count Clear for V-by-OneHSII Lane1. After set 0x1, need to return 0x0 for restart CRC Error Count. Clear acccess should be multi-address burst access of 0x1A38, 0x1A39, 0x1A3A and 0x1A3B in series. 0x0: Count CRC Error 0x1: Error count set 0
0x1A3B	[7:1]	reserved	7	-	-	-
	[0]	FC_ERROR_CLEAR_4-4_L1	1	R/W	0	VbyOneHSII BC CRC Error Count Clear for V-by-OneHSII Lane1. After set 0x1, need to return 0x0 for restart CRC Error Count. Clear acccess should be multi-address burst access of 0x1A38, 0x1A39, 0x1A3A and 0x1A3B in series. 0x0: Count CRC Error 0x1: Error count set 0

Address	bit	Register Name	width	R/W	Init	Description
0x1C00	[7]	reserved	1	-	-	-
	[6:0]	MON0	7	R/W	7'h0	MON0 pin debug output select. See Monitor configuration table.
0x1C01	[7]	reserved	1	-	-	-
	[6:0]	MON1	7	R/W	7'h0	MON1 pin debug output select. See Monitor configuration table.
0x1C02	[7:0]	DBG_GPIO0_IOSEL	8	R/W	8'h0	GPIO0 tuning select. 0x0: Normal operation 0x01: LOCKN for FC Lane0 input Others: reserved
0x1C03	[7:0]	DBG_GPIO1_IOSEL	8	R/W	8'h0	GPIO1 tuning select. 0x0: Normal operation 0x11: Internal OSC clock output 0x12: MIPI DSI Byte Clock for port0 output 0x13: MIPI DSI Byte Clock for port1 output 0x14: VbyOneHSII Ser Clock for lane0 output 0x15: VbyOneHSII Ser Clock for lane1 output Others: reserved MIPI DSI Byte Clock[MHz] = MIPI datarate[Mbps/lane] / 8
0x1C04	[7:0]	DBG_GPIO2_IOSEL	8	R/W	8'h0	GPIO2 tuning select. 0x0: Normal operation 0x11: Internal OSC clock output 0x12: MIPI DSI Byte Clock for port0 output 0x13: MIPI DSI Byte Clock for port1 output 0x14: VbyOneHSII Ser Clock for lane0 output 0x15: VbyOneHSII Ser Clock for lane1 output Others: reserved MIPI DSI Byte Clock[MHz] = MIPI datarate[Mbps/lane] / 8
0x1C05	[7:0]	reserved	8	-	-	-
0x1C06	[7:0]	reserved	8	-	-	-
0x1C07	[7:0]	reserved	8	-	-	-
0x1C08	[7:0]	reserved	8	-	-	-
0x1C09	[7:0]	reserved	8	-	-	-
0x1C0A	[7:0]	reserved	8	-	-	-
0x1C0B	[7:0]	reserved	8	-	-	-
0x1C0C	[7:0]	reserved	8	-	-	-
0x1C0D	[7:0]	reserved	8	-	-	-
0x1C0E	[7:0]	reserved	8	-	-	-
0x1C0F	[7:0]	reserved	8	-	-	-
0x1C10	[7:0]	reserved	8	-	-	-
0x1C11	[7:0]	reserved	8	-	-	-
0x1C12	[7:0]	reserved	8	-	-	-
0x1C13	[7:0]	DIVRATIO1_TX1CLK	2	R/W	2'h0	VbyOneHSII Ser Clock for lane1 division ratio 0x0: Divided by 1 (Non divided) 0x1: Divided by 2 0x2: Divided by 4 0x3: Divided by 8
	[5:4]	DIVRATIO1_TX0CLK	2	R/W	2'h0	VbyOneHSII Ser Clock for lane0 division ratio 0x0: Divided by 1 (Non divided) 0x1: Divided by 2 0x2: Divided by 4 0x3: Divided by 8
	[3:2]	DIVRATIO1_RX1CLK	2	R/W	2'h0	MIPI DSI Byte Clock for port1 division ratio 0x0: Divided by 1 (Non divided) 0x1: Divided by 2 0x2: Divided by 4 0x3: Divided by 8
	[1:0]	DIVRATIO1_RX0CLK	2	R/W	2'h0	MIPI DSI Byte Clock for port0 division ratio 0x0: Divided by 1 (Non divided) 0x1: Divided by 2 0x2: Divided by 4 0x3: Divided by 8
0x1C14	[7:0]	reserved	8	-	-	-
0x1C15	[7:6]	reserved	2	-	-	-
	[5:3]	FREF1SEL	3	R/W	3'h0	FC Lane1 clock reference select 0x0: Normal operation 0x4: Internal oscillator clock Others: reserved
	[2:0]	FREF0SEL	3	R/W	3'h0	FC Lane0 clock reference select 0x0: Normal operation 0x4: Internal oscillator clock Others: reserved
0x1C16	[7:0]	reserved	8	-	-	-
0x1C17	[7:0]	reserved	8	-	-	-
0x1C18	[7:4]	reserved	4	-	-	-
	[3:2]	LOCKN_CTRL1	2	R/W	2'h0	VbyOneHSII Lane1 CDR LOCKN select 0x0: Normal operation, from BCC 0x1: External input from GPIOx 0x2: Low fix, Fix CDR Lock 0x3: High fix, Fix CDR Unlock
	[1:0]	LOCKN_CTRL0	2	R/W	2'h0	VbyOneHSII Lane0 CDR LOCKN select 0x0: Normal operation, from BCC 0x1: External input from GPIOx 0x2: Low fix, Fix CDR Lock 0x3: High fix, Fix CDR Unlock

Table 25. Monitor configuration table (1/2)

MON0/1[7:0]	Output signal	Description
0x00	-	-
0x01	-	-
0x02	H-fix	-
0x03	L-fix	-
0x04	Reserved	-
0x05	Reserved	-
0x06	Reserved	-
0x07	Reserved	-
0x08	Reserved	-
0x09	Reserved	-
0x0A	Reserved	-
0x0B	Reserved	-
0x0C	FCTX_BCRX_LINK_1.VSYNC0	VbyOneHSII Ser VSYNC for lane0
0x0D	FCTX_BCRX_LINK_1.HSYNC0	VbyOneHSII Ser HSYNC for lane0
0x0E	FCTX_BCRX_LINK_1.DE0	VbyOneHSII Ser DE for lane0
0x0F	Reserved	-
0x10	Reserved	-
0x11	Reserved	-
0x12	Reserved	-
0x13	Reserved	-
0x14	Reserved	-
0x15	FCTX_BCRX_LINK_2.VSYNC0	VbyOneHSII Ser VSYNC for lane1
0x16	FCTX_BCRX_LINK_2.HSYNC0	VbyOneHSII Ser HSYNC for lane1
0x17	FCTX_BCRX_LINK_2.DE0	VbyOneHSII Ser DE for lane1
0x18	U_DSI_WR0.RHSD0[0]	DSI port0 lane0 [0] Data
0x19	U_DSI_WR0.RHSD0[1]	DSI port0 lane0 [1] Data
0x1A	U_DSI_WR0.RHSD0[2]	DSI port0 lane0 [2] Data
0x1B	U_DSI_WR0.RHSD0[3]	DSI port0 lane0 [3] Data
0x1C	U_DSI_WR0.RHSD0[4]	DSI port0 lane0 [4] Data
0x1D	U_DSI_WR0.RHSD0[5]	DSI port0 lane0 [5] Data
0x1E	U_DSI_WR0.RHSD0[6]	DSI port0 lane0 [6] Data
0x1F	U_DSI_WR0.RHSD0[7]	DSI port0 lane0 [7] Data
0x20	U_DSI_WR0.RHSD1[0]	DSI port0 lane1 [0] Data
0x21	U_DSI_WR0.RHSD1[1]	DSI port0 lane1 [1] Data
0x22	U_DSI_WR0.RHSD1[2]	DSI port0 lane1 [2] Data
0x23	U_DSI_WR0.RHSD1[3]	DSI port0 lane1 [3] Data
0x24	U_DSI_WR0.RHSD1[4]	DSI port0 lane1 [4] Data
0x25	U_DSI_WR0.RHSD1[5]	DSI port0 lane1 [5] Data
0x26	U_DSI_WR0.RHSD1[6]	DSI port0 lane1 [6] Data
0x27	U_DSI_WR0.RHSD1[7]	DSI port0 lane1 [7] Data
0x28	U_DSI_WR0.RHSD2[0]	DSI port0 lane2 [0] Data
0x29	U_DSI_WR0.RHSD2[1]	DSI port0 lane2 [1] Data
0x2A	U_DSI_WR0.RHSD2[2]	DSI port0 lane2 [2] Data
0x2B	U_DSI_WR0.RHSD2[3]	DSI port0 lane2 [3] Data
0x2C	U_DSI_WR0.RHSD2[4]	DSI port0 lane2 [4] Data
0x2D	U_DSI_WR0.RHSD2[5]	DSI port0 lane2 [5] Data
0x2E	U_DSI_WR0.RHSD2[6]	DSI port0 lane2 [6] Data
0x2F	U_DSI_WR0.RHSD2[7]	DSI port0 lane2 [7] Data
0x30	U_DSI_WR0.RHSD3[0]	DSI port0 lane3 [0] Data
0x31	U_DSI_WR0.RHSD3[1]	DSI port0 lane3 [1] Data
0x32	U_DSI_WR0.RHSD3[2]	DSI port0 lane3 [2] Data
0x33	U_DSI_WR0.RHSD3[3]	DSI port0 lane3 [3] Data
0x34	U_DSI_WR0.RHSD3[4]	DSI port0 lane3 [4] Data
0x35	U_DSI_WR0.RHSD3[5]	DSI port0 lane3 [5] Data
0x36	U_DSI_WR0.RHSD3[6]	DSI port0 lane3 [6] Data
0x37	U_DSI_WR0.RHSD3[7]	DSI port0 lane3 [7] Data

Table 26. Monitor configuration table (continued 2/2)

MON0/1[7:0]	Output signal	Description
0x38	U_DSI_WR1.RHSD0[0]	DSI port1 lane0 [0] Data
0x39	U_DSI_WR1.RHSD0[1]	DSI port1 lane0 [1] Data
0x3A	U_DSI_WR1.RHSD0[2]	DSI port1 lane0 [2] Data
0x3B	U_DSI_WR1.RHSD0[3]	DSI port1 lane0 [3] Data
0x3C	U_DSI_WR1.RHSD0[4]	DSI port1 lane0 [4] Data
0x3D	U_DSI_WR1.RHSD0[5]	DSI port1 lane0 [5] Data
0x3E	U_DSI_WR1.RHSD0[6]	DSI port1 lane0 [6] Data
0x3F	U_DSI_WR1.RHSD0[7]	DSI port1 lane0 [7] Data
0x40	U_DSI_WR1.RHSD1[0]	DSI port1 lane1 [0] Data
0x41	U_DSI_WR1.RHSD1[1]	DSI port1 lane1 [1] Data
0x42	U_DSI_WR1.RHSD1[2]	DSI port1 lane1 [2] Data
0x43	U_DSI_WR1.RHSD1[3]	DSI port1 lane1 [3] Data
0x44	U_DSI_WR1.RHSD1[4]	DSI port1 lane1 [4] Data
0x45	U_DSI_WR1.RHSD1[5]	DSI port1 lane1 [5] Data
0x46	U_DSI_WR1.RHSD1[6]	DSI port1 lane1 [6] Data
0x47	U_DSI_WR1.RHSD1[7]	DSI port1 lane1 [7] Data
0x48	U_DSI_WR1.RHSD2[0]	DSI port1 lane2 [0] Data
0x49	U_DSI_WR1.RHSD2[1]	DSI port1 lane2 [1] Data
0x4A	U_DSI_WR1.RHSD2[2]	DSI port1 lane2 [2] Data
0x4B	U_DSI_WR1.RHSD2[3]	DSI port1 lane2 [3] Data
0x4C	U_DSI_WR1.RHSD2[4]	DSI port1 lane2 [4] Data
0x4D	U_DSI_WR1.RHSD2[5]	DSI port1 lane2 [5] Data
0x4E	U_DSI_WR1.RHSD2[6]	DSI port1 lane2 [6] Data
0x4F	U_DSI_WR1.RHSD2[7]	DSI port1 lane2 [7] Data
0x50	U_DSI_WR1.RHSD3[0]	DSI port1 lane3 [0] Data
0x51	U_DSI_WR1.RHSD3[1]	DSI port1 lane3 [1] Data
0x52	U_DSI_WR1.RHSD3[2]	DSI port1 lane3 [2] Data
0x53	U_DSI_WR1.RHSD3[3]	DSI port1 lane3 [3] Data
0x54	U_DSI_WR1.RHSD3[4]	DSI port1 lane3 [4] Data
0x55	U_DSI_WR1.RHSD3[5]	DSI port1 lane3 [5] Data
0x56	U_DSI_WR1.RHSD3[6]	DSI port1 lane3 [6] Data
0x57	U_DSI_WR1.RHSD3[7]	DSI port1 lane3 [7] Data

8. Application and Implementation

NOTE

Information in the following applications sections is not part of the THine component specification, and THine does not warrant its accuracy or completeness. THine's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1. Applications Information

V-by-One® HSII behavior is connectable to V-by-One® HSII receiver like THCV334-Q.

V-by-One® HS behavior, in which FCTHRIO is disabled, is connectable to standard V-by-One® HS product with external LOCKN connection.

8.2. Typical Applications

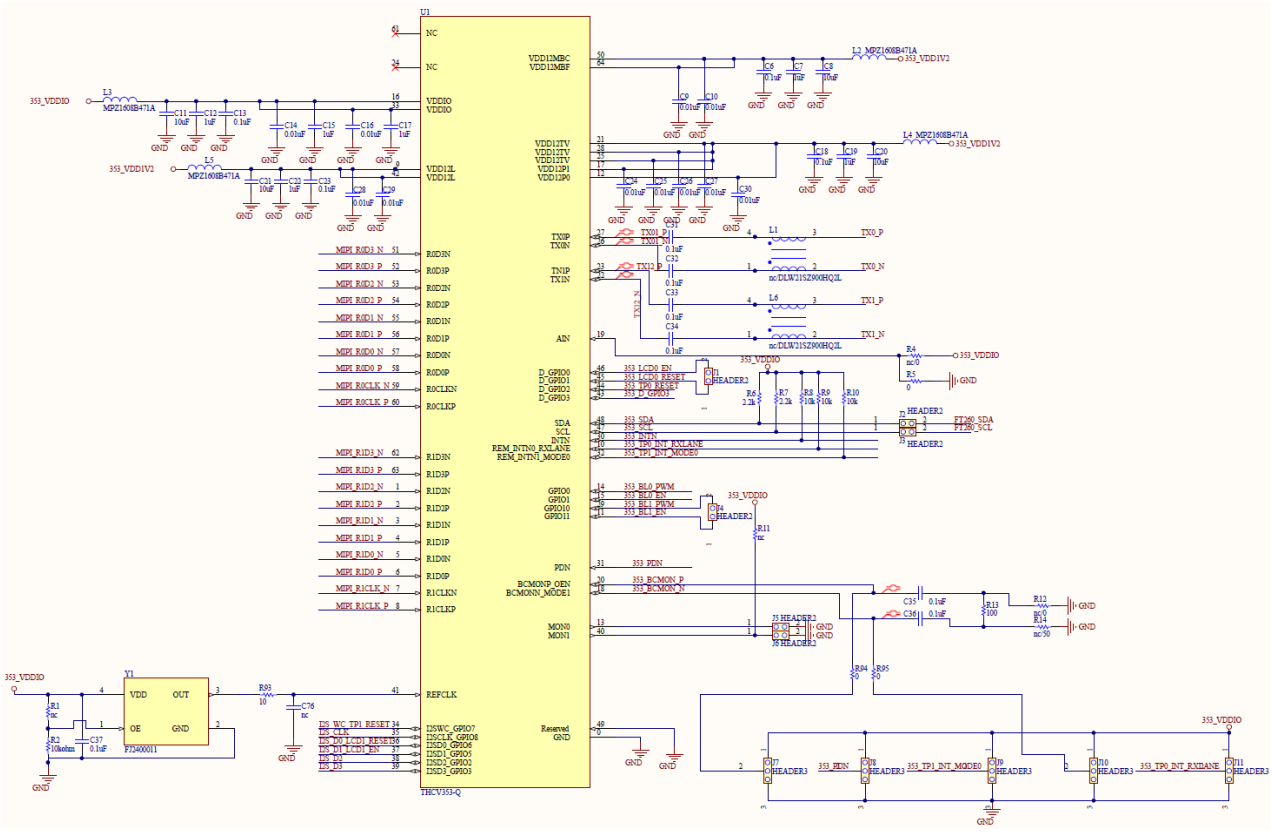


Figure 34. Typical Application Schematic

8.2.1. Design Requirements

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme.

For applications utilizing single-ended 50Ω coaxial cable, the unused data pins should be terminated with a 50Ω resistor.

8.2.2. Detailed Design Procedure

8.2.2.1. High-Speed Interconnect Guidelines

- ☐ Use at least four-layer PCBs with signals, ground, power, and signals assigned for each layer. (Refer to figure below.)
- ☐ PCB traces for high-speed signals must be single-ended micorstirp lines or coupled microstrip lines whose differential characteristic impedance is 100Ω.
- ☐ Minimize the distance between traces of a differential pair (S1) to maximize common mode rejection and coupling effect which works to reduce EMI(Electro-Magnetic Interference).
- ☐ Route differential signal traces symmetrically.
- ☐ Avoid right-angle turns or minimize the number of vias on the high speed traces because they usually cause impedance discontinuity in the transmission lines and degrade the signal integrity.
- ☐ Mismatch among impedances of PCB traces, connectors, or cables also caused reflection, limiting the bandwidth of the high-speed channels.
- ☐ Using common-mode filter on differential traces is desirable to reduce EMI. Pay attention on data-rate driven noise. For example, if data-rate is 1.5Gbps, common mode choke coil of 1.5GHz common mode impedance is desired to be high, while 1.5GHz differential impedance is low.

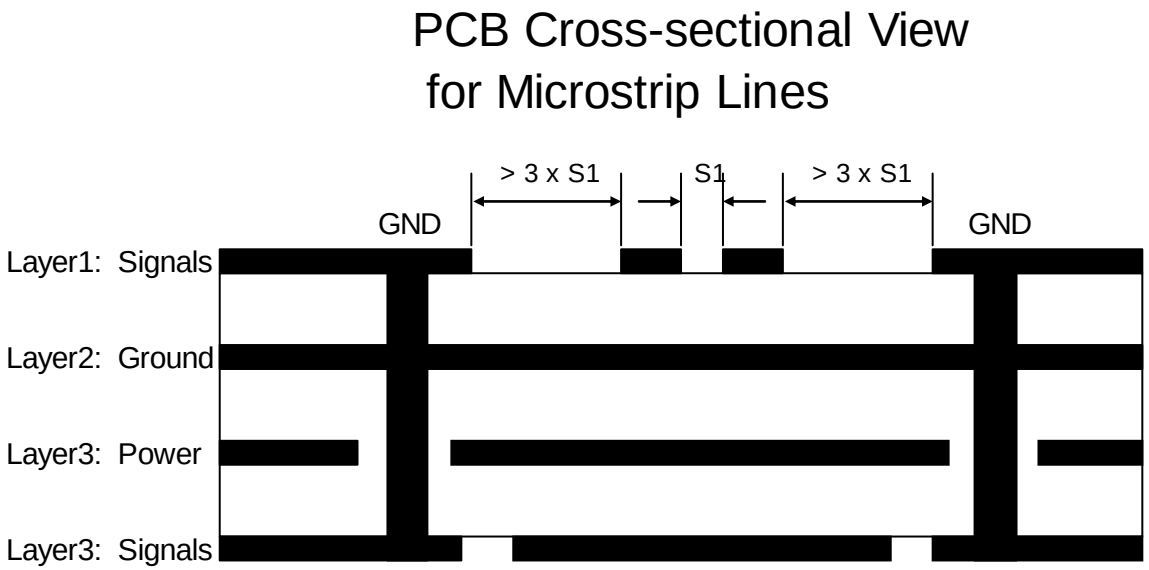


Figure 35. PCB Cross-sectional View

9. Power Supply Recommendations

9.1. Power-Up Requirements and PDN Pin

Please refer to 6.6.6 Power On and Lock/Re-Lock Sequence AC Specifications.

10. Layout

10.1. Layout Guidelines

Use at least four-layer PCBs with signals, ground, power, and signals assigned for each layer.

10.2. Layout Example

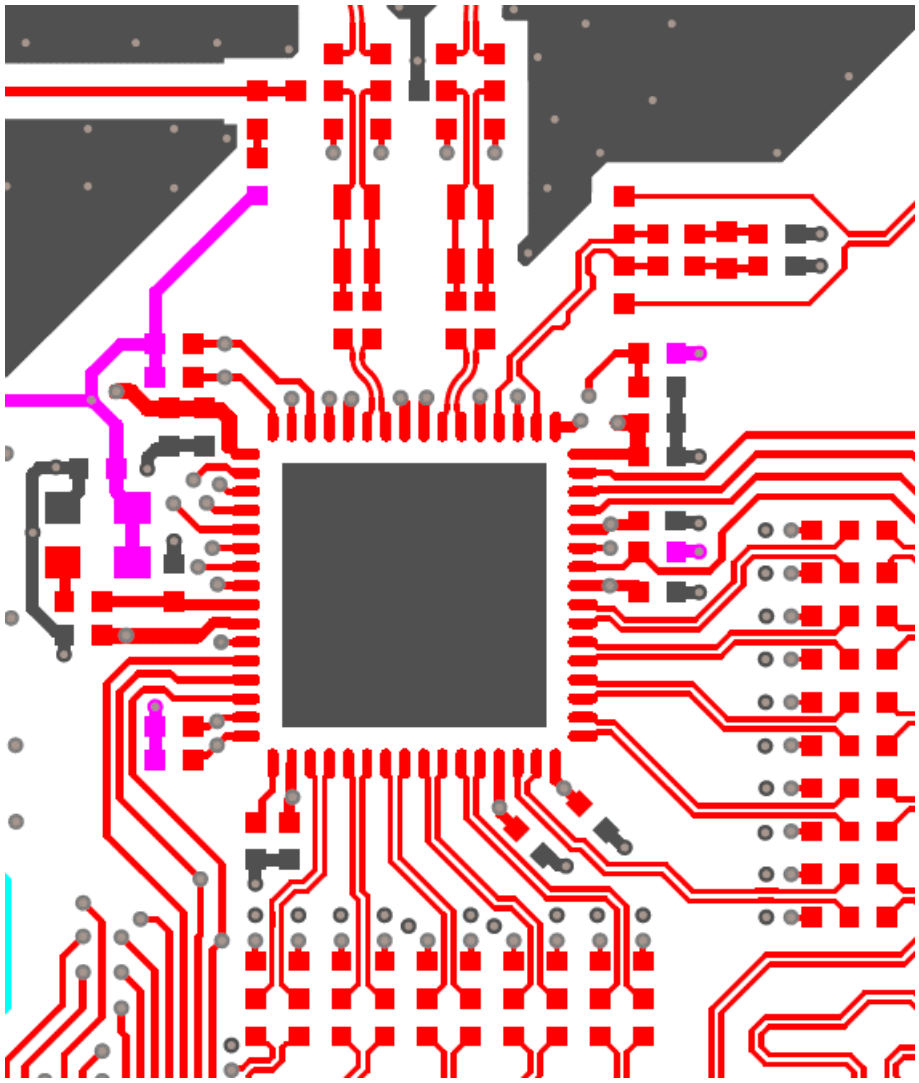


Figure 36. Layout Example

11. Package

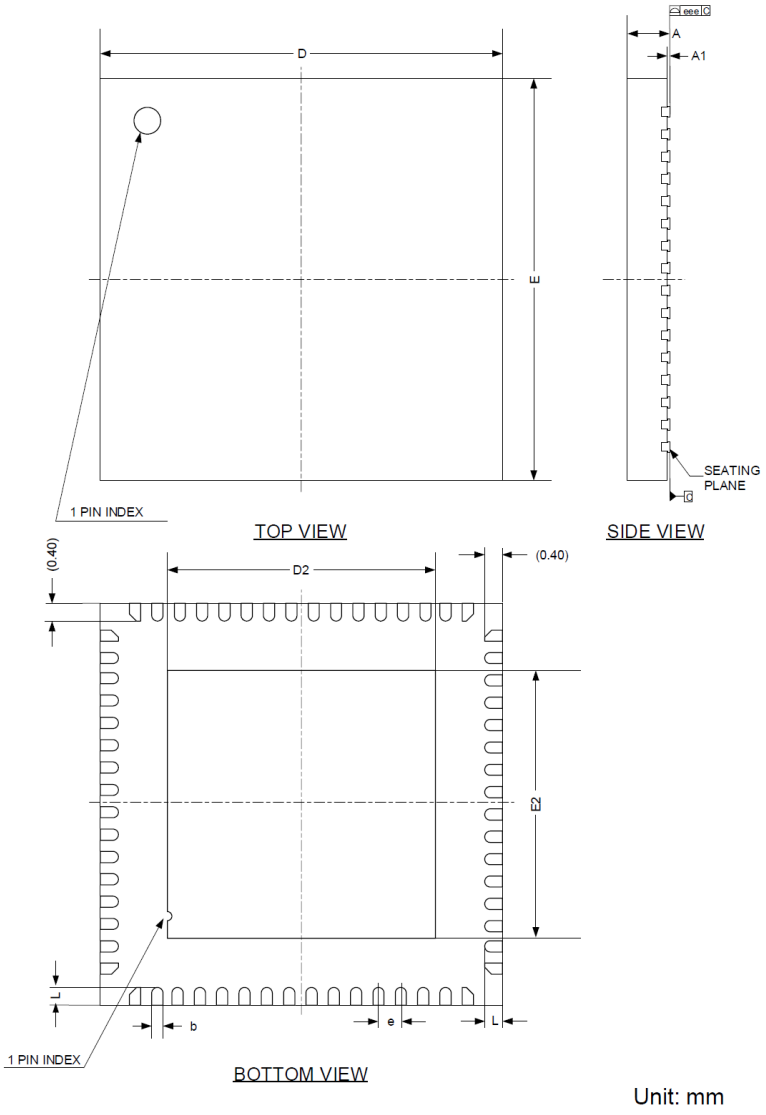


Figure 37. Package Outline

Table 27. Package Outline Dimensions

Symbol	Items	Min.	Nom.	Max.
A	Mounting Height	-	-	0.90
A1	Standoff	0.00	-	0.05
b	Terminal Width	0.18	0.25	0.30
D	Body Length		9.00 BSC	
D2	Exposed Length	5.90	6.00	6.10
E	Body Width		9.00 BSC	
E2	Exposed Width	5.90	6.00	6.10
L	-	0.30	0.40	0.50
e	Pitch		0.50 BSC	
eee	Coplanarity		0.08	

12. Land Pattern

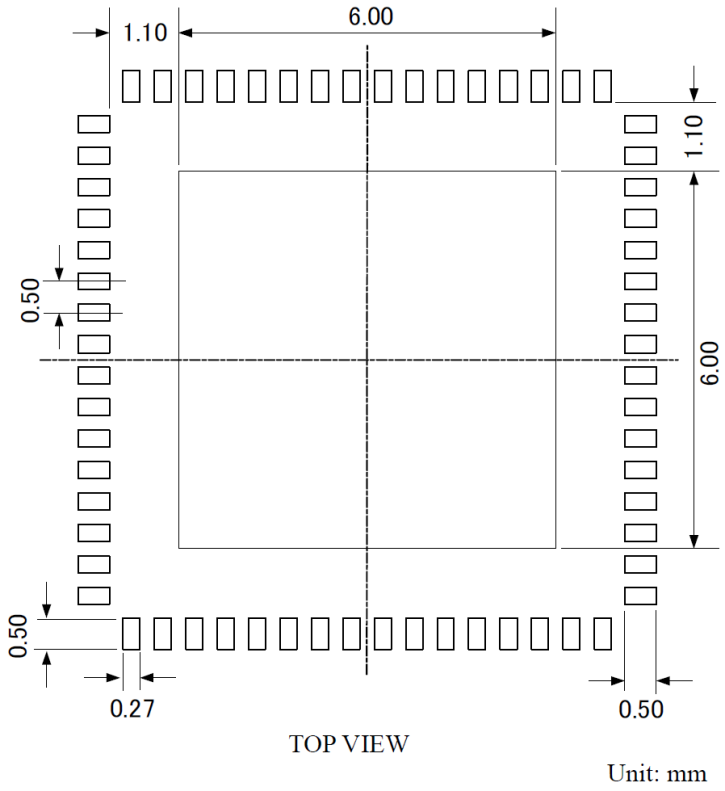


Figure 38. Reference Land Pattern

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7. This product may be permanently damaged and suffer from performance degradation or loss of mechanical functionality if subjected to electrostatic charge exceeding capacity of the ESD (Electrostatic Discharge) protection circuitry. Safety earth ground must be provided to anything in contact with the product, including any operator, floor, tester and soldering iron.

8. Please note that this product is not designed to be radiation-proof.

9. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.

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12. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses. THine accepts no liability whatsoever for any damage or loss caused to the user due to use under a condition exceeding the limiting values.

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