8-bit Serial-in, Parallel-out Shift Register

CJ74HC/HCT164 Logic

1 Introduction

The CJ74HC/HCT164 is an 8-bit serial-in/parallel-out shift register. The device features two serial data inputs (DSA and DSB), eight parallel data outputs (Q0 to Q7). Data is entered serially through DSA or DSB and either input can be used as an active HIGH enable for data entry through the other input. Data is shifted on the LOW-to-HIGH transitions of the clock (CP) input. A LOW on the master reset input (MR) clears the register and forces all outputs LOW, independently of other inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2 Available Packages

PART NUMBER	PACKAGE
CJ74HC164	SOP14
	TSSOP14
CJ74HCT164	SOP14
	TSSOP14

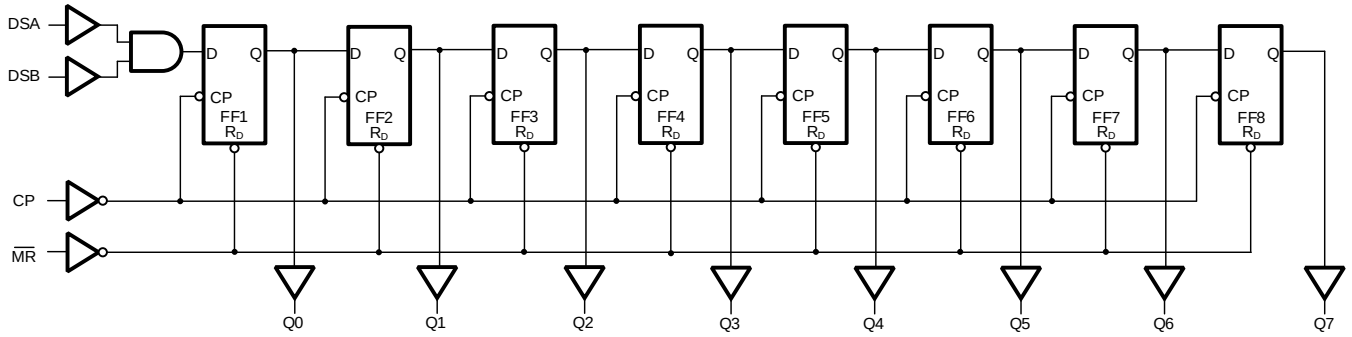
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Input levels:
  - For CJ74HC164: CMOS level
  - For CJ74HCT164: TTL level
- Gated serial data inputs
- Asynchronous master reset
- Specified from -40°C to +125°C

4 Applications

- Programable Logic Controllers
- Appliances
- Video Display Systems
- Output Expander



Function diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74HC164ADN	SOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HCT164ADN	SOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HC164BDN	TSSOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active
CJ74HCT164BDN	TSSOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

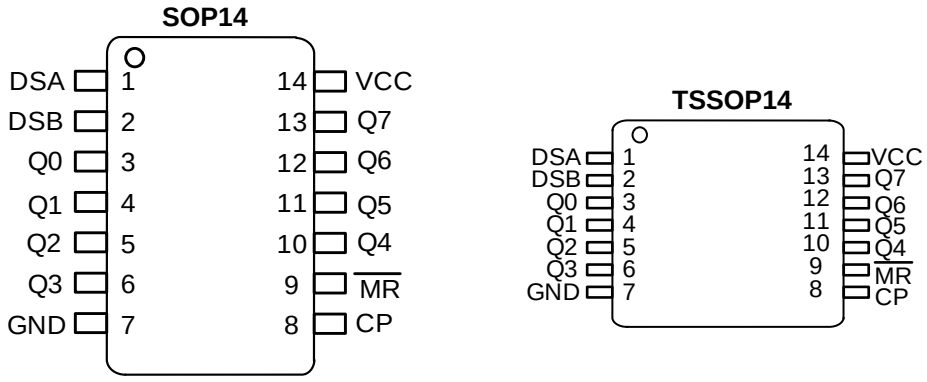


Figure 6-1 Pin Configuration

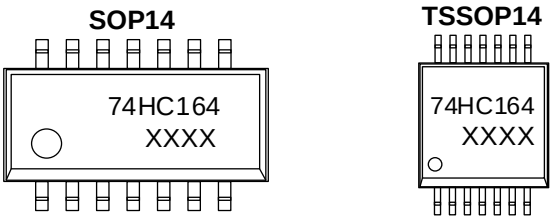
6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	DSA	I	Data input
2	DSB	I	Data input
3	Q0	O	Output
4	Q1	O	Output
5	Q2	O	Output
6	Q3	O	Output
7	GND	G	Ground (0V)
8	CP	I	Clock input (LOW-to-HIGH, edge-triggered)
9	$\overline{MR}$	I	Master reset input (active LOW)
10	Q4	O	Output
11	Q5	O	Output
12	Q6	O	Output
13	Q7	O	Output
14	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information

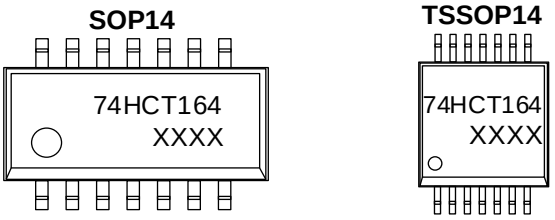
6.3.1 CJ74HC164



74HC164: Device number.

XXXX: Code, indicates weekly record information.

6.3.2 CJ74HCT164



74HCT164: Device number.

XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-		-0.5	+7.0	V
I_{IK}	Input clamping current	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$		-	±20	mA
I_{OK}	Output clamping current	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$		-	±20	mA
I_O	Output current	$-0.5V < V_O < V_{CC}+0.5V$		-	±25	mA
I_{CC}	Supply current	-		-	50	mA
I_{GND}	Ground current	-		-50	-	mA
P_{tot}	Total power dissipation	-		-	500	mW
T_{stg}	Storage temperature	-		-65	+150	°C
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC164						
V_{CC}	Supply voltage	-	2.0	5.0	6.0	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
Δt/ΔV	Input transition rise and fall rate	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
T_{amb}	Ambient temperature	-	-40	-	+125	°C
CJ74HCT164						
V_{CC}	Supply voltage	-	4.5	5.0	5.5	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
Δt/ΔV	Input transition rise and fall rate	V_{CC}=4.5V	-	1.67	139	ns/V
T_{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM)(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC164							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8	uA
C_I	Input capacitance	-		-	3.5	-	pF
CJ74HCT164							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	1.6	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	1.2	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.15	0.26	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	8	uA
ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-2.1V; I_O=0A; Other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V		-	-	360	uA
C_I	Input capacitance	-		-	3.5	-	pF

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC164							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
CJ74HCT164							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.84	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-2.1V; I_O=0A; Other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V		-	-	450	uA

7.4.3 DC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC164							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
CJ74HCT164							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	160	uA
ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-2.1V; I_O=0A; Other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V		-	-	490	uA

7.4.4 AC Characteristics 1

T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC164							
t_{pd}(1)	CP to Qn propagation delay	See Figure 8-6	V_{CC}=2.0V	-	41	170	ns
			V_{CC}=4.5V	-	15	34	ns
			V_{CC}=5.0V; C_L=15pF	-	12	-	ns
			V_{CC}=6.0V	-	12	29	ns
t_{PHL}	$\overline{MR}$ to Qn propagation delay	See Figure 8-7	V_{CC}=2.0V	-	39	140	ns
			V_{CC}=4.5V	-	14	28	ns
			V_{CC}=5.0V; C_L=15pF	-	11	-	ns
			V_{CC}=6.0V	-	11	24	ns
t_t(2)	Transition time	See Figure 8-6	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
t_W	CP pulse width	See Figure 8-6	V_{CC}=2.0V	80	14	-	ns
			V_{CC}=4.5V	16	5	-	ns
			V_{CC}=6.0V	14	4	-	ns
t_W	$\overline{MR}$ pulse width	See Figure 8-7	V_{CC}=2.0V	60	17	-	ns
			V_{CC}=4.5V	12	6	-	ns
			V_{CC}=6.0V	10	5	-	ns
t_{rec}	$\overline{MR}$ to CP recovery time	See Figure 8-7	V_{CC}=2.0V	60	17	-	ns
			V_{CC}=4.5V	12	6	-	ns
			V_{CC}=6.0V	10	5	-	ns
t_{su}	DSA and DSB to CP set-up time	See Figure 8-8	V_{CC}=2.0V	60	8	-	ns
			V_{CC}=4.5V	12	3	-	ns
			V_{CC}=6.0V	10	2	-	ns
t_h	DSA and DSB to CP hold time	See Figure 8-8	V_{CC}=2.0V	+4	-6	-	ns
			V_{CC}=4.5V	+4	-2	-	ns
			V_{CC}=6.0V	+4	-2	-	ns
f_{max}	CP maximum frequency	See Figure 8-6	V_{CC}=2.0V	6	23	-	MHz
			V_{CC}=4.5V	30	71	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	78	-	MHz
			V_{CC}=6.0V	35	85	-	MHz
C_{PD}(3)	Power dissipation capacitance	Per package; V_I= GND to V_{CC}		-	40	-	pF
CJ74HCT164							
t_{pd}	CP to Qn propagation delay	See Figure 8-6	V_{CC}=4.5V	-	17	36	ns
			V_{CC}=5.0V; C_L=15pF	-	14	-	ns

t_{PHL}	$\overline{MR}$ to Qn propagation delay	See Figure 8-7	V_{CC}=4.5V	-	19	38	ns
			V_{CC}=5.0V; C_L=15pF	-	16	-	ns
t_t	Transition time	See Figure 8-6	V_{CC}=4.5V	-	7	15	ns
t_W	CP pulse width	See Figure 8-6	V_{CC}=4.5V	18	7	-	ns
t_W	$\overline{MR}$ pulse width	See Figure 8-7	V_{CC}=4.5V	18	10	-	ns
t_{rec}	$\overline{MR}$ to CP recovery time	See Figure 8-7	V_{CC}=4.5V	16	7	-	ns
t_{su}	DSA and DSB to CP set-up time	See Figure 8-7	V_{CC}=4.5V	12	6	-	ns
t_h	DSA and DSB to CP hold time	See Figure 8-8	V_{CC}=4.5V	+4	-2	-	ns
f_{max}	CP maximum frequency	See Figure 8-8	V_{CC}=4.5V	27	55	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	61	-	MHz
C_{PD}	Power dissipation capacitance	Per package; V_I= GND to V_{CC}-1.5V		-	40	-	pF

(1) t_{pd} is the same as t_{PLH} and t_{PHL}.

(2) t_t is the same as t_{THL} and t_{TLH}.

(3) C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=(C_{PD}xV_{CC}^2xf_ixN)+\sum(C_LxV_{CC}^2xf_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_LxV_{CC}^2xf_o)$=sum of outputs.

7.4.5 AC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC164							
t_{pd}(1)	CP to Qn propagation delay	See Figure 8-6	V_{CC}=2.0V	-	-	215	ns
			V_{CC}=4.5V	-	-	43	ns
			V_{CC}=6.0V	-	-	37	ns
t_{PHL}	$\overline{MR}$ to Qn propagation delay	See Figure 8-7	V_{CC}=2.0V	-	-	175	ns
			V_{CC}=4.5V	-	-	35	ns
			V_{CC}=6.0V	-	-	30	ns
t_t(2)	Transition time	See Figure 8-6	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	16	ns
t_W	CP pulse width	See Figure 8-6	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
t_W	$\overline{MR}$ pulse width	See Figure 8-7	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns

			V_{CC}=6.0V	13	-	-	ns
t_{rec}	$\overline{MR}$ to CP recovery time	See Figure 8-7	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
t_{su}	DSA and DSB to CP set-up time	See Figure 8-8	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
t_h	DSA and DSB to CP hold time	See Figure 8-8	V_{CC}=2.0V	4	-	-	ns
			V_{CC}=4.5V	4	-	-	ns
			V_{CC}=6.0V	4	-	-	ns
f_{max}	CP maximum frequency	See Figure 8-6	V_{CC}=2.0V	5	-	-	MHz
			V_{CC}=4.5V	24	-	-	MHz
			V_{CC}=6.0V	28	-	-	MHz
CJ74HCT164							
t_{pd}	CP to Qn propagation delay	See Figure 8-6	V_{CC}=4.5V	-	-	45	ns
t_{PHL}	$\overline{MR}$ to Qn propagation delay	See Figure 8-7	V_{CC}=4.5V	-	-	48	ns
t_t	Transition time	See Figure 8-6	V_{CC}=4.5V	-	-	19	ns
t_W	CP pulse width	See Figure 8-6	V_{CC}=4.5V	23	-	-	ns
t_W	$\overline{MR}$ pulse width	See Figure 8-7	V_{CC}=4.5V	23	-	-	ns
t_{rec}	$\overline{MR}$ to CP recovery time	See Figure 8-7	V_{CC}=4.5V	20	-	-	ns
t_{su}	DSA and DSB to CP set-up time	See Figure 8-8	V_{CC}=4.5V	15	-	-	ns
t_h	DSA and DSB to CP hold time	See Figure 8-8	V_{CC}=4.5V	+4	-	-	ns
f_{max}	CP maximum frequency	See Figure 8-6	V_{CC}=4.5V	22	-	-	MHz

(1) t_{pd} is the same as t_{PLH} and t_{PHL}.

(2) t_t is the same as t_{THL} and t_{TLH}.

7.4.6 AC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC164							
t_{pd}(1)	CP to Qn propagation delay	See Figure 8-6	V_{CC}=2.0V	-	-	255	ns
			V_{CC}=4.5V	-	-	51	ns
			V_{CC}=6.0V	-	-	43	ns
t_{PHL}	$\overline{MR}$ to Qn propagation delay	See Figure 8-7	V_{CC}=2.0V	-	-	210	ns
			V_{CC}=4.5V	-	-	42	ns
			V_{CC}=6.0V	-	-	36	ns
t_t(2)	Transition time	See Figure 8-6	V_{CC}=2.0V	-	-	110	ns
			V_{CC}=4.5V	-	-	22	ns

			V_{CC}=6.0V	-	-	19	ns
t_W	CP pulse width	See Figure 8-6	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
t_W	$\overline{MR}$ pulse width	See Figure 8-7	V_{CC}=2.0V	90	-	-	ns
			V_{CC}=4.5V	18	-	-	ns
			V_{CC}=6.0V	15	-	-	ns
t_{rec}	$\overline{MR}$ to CP recovery time	See Figure 8-7	V_{CC}=2.0V	90	-	-	ns
			V_{CC}=4.5V	18	-	-	ns
			V_{CC}=6.0V	15	-	-	ns
t_{su}	DSA and DSB to CP set-up time	See Figure 8-8	V_{CC}=2.0V	90	-	-	ns
			V_{CC}=4.5V	18	-	-	ns
			V_{CC}=6.0V	15	-	-	ns
t_h	DSA and DSB to CP hold time	See Figure 8-8	V_{CC}=2.0V	4	-	-	ns
			V_{CC}=4.5V	4	-	-	ns
			V_{CC}=6.0V	4	-	-	ns
f_{max}	CP maximum frequency	See Figure 8-6	V_{CC}=2.0V	5	-	-	MHz
			V_{CC}=4.5V	20	-	-	MHz
			V_{CC}=6.0V	24	-	-	MHz
CJ74HCT164							
t_{pd}	CP to Qn propagation delay	See Figure 8-6	V_{CC}=4.5V	-	-	54	ns
t_{PHL}	$\overline{MR}$ to Qn propagation delay	See Figure 8-7	V_{CC}=4.5V	-	-	57	ns
t_t	transition time	See Figure 8-6	V_{CC}=4.5V	-	-	22	ns
t_W	CP pulse width	See Figure 8-6	V_{CC}=4.5V	27	-	-	ns
t_W	$\overline{MR}$ pulse width	See Figure 8-7	V_{CC}=4.5V	27	-	-	ns
t_{rec}	$\overline{MR}$ to CP recovery time	See Figure 8-7	V_{CC}=4.5V	24	-	-	ns
t_{su}	DSA and DSB to CP set-up time	See Figure 8-8	V_{CC}=4.5V	18	-	-	ns
t_h	DSA and DSB to CP hold time	See Figure 8-8	V_{CC}=4.5V	4	-	-	ns
f_{max}	CP maximum frequency	See Figure 8-6	V_{CC}=4.5V	18	-	-	MHz

(1) t_{pd} is the same as t_{PLH} and t_{PHL}.

(2) t_t is the same as t_{THL} and t_{TLH}.

8 Detailed Description

8.1 Overview

The CJ74HC/HCT164 is an 8-bit serial-in/parallel-out shift register. The device features two serial data inputs (DSA and DSB), eight parallel data outputs (Q0 to Q7). Data is entered serially through DSA or DSB and either input can be used as an active HIGH enable for data entry through the other input. Data is shifted on the LOW-to-HIGH transitions of the clock (CP) input. A LOW on the master reset input (MR) clears the register and forces all outputs LOW, independently of other inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

8.2 Functional Block Diagram

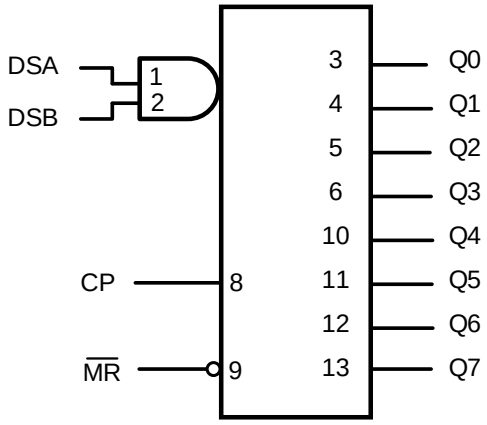


Figure 8-1 Logic symbol

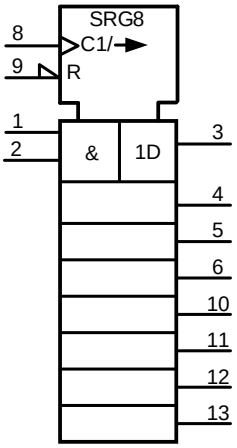


Figure 8-2 IEC logic symbol

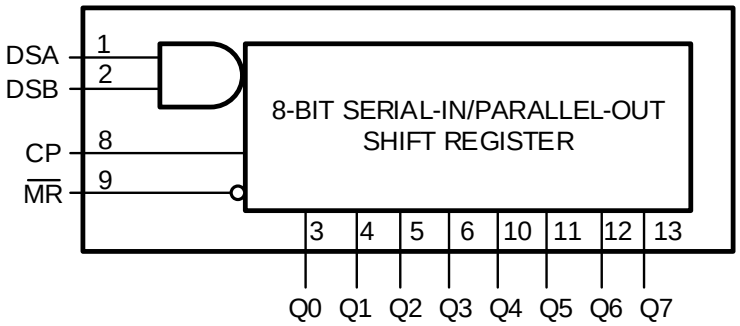


Figure 8-3 Logic diagram

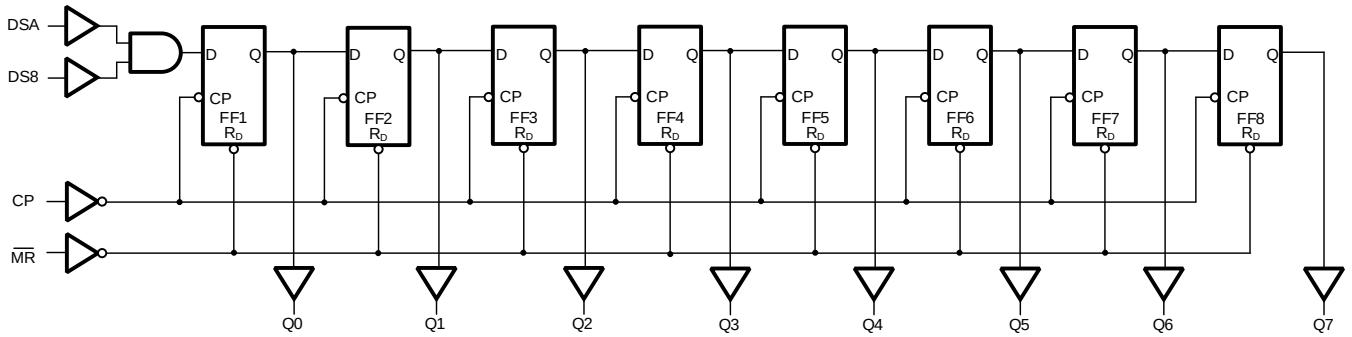


Figure 8-4 Function diagram

8.3 Function Table(1)

OPERATING MODES	INPUT				OUTPUT	
	$\overline{MR}$	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	l	h	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	H	q0 to q6

(1) H=HIGH voltage level; L=LOW voltage level; ↑=LOW-to-HIGH clock transition;
h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
q=lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

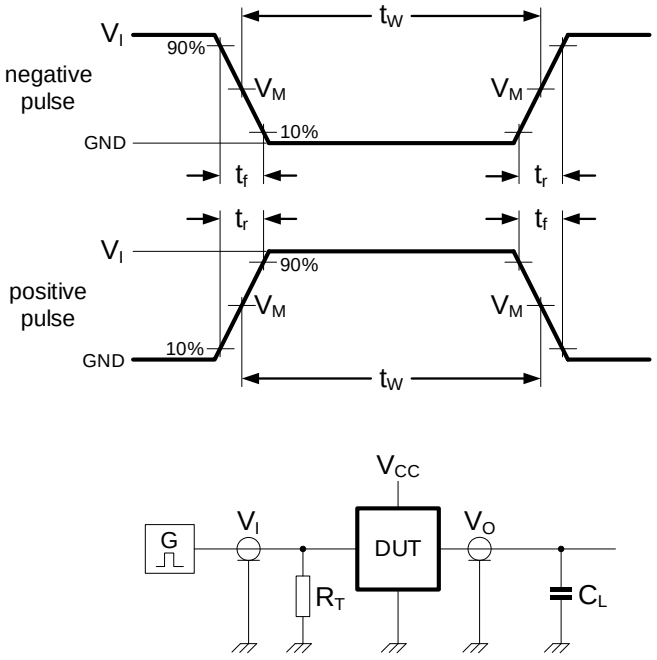


Figure 8-5 Test circuit for measuring switching times

Definitions for test circuit:

C_L=load capacitance including jig and probe capacitance.

R_T=termination resistance should be equal to the output impedance Z_o of the pulse generator.

8.4.2 AC Testing Waveforms

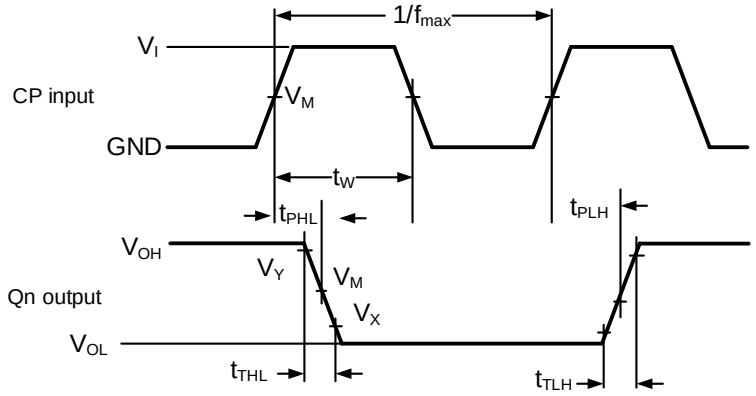


Figure 8-6 Waveforms showing the clock (CP) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency

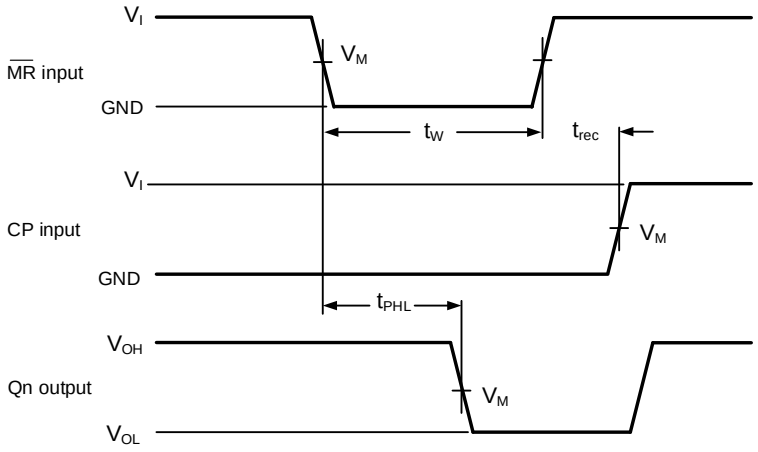


Figure 8-7 Waveforms showing the master reset (MR) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock (CP) removal time

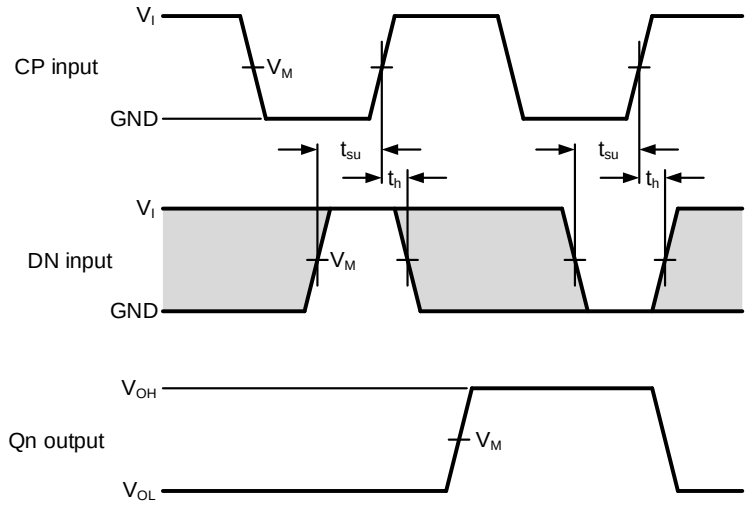


Figure 8-8 Waveforms showing the data set-up and hold times for Dn inputs

8.4.3 Measurement Points

TYPE	INPUT	OUTPUT		
	V_M	V_M	V_X	V_Y
CJ74HC164	0.5xV_{CC}	0.5xV_{CC}	0.1xV_{CC}	0.9xV_{CC}
CJ74HCT164	1.3V	1.3V	0.1xV_{CC}	0.9xV_{CC}

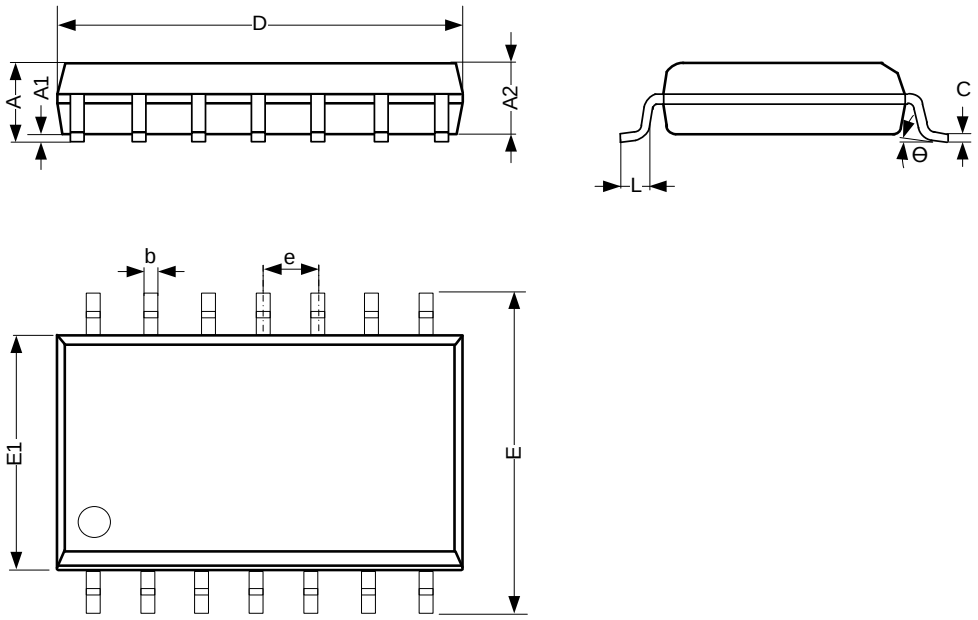
8.4.4 Test Data

TYPE	INPUT		LOAD	TEST
	V_I	t_r , t_f	C_L	
CJ74HC164	V_{CC}	6.0ns	15pF, 50pF	t_{PLH}, t_{PHL}
CJ74HCT164	3.0V	6.0ns	15pF, 50pF	t_{PLH}, t_{PHL}

9 Mechanical Information

9.1 SOP14 Mechanical Information

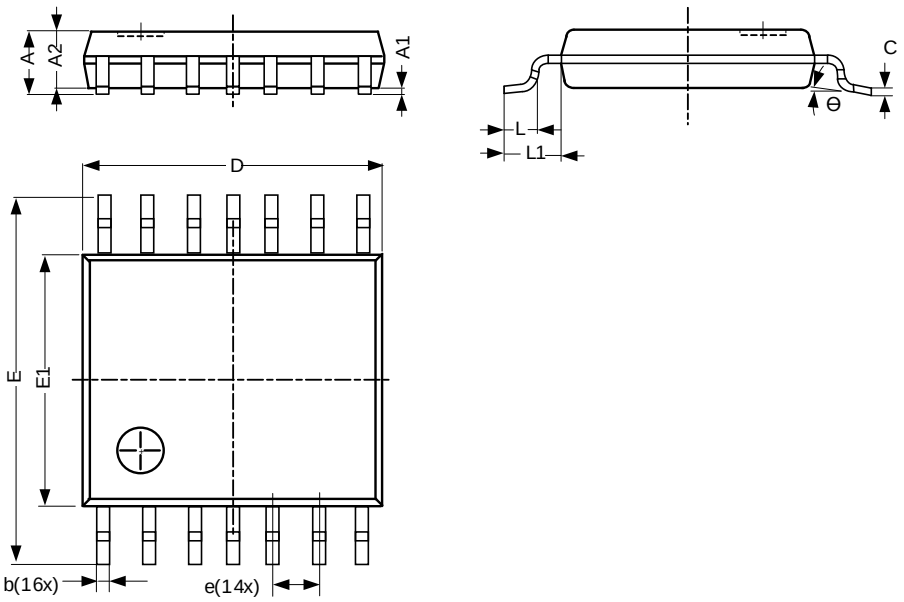
9.1.1 SOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.50	-	1.75
A1	0.05	-	0.25
A2	1.30	-	-
b	0.33	-	0.50
c	0.19	-	0.25
D	8.43	-	8.76
E	5.80	-	6.25
E1	3.75	-	4.00
e	1.27 BSC		
L	0.40	-	0.89
Θ	0°	-	8°
Unit: mm			

9.2 TSSOP14 Mechanical Information

9.2.1 TSSOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

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