

Dual 2-input OR Gate

CJ74LVC2G32 Logic

1 Introduction

The CJ74LVC2G32 provides a 2-input OR gate function.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V and 5V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

2 Available Packages

PART NUMBER	PACKAGE
CJ74LVC2G32	TSSOP8
	VSSOP8
	DFN1.35x1-8L

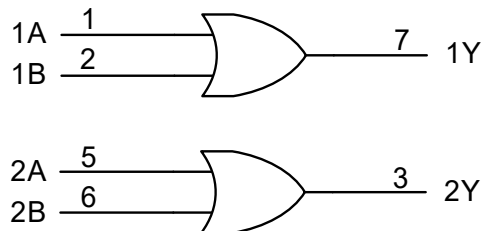
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range from 1.65V to 5.5V
- 5V tolerant outputs in the Power-down mode
- $\pm 24\text{mA}$ output drive ($V_{CC}=3.0\text{V}$)
- CMOS low power consumption
- Latch-up performance exceeds 250mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5V
- Specified from -40°C to $+125^{\circ}\text{C}$

4 Applications

- Down Translation
- Logical OR



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74LVC2G32BAN	TSSOP8	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units / Reel	Active
CJ74LVC2G32VAN	VSSOP8	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units / Reel	Active
CJ74LVC2G32DMN	DFN1.35x1-8L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

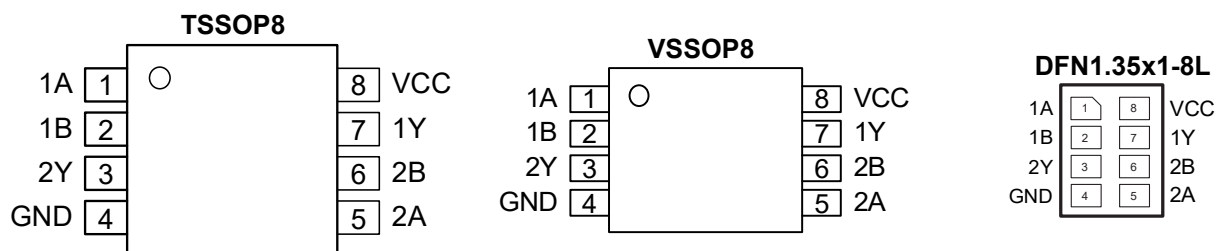


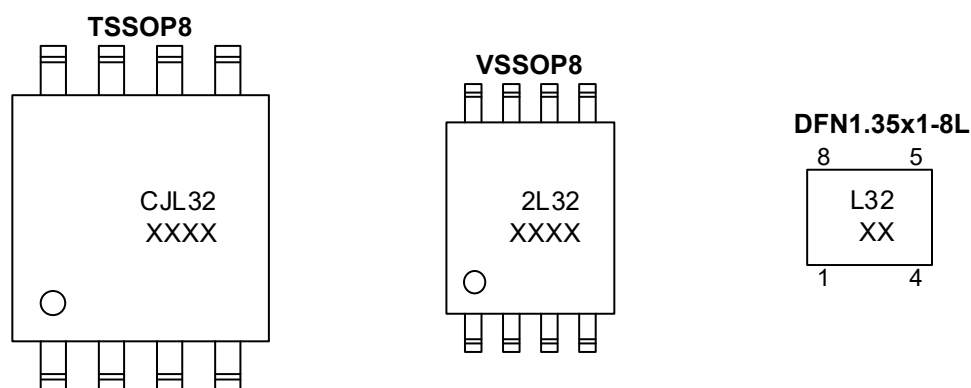
Figure 6-1 Pin configuration

6.2 Pin Function

PIN		I/O ⁽¹⁾	DESCRIPTION
No.	NAME		
1	1A	I	Data input
2	1B	I	Data input
3	2Y	O	Data output
4	GND	G	Ground (0V)
5	2A	I	Data input
6	2B	I	Data input
7	1Y	O	Data output
8	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



XXXX or XX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	Supply voltage	-	-0.5	+6.5	V
V _I	Input voltage	-	-0.5	+6.5	V
V _O	Output voltage	Active mode	-0.5	V _{CC} +0.5	V
		Power-down mode	-0.5	+6.5	V
I _{IK}	Input clamping current	V _I < 0V	-50	-	mA
I _{OK}	Output clamping current	V _O > V _{CC} or V _O < 0V	-	±50	mA
I _O	Output current	V _O =0V to V _{CC}	-	±50	mA
I _{CC}	Supply current	-	-	100	mA
I _{GND}	Ground current	-	-100	-	mA
T _{stg}	Storage temperature	-	-65	+150	°C
P _{tot}	Total power dissipation	-	-	300	mW
T _L	Soldering temperature	10s	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

(1) When V_{CC}=0V (Power-down mode), the output voltage can be 5.5V in normal operation.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{CC}	Supply voltage	-	1.65	-	5.5	V
V _I	Input voltage	-	0	-	5.5	V
V _O	Output voltage	Active mode	0	-	V _{CC}	V
		Power-down mode	0	-	5.5	V
T _{amb}	Ambient temperature	-	-40	-	+125	°C
Δt/ΔV	Input transition rise and fall rate	V _{CC} =1.65V to 2.7V	-	-	20	ns/V
		V _{CC} =2.7V to 5.5V	-	-	10	ns/V

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
V _{ESD-HBM}	Electrostatic discharge	Human body model (HBM) ⁽¹⁾	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	$V_{CC}=1.65\text{V to }1.95\text{V}$		$0.65 \times V_{CC}$	-	-	V
		$V_{CC}=2.3\text{V to }2.7\text{V}$		1.7	-	-	V
		$V_{CC}=2.7\text{V to }3.6\text{V}$		2.0	-	-	V
		$V_{CC}=4.5\text{V to }5.5\text{V}$		$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC}=1.65\text{V to }1.95\text{V}$		-	-	$0.35 \times V_{CC}$	V
		$V_{CC}=2.3\text{V to }2.7\text{V}$		-	-	0.7	V
		$V_{CC}=2.7\text{V to }3.6\text{V}$		-	-	0.8	V
		$V_{CC}=4.5\text{V to }5.5\text{V}$		-	-	$0.3 \times V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O = -100\mu\text{A}; V_{CC}=1.65\text{V to }5.5\text{V}$	$V_{CC}-0.1$	-	-	V
			$I_O = -4\text{mA}; V_{CC}=1.65\text{V}$	1.2	1.53	-	V
			$I_O = -8\text{mA}; V_{CC}=2.3\text{V}$	1.9	2.13	-	V
			$I_O = -12\text{mA}; V_{CC}=2.7\text{V}$	2.2	2.50	-	V
			$I_O = -24\text{mA}; V_{CC}=3.0\text{V}$	2.3	2.60	-	V
			$I_O = -32\text{mA}; V_{CC}=4.5\text{V}$	3.8	4.10	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O = 100\mu\text{A}; V_{CC}=1.65\text{V to }5.5\text{V}$	-	-	0.10	V
			$I_O = 4\text{mA}; V_{CC}=1.65\text{V}$	-	0.08	0.45	V
			$I_O = 8\text{mA}; V_{CC}=2.3\text{V}$	-	0.14	0.30	V
			$I_O = 12\text{mA}; V_{CC}=2.7\text{V}$	-	0.19	0.40	V
			$I_O = 24\text{mA}; V_{CC}=3.0\text{V}$	-	0.37	0.55	V
			$I_O = 32\text{mA}; V_{CC}=4.5\text{V}$	-	0.43	0.55	V
I_I	Input leakage current	$V_I=5.5\text{V or GND}; V_{CC}=0\text{V to }5.5\text{V}$		-	-	± 1	μA
I_{OFF}	Power-off leakage current	$V_I \text{ or } V_O=5.5\text{V}; V_{CC}=0\text{V}$		-	-	± 2	μA
I_{CC}	Supply current	$V_I=5.5\text{V or GND}; I_O=0\text{A}; V_{CC}=1.65\text{V to }5.5\text{V}$		-	-	4	μA
ΔI_{CC}	Additional supply current	Per pin; $V_I=V_{CC}-0.6\text{V}; I_O=0\text{A}; V_{CC}=2.3\text{V to }5.5\text{V}$		-	-	500	μA
C_I	Input capacitance	-		-	2.5	-	pF

(1) All typical values are measured at $T_{amb}=25^{\circ}\text{C}$.

7.4.2 DC Characteristics 2

$T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	$V_{CC}=1.65\text{V to }1.95\text{V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC}=2.3\text{V to }2.7\text{V}$	1.7	-	-	V
		$V_{CC}=2.7\text{V to }3.6\text{V}$	2.0	-	-	V
		$V_{CC}=4.5\text{V to }5.5\text{V}$	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC}=1.65\text{V to }1.95\text{V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC}=2.3\text{V to }2.7\text{V}$	-	-	0.7	V
		$V_{CC}=2.7\text{V to }3.6\text{V}$	-	-	0.8	V
		$V_{CC}=4.5\text{V to }5.5\text{V}$	-	-	$0.3 \times V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O = -100\mu\text{A}; V_{CC}=1.65\text{V to }5.5\text{V}$	$V_{CC}-0.1$	-	V
			$I_O = -4\text{mA}; V_{CC}=1.65\text{V}$	0.95	-	V
			$I_O = -8\text{mA}; V_{CC}=2.3\text{V}$	1.7	-	V
			$I_O = -12\text{mA}; V_{CC}=2.7\text{V}$	1.9	-	V
			$I_O = -24\text{mA}; V_{CC}=3.0\text{V}$	2.0	-	V
			$I_O = -32\text{mA}; V_{CC}=4.5\text{V}$	3.4	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O = 100\mu\text{A}; V_{CC}=1.65\text{V to }5.5\text{V}$	-	-	0.10
			$I_O = 4\text{mA}; V_{CC}=1.65\text{V}$	-	-	0.70
			$I_O = 8\text{mA}; V_{CC}=2.3\text{V}$	-	-	0.45
			$I_O = 12\text{mA}; V_{CC}=2.7\text{V}$	-	-	0.60
			$I_O = 24\text{mA}; V_{CC}=3.0\text{V}$	-	-	0.80
			$I_O = 32\text{mA}; V_{CC}=4.5\text{V}$	-	-	0.80
I_I	Input leakage current	$V_I=5.5\text{V or GND}; V_{CC}=0\text{V to }5.5\text{V}$	-	-	± 1	μA
I_{OFF}	Power-off leakage current	$V_I \text{ or } V_O=5.5\text{V}; V_{CC}=0\text{V}$	-	-	± 2	μA
I_{CC}	Supply current	$V_I=5.5\text{V or GND}; I_O=0\text{A}; V_{CC}=1.65\text{V to }5.5\text{V}$	-	-	4	μA
ΔI_{CC}	Additional supply current	Per pin; $V_I=V_{CC}-0.6\text{V}; I_O=0\text{A}; V_{CC}=2.3\text{V to }5.5\text{V}$	-	-	500	μA

(1) All typical values are measured at $T_{amb}=25^{\circ}\text{C}$.

7.4.3 AC Characteristics 1

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t _{pd}	nA, nB to nY propagation delay	See Figure 8-5	V _{CC} =1.65V to 1.95V	1.3	3.9	8.8	ns
			V _{CC} =2.3V to 2.7V	0.8	2.4	4.7	ns
			V _{CC} =2.7V	0.8	2.7	4.8	ns
			V _{CC} =3.0V to 3.6V	0.9	2.2	4.2	ns
			V _{CC} =4.5V to 5.5V	0.7	1.7	3.2	ns
C _{PD}	Power dissipation capacitance	Per gate; V _I =GND to V _{CC}		-	14	-	pF

- (1) Typical values are measured at normal V_{CC} and $T_{amb}=25^{\circ}\text{C}$.
- (2) t_{pd} is the same as t_{PLH} and t_{PHL} .
- (3) C_{PD} is used to determine the dynamic power dissipation (P_D in uW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

7.4.4 AC Characteristics 2

$T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t _{pd}	nA, nB to nY propagation delay	See Figure 8-5	V _{CC} =1.65V to 1.95V	1.3	-	11.0	ns
			V _{CC} =2.3V to 2.7V	0.8	-	5.9	ns
			V _{CC} =2.7V	0.8	-	6.0	ns
			V _{CC} =3.0V to 3.6V	0.9	-	5.3	ns
			V _{CC} =4.5V to 5.5V	0.7	-	4.0	ns

- (1) Typical values are measured at normal V_{CC} and $T_{amb}=25^{\circ}\text{C}$.
- (2) t_{pd} is the same as t_{PLH} and t_{PHL} .

8 Detailed Description

8.1 Overview

The CJ74LVC2G32 provides a 2-input OR gate function.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V and 5V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

8.2 Functional Block Diagram

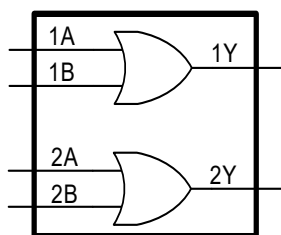


Figure 8-1 Logic symbol

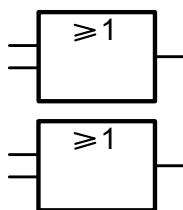


Figure 8-2 IEC logic symbol

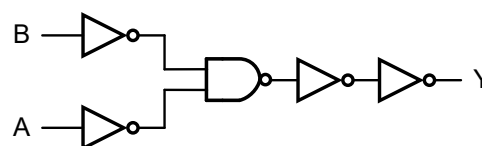


Figure 8-3 Logic diagram

8.3 Function Table⁽¹⁾

INPUT		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

(1) H=HIGH voltage level; L=LOW voltage level.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

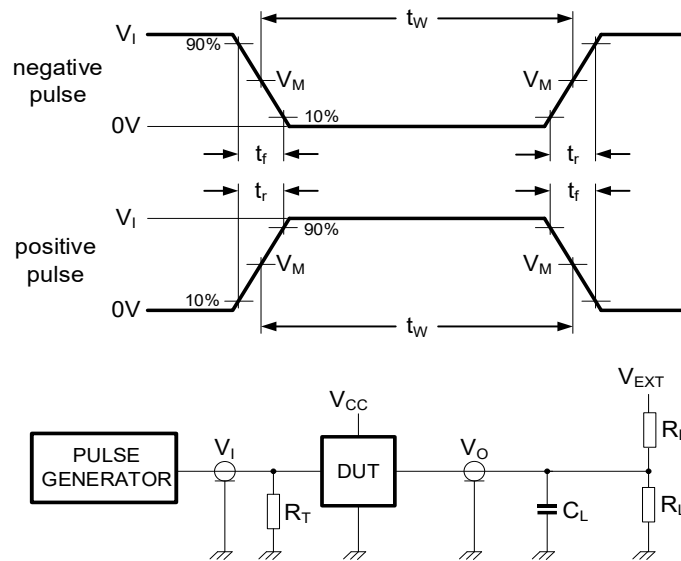


Figure 8-4 Test circuit for measuring switching times

Definitions for test circuit:

R_L =Load resistance.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} =External voltage for measuring switching times.

8.4.2 AC Testing Waveforms

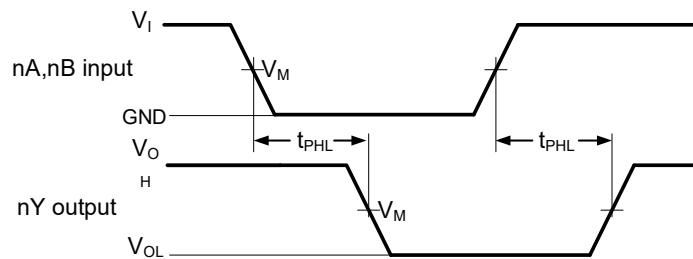


Figure 8-5 The input (nA, nB) to output (nY) propagation delays

8.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{CC}	V_M	V_M
1.65V to 1.95V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3V to 2.7V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7V	1.5V	1.5V
3.0V to 3.6V	1.5V	1.5V
4.5V to 5.5V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

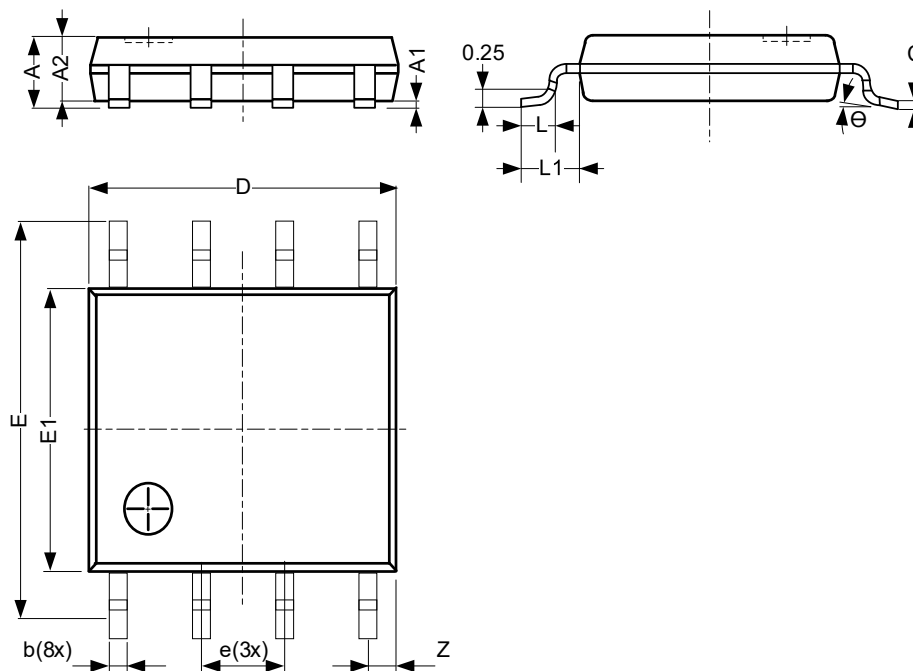
8.4.4 Test Data

SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}
V_{CC}	V_I	$t_r=t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65V to 1.95V	V_{CC}	$\leq 2.0\text{ns}$	30pF	1k Ω	Open
2.3V to 2.7V	V_{CC}	$\leq 2.0\text{ns}$	30pF	500 Ω	Open
2.7V	2.7V	$\leq 2.5\text{ns}$	50pF	500 Ω	Open
3.0V to 3.6V	2.7V	$\leq 2.5\text{ns}$	50pF	500 Ω	Open
4.5V to 5.5V	V_{CC}	$\leq 2.5\text{ns}$	50pF	500 Ω	Open

9 Mechanical Information

9.1 TSSOP8 Mechanical Information

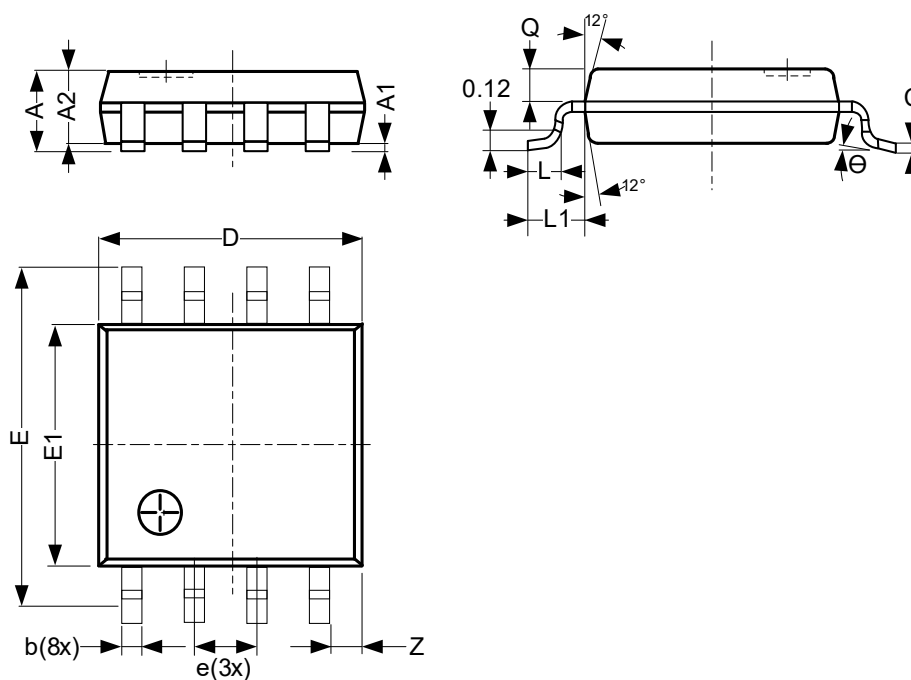
9.1.1 TSSOP8 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.10
A1	0	-	0.15
A2	0.75	-	0.95
b	0.22	-	0.38
c	0.08	-	0.18
D	2.90	-	3.10
E	3.90	-	4.10
E1	2.90	-	3.10
e	0.65 BSC		
L	0.33	-	0.47
L1	-	0.50	-
Z	0.35	-	0.70-
θ	0°	-	8°
Unit: mm			

9.2 VSSOP8 Mechanical Information

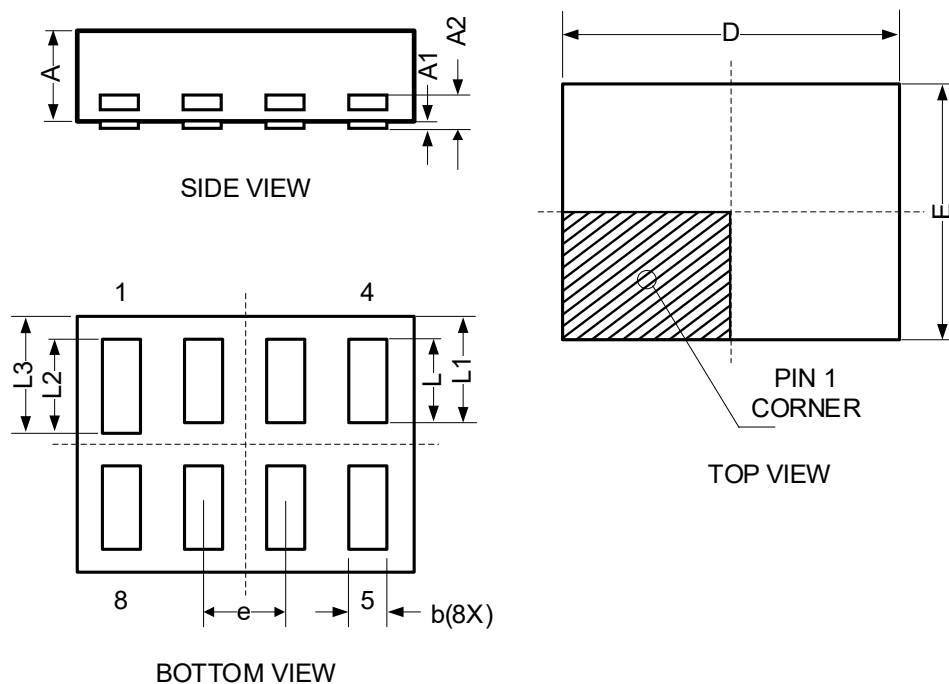
9.2.1 VSSOP8 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.00
A1	0	-	0.15
A2	0.60	-	0.85
Q	0.19		0.21
b	0.17	-	0.27
c	0.08	-	0.23
D	1.90	-	2.10
E	3.00	-	3.20
E1	2.20	-	2.40
e	0.50 BSC		
L	0.15	-	0.40
L1	-	0.40	-
Z	0.10	-	0.40-
θ	0°	-	8°
Unit: mm			

9.3 DFN1.35x1-8L Mechanical Information

9.3.1 DFN1.35x1-8L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.28	-	0.32
A1	0.00	-	0.05
A2	-	0.10	-
D	-	1.35	-
E	-	1.00	-
e	0.35 BSC		
b	0.11	-	0.21
L	0.25	-	0.35
L1	0.275	-	0.475
L2	0.30	-	0.40
L3	0.325	-	0.525
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- <https://www.jscj-elec.com> for more details.

10.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

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