Octal D-type flip-flop; positive edge-trigger; 3-state

CJ74HC/HCT374 Logic

1 Introduction

The CJ74HC/HCT374 is an octal positive-edge triggered D-type flip-flop with 3-state outputs. The device features a clock (CP) and output enable (/OE) inputs. The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A HIGH on /OE causes the outputs to assume a high-impedance OFF-state. Operation of the /OE input does not affect the state of the flip-flops. Inputs also include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

The CJ74HCT374 features reduced input threshold levels to allow interfacing to TTL logic levels.

2 Available Packages

PART NUMBER	PACKAGE
CJ74HC374	SOP20
	TSSOP20
CJ74HCT374	SOP20
	TSSOP20

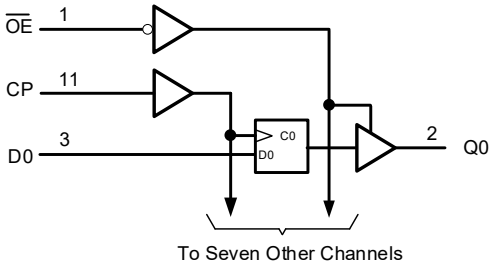
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Input levels:
  - For CJ74HC374: CMOS level
  - For CJ74HCT374: TTL level
- Octal bus interface
- Non-inverting 3-state outputs
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Specified from -40°C to +125°C

4 Applications

- Printers
- Network Switches
- Tests and Measurements
- Wireless Infrastructure
- Motor Controls
- Server Motherboards



Function diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74HC374AGN	SOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 2000 Units / Reel	Active
CJ74HCT374AGN	SOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 2000 Units / Reel	Active
CJ74HC374BGN	TSSOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HCT374BGN	TSSOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

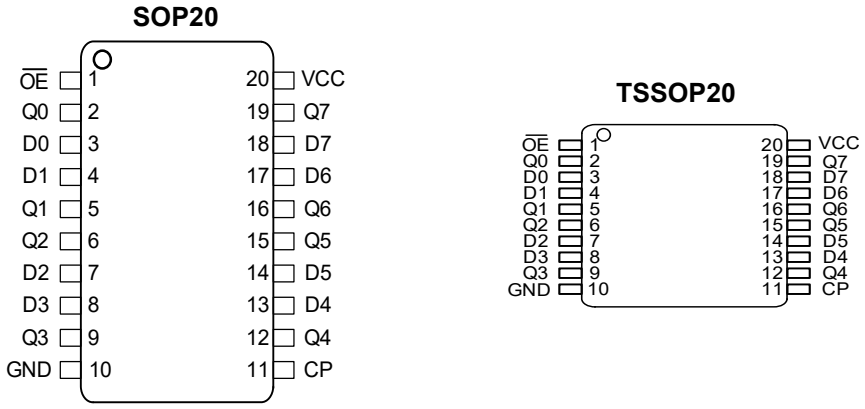


Figure 6-1 Pin configuration

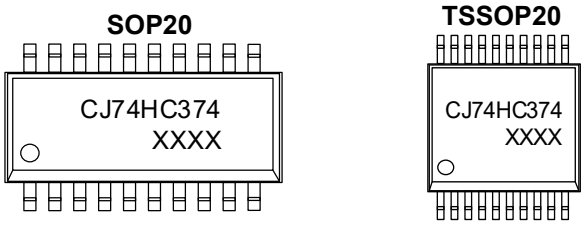
6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	$\overline{OE}$	I	Output enable input (active LOW)
2	Q0	O	Data output
3	D0	I	Data input
4	D1	I	Data input
5	Q1	O	Data output
6	Q2	O	Data output
7	D2	I	Data input
8	D3	I	Data input
9	Q3	O	Data output
10	GND	G	Ground (0V)
11	CP	I	Clock input (LOW-to-HIGH, edge-triggered)
12	Q4	O	Data output
13	D4	I	Data input
14	D5	I	Data input
15	Q5	O	Data output
16	Q6	O	Data output
17	D6	I	Data input
18	D7	I	Data input
19	Q7	O	Data output
20	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information

6.3.1 CJ74HC374



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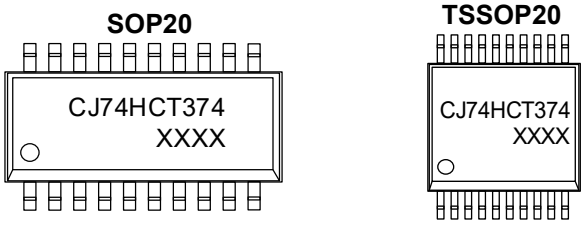
6.3.2 CJ74HCT374



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7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-		-0.5	+7.0	V
I_{IK}	Input clamping current	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
I_{OK}	Output clamping current	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
I_O	Output current	-0.5V < V_O < V_{CC}+0.5V		-	±35	mA
I_{CC}	Supply current	-		-	70	mA
I_{GND}	Ground current	-		-70	-	mA
T_{stg}	Storage temperature	-		-65	+150	°C
P_{tot}	Total power dissipation	-		-	500	mW
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC374						
V_{CC}	Supply voltage	-	2.0	5.0	6.0	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
Δt/ΔV	Input transition rise and fall rate	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
T_{amb}	Ambient temperature	-	-40	-	+125	°C
CJ74HCT374						
V_{CC}	Supply voltage	-	4.5	5.0	5.5	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
Δt/ΔV	Input transition rise and fall rate	V_{CC}=4.5V	-	1.67	139	ns/V
T_{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM)(1)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC374							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-7.8mA; V_{CC}=6.0V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=7.8mA; V_{CC}=6.0V	-	0.16	0.26	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V; V_O=V_{CC} or GND		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
C_I	Input capacitance	-		-	3.5	-	pF
CJ74HCT374							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	0.16	0.26	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	V_I=V_{IH} or V_{IL}; V_{CC}=5.5V; V_O=V_{CC} or GND		-	-	±1.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	8.0	uA
ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	$\overline{OE}$ input	-	-	450	uA
			CP input	-	-	324	uA
			Dn input	-	-	126	uA

C_I	Input capacitance	-	-	3.5	-	pF

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC374							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-7.8mA; V_{CC}=6.0V	5.34	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=7.8mA; V_{CC}=6.0V	-	-	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V; V_O=V_{CC} or GND		-	-	±5.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
CJ74HCT374							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.84	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	-	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	V_I=V_{IH} or V_{IL}; V_{CC}=5.5V; V_O=V_{CC} or GND		-	-	±5.0	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-2.1V; Other inputs at	$\overline{OE}$ input	-	-	563	uA
			CP input	-	-	405	uA

		V_{CC} or GND; I_O=0A; V_{CC}=4.5V to 5.5V	Dn input	-	-	158	uA

7.4.3 DC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC374							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-7.8mA; V_{CC}=6.0V	5.2	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=7.8mA; V_{CC}=6.0V	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V; V_O=V_{CC} or GND		-	-	±10	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
CJ74HCT374							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.7	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
I_{OZ}	OFF-state output current	V_I=V_{IH} or V_{IL}; V_{CC}=5.5V; V_O=V_{CC} or GND		-	-	±10	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	160	uA
ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-	$\overline{OE}$ input	-	-	613	uA

		2.1V; Other inputs at V_{CC} or GND; I_O=0A; VCC=4.5V to 5.5V;	CP input	-	-	441	uA
			Dn input	-	-	172	uA

7.4.4 AC Characteristics 1

T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC374							
t_{pd}	CP to Qn propagation delay	See Figure 8-6	V_{CC}=2.0V	-	50	165	ns
			V_{CC}=4.5V	-	18	33	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
			V_{CC}=6.0V	-	14	18	ns
t_{en}	$\overline{OE}$ to Qn enable time	See Figure 8-7	V_{CC}=2.0V	-	41	150	ns
			V_{CC}=4.5V	-	15	30	ns
			V_{CC}=6.0V	-	12	26	ns
t_{dis}	$\overline{OE}$ to Qn disable time	See Figure 8-7	V_{CC}=2.0V	-	50	150	ns
			V_{CC}=4.5V	-	18	30	ns
			V_{CC}=6.0V	-	14	26	ns
t_t	Transition time	Qn output; See Figure 8-6	V_{CC}=2.0V	-	14	60	ns
			V_{CC}=4.5V	-	5	12	ns
			V_{CC}=6.0V	-	4	10	ns
t_W	Pulse width	CP; HIGH or LOW; See Figure 8-6	V_{CC}=2.0V	80	-	-	ns
			V_{CC}=4.5V	16	-	-	ns
			V_{CC}=6.0V	14	-	-	ns
t_{su}	Dn to CP set-up time	See Figure 8-6	V_{CC}=2.0V	60	-	-	ns
			V_{CC}=4.5V	12	-	-	ns
			V_{CC}=6.0V	10	-	-	ns
t_h	Dn to CP hold time	See Figure 8-6	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	V_{CC}=2.0V	6.0	23	-	MHz
			V_{CC}=4.5V	30	70	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	77	-	MHz
			V_{CC}=6.0V	35	83	-	MHz
C_{PD}	Power dissipation capacitance	Per flip-flop; V_I=GND to V_{CC}		-	17	-	pF
CJ74HCT374							
t_{pd}	CP to Qn propagation delay	See Figure 8-6	V_{CC}=4.5V	-	16	32	ns
			V_{CC}=5.0V; C_L=15pF	-	13	-	ns

t_{en}	$\overline{OE}$ to Qn enable time	See Figure 8-7	V_{CC}=4.5V	-	16	30	ns
t_{dis}	$\overline{OE}$ to Qn disable time	See Figure 8-7	V_{CC}=4.5V	-	18	28	ns
t_t	Transition time	Qn; See Figure 8-6	V_{CC}=4.5V	-	5	12	ns
t_W	Pulse width	CP; HIGH or LOW; See Figure 8-6	V_{CC}=4.5V	19	-	-	ns
t_{su}	Dn to CP set-up time	See Figure 8-6	V_{CC}=4.5V	12	-	-	ns
t_h	Dn to CP hold time	See Figure 8-6	V_{CC}=4.5V	5	-	-	ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	V_{CC}=4.5V	26	44	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	48	-	MHz
C_{PD}	Power dissipation capacitance	Per flip-flop; V_I=GND to V_{CC}-1.5V		-	17	-	pF

Note:

(1) t_{pd} is the same as t_{PLH} and t_{PHL}.

(2) t_{en} is the same as t_{PZL} and t_{PZH}.

(3) t_{dis} is the same as t_{PLZ} and t_{PHZ}.

(4) t_t is the same as t_{THL} and t_{TLH}.

(5) C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=(C_{PD}xV_{CC}^2xf_ixN)+\sum(C_LxV_{CC}^2xf_o)$ where:

f_i=input frequency in MHz; f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_LxV_{CC}^2xf_o)$=sum of outputs.

7.4.5 AC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC374							
t_{pd}	CP to Qn propagation delay	See Figure 8-6	V_{CC}=2.0V	-	-	205	ns
			V_{CC}=4.5V	-	-	41	ns
			V_{CC}=6.0V	-	-	35	ns
t_{en}	$\overline{OE}$ to Qn enable time	See Figure 8-7	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
t_{dis}	$\overline{OE}$ to Qn disable time	See Figure 8-7	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
t_t	Transition time	Qn output; See Figure 8-6	V_{CC}=2.0V	-	-	75	ns
			V_{CC}=4.5V	-	-	15	ns
			V_{CC}=6.0V	-	-	13	ns
t_W	Pulse width	CP; HIGH or LOW; See Figure 8-6	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns

t_{su}	Dn to CP set-up time	See Figure 8-6	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
t_h	Dn to CP hold time	See Figure 8-6	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	V_{CC}=2.0V	4.8	-	-	MHz
			V_{CC}=4.5V	24	-	-	MHz
			V_{CC}=6.0V	28	-	-	MHz
CJ74HCT374							
t_{pd}	CP to Qn propagation delay	See Figure 8-6	V_{CC}=4.5V	-	-	40	ns
t_{en}	$\overline{OE}$ to Qn enable time	See Figure 8-7	V_{CC}=4.5V	-	-	38	ns
t_{dis}	$\overline{OE}$ to Qn disable time	See Figure 8-7	V_{CC}=4.5V	-	-	35	ns
t_t	Transition time	Qn; See Figure 8-6	V_{CC}=4.5V	-	-	15	ns
t_W	Pulse width	CP; HIGH or LOW; See Figure 8-6	V_{CC}=4.5V	24	-	-	ns
t_{su}	Dn to CP set-up time	See Figure 8-6	V_{CC}=4.5V	15	-	-	ns
t_h	Dn to CP hold time	See Figure 8-6	V_{CC}=4.5V	5	-	-	ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	V_{CC}=4.5V	21	-	-	MHz

Note:

(1) t_{pd} is the same as t_{PLH} and t_{PHL}.

(2) t_{en} is the same as t_{PZL} and t_{PZH}.

(3) t_{dis} is the same as t_{PLZ} and t_{PHZ}.

(4) t_t is the same as t_{THL} and t_{TLH}.

7.4.6 AC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC374							
t_{pd}	CP to Qn propagation delay	See Figure 8-6	V_{CC}=2.0V	-	-	250	ns
			V_{CC}=4.5V	-	-	50	ns
			V_{CC}=6.0V	-	-	43	ns
t_{en}	$\overline{OE}$ to Qn enable time	See Figure 8-7	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns
			V_{CC}=6.0V	-	-	38	ns
t_{dis}	$\overline{OE}$ to Qn disable time	See Figure 8-7	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns
			V_{CC}=6.0V	-	-	38	ns
t_t	Transition time	Qn output; See Figure 8-6	V_{CC}=2.0V	-	-	90	ns
			V_{CC}=4.5V	-	-	18	ns

			V_{CC}=6.0V	-	-	15	ns
t_W	Pulse width	CP; HIGH or LOW; See Figure 8-6	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
t_{su}	Dn to CP set-up time	See Figure 8-6	V_{CC}=2.0V	90	-	-	ns
			V_{CC}=4.5V	18	-	-	ns
			V_{CC}=6.0V	15	-	-	ns
t_h	Dn to CP hold time	See Figure 8-6	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	V_{CC}=2.0V	4.0	-	-	MHz
			V_{CC}=4.5V	20	-	-	MHz
			V_{CC}=6.0V	24	-	-	MHz
CJ74HCT374							
t_{pd}	CP to Qn propagation delay	See Figure 8-6	V_{CC}=4.5V	-	-	48	ns
t_{en}	$\overline{OE}$ to Qn enable time	See Figure 8-7	V_{CC}=4.5V	-	-	45	ns
t_{dis}	$\overline{OE}$ to Qn disable time	See Figure 8-7	V_{CC}=4.5V	-	-	42	ns
t_t	Transition time	Qn; See Figure 8-6	V_{CC}=4.5V	-	-	18	ns
t_W	Pulse width	CP; HIGH or LOW; See Figure 8-6	V_{CC}=4.5V	29	-	-	ns
t_{su}	Dn to CP set-up time	See Figure 8-6	V_{CC}=4.5V	18	-	-	ns
t_h	Dn to CP hold time	See Figure 8-6	V_{CC}=4.5V	5	-	-	ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	V_{CC}=4.5V	17	-	-	MHz

Note:

(1) t_{pd} is the same as t_{PLH} and t_{PHL}.

(2) t_{en} is the same as t_{PZL} and t_{PZH}.

(3) t_{dis} is the same as t_{PLZ} and t_{PHZ}.

(4) t_t is the same as t_{THL} and t_{TLH}.

8 Detailed Description

8.1 Overview

The CJ74HC/HCT374 is an octal positive-edge triggered D-type flip-flop with 3-state outputs. The device features a clock (CP) and output enable (/OE) inputs. The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A HIGH on /OE causes the outputs to assume a high-impedance OFF-state. Operation of the /OE input does not affect the state of the flip-flops. Inputs also include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

The CJ74HCT374 features reduced input threshold levels to allow interfacing to TTL logic levels.

8.2 Functional Block Diagram

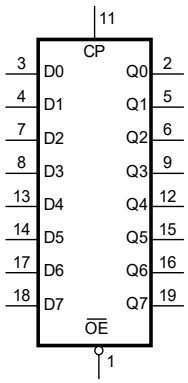


Figure 8-1 Logic symbol

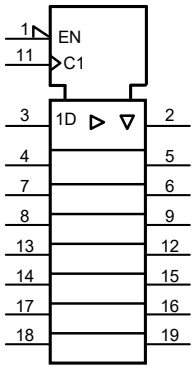


Figure 8-2 IEC logic symbol

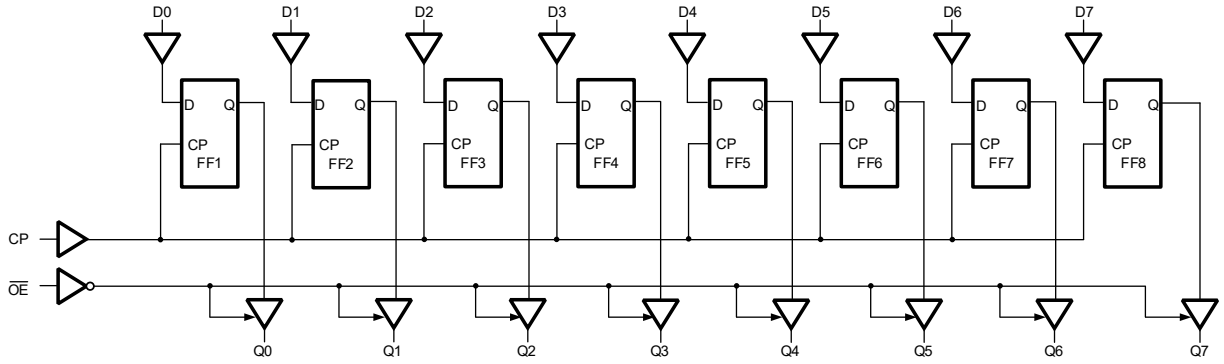


Figure 8-3 Logic diagram

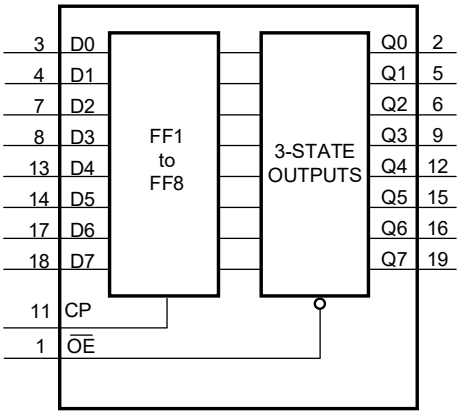


Figure 8-4 Functional diagram

8.3 Function Table(1)

OPERATING MODES	INPUT			INTERNAL FLIP-FLOPS	OUTPUT
	$\overline{OE}$	CP	Dn		Qn
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

(1) H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state;
h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
↑=LOW-to-HIGH clock transition.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

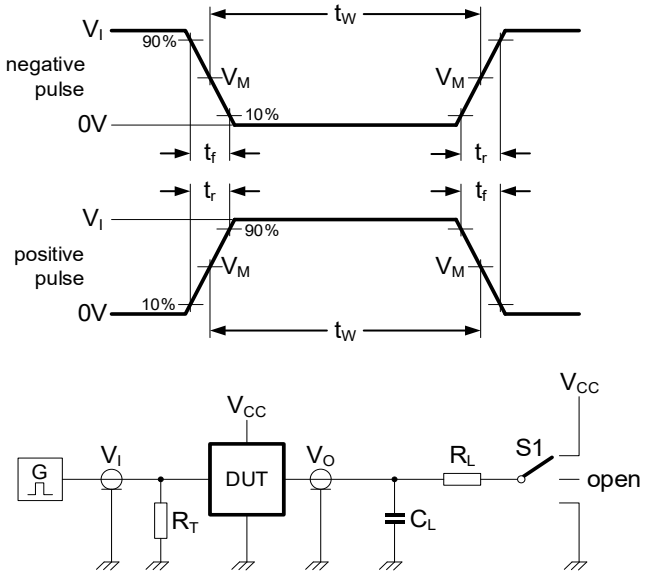


Figure 8-5 Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1=Test selection switch.

8.4.2 AC Testing Waveforms

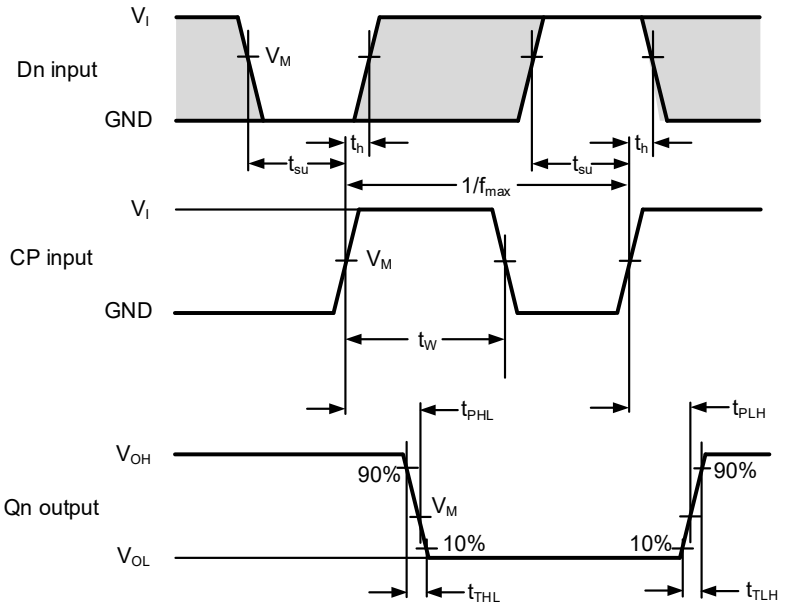


Figure 8-6 Clock input (CP) to output (Qn) propagation delay, clock pulse width, data (Dn) to clock (CP) set-up and hold times, output transition times (Qn) and maximum clock frequency

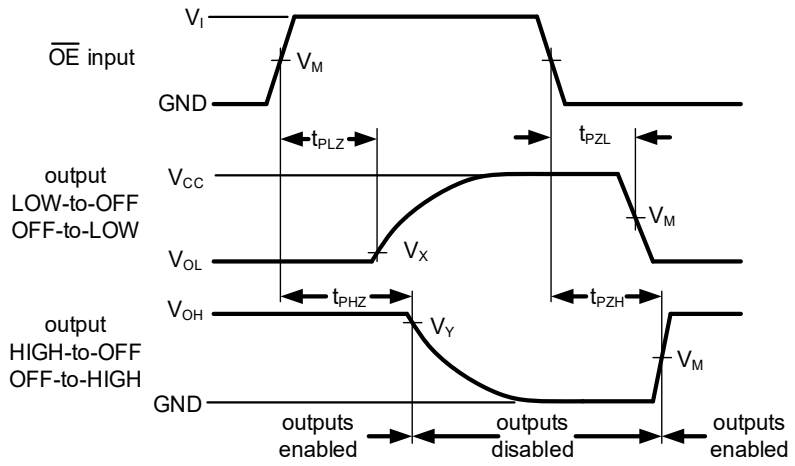


Figure 8-7 3-state enable and disable times

8.4.3 Measurement Points

TYPE	INPUT		OUTPUT		
	V_I	V_M	V_M	V_X	V_Y
CJ74HC374	GND to V_{CC}	0.5xV_{CC}	0.5xV_{CC}	0.1xV_{CC}	0.9xV_{CC}
CJ74HCT374	GND to 3V	1.3V	1.3V	0.1xV_{CC}	0.9xV_{CC}

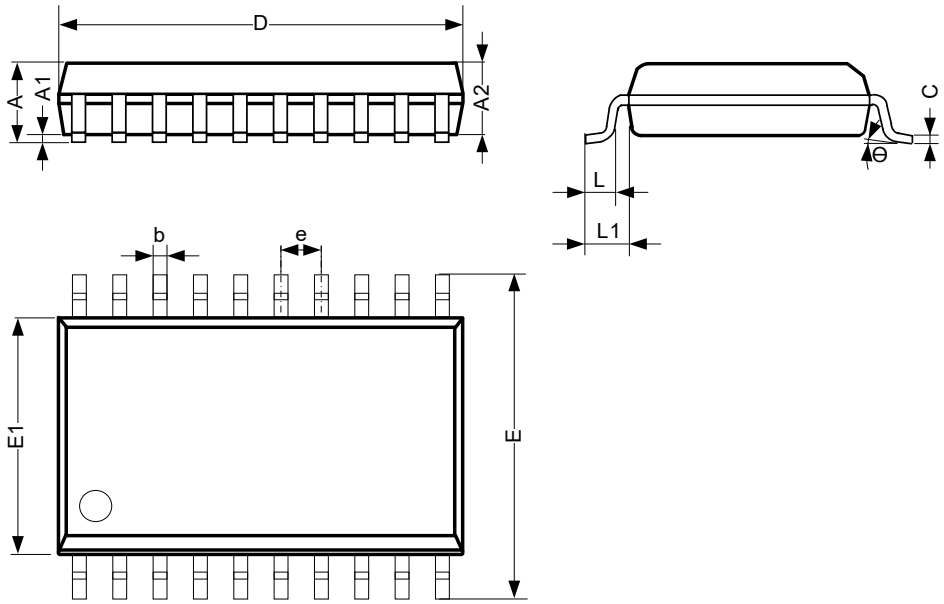
8.4.4 Test Data

TYPE	INPUT		LOAD		S1 POSITION		
	V_I	t_r , t_f	C_L	R_L	t_{PHL},t_{PLH}	t_{PZH},t_{PHZ}	t_{PZL},t_{PLZ}
CJ74HC374	GND to V_{CC}	6ns	15pF, 50pF	1kΩ	Open	GND	V_{CC}
CJ74HCT374	GND to 3V	6ns	15pF, 50pF	1kΩ	Open	GND	V_{CC}

9 Mechanical Information

9.1 SOP20 Mechanical Information

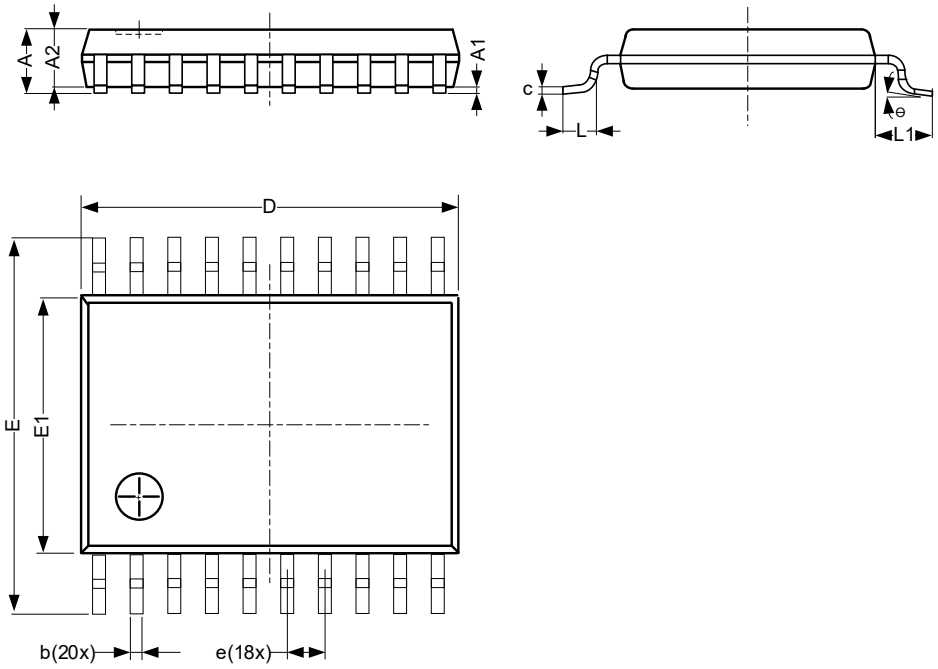
9.1.1 SOP20 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	2.47	-	2.65
A1	0.05	-	0.30
A2	2.20	-	2.44
b	0.35	-	0.50
c	0.15	-	0.30
D	12.54	-	12.94
E	10.00	-	10.60
E1	7.30	-	7.70
e	1.27 BSC		
L	0.40	-	1.05
L1	1.30	-	1.50
θ	0°	-	8°
Unit: mm			

9.2 TSSOP20 Mechanical Information

9.2.1 TSSOP20 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	6.40	-	6.60
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

July, 2025: rev - 1.1, Change marking information.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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