



PSMNR90-80ASF

NextPower 80 V, 0.85 mOhm, N-channel MOSFET in CCPAK1212 package

20 October 2025

Product data sheet

1. General description

NextPower 80 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for high power industrial and consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- 505 Amps $I_{D(max)}$ continuous current rating
- Low $Q_G \times R_{DSon}$ FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{as})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant CCPAK1212 package
- CCPAK1212 is JEDEC listed package for open market and 2nd source compatibility

3. Applications

- Battery protection
- High power full and half-bridge configurations
- BLDC motor control
- OR-ing

4. Quick reference data

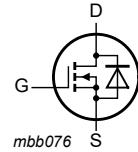
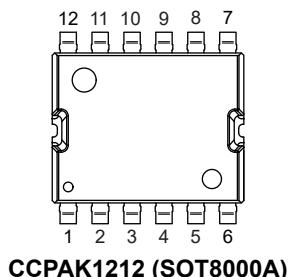
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25^{\circ}\text{C} \leq T_j \leq 175^{\circ}\text{C}$	-	-	80	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25^{\circ}\text{C}$; Fig. 2	-	-	505	A
P_{tot}	total power dissipation	$T_{mb} = 25^{\circ}\text{C}$; Fig. 1	-	-	1.55	kW
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25^{\circ}\text{C}$; Fig. 11	-	0.67	0.85	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}; V_{DS} = 40\text{ V}; V_{GS} = 10\text{ V}; T_j = 25^{\circ}\text{C}$; Fig. 13 ; Fig. 14	154	309	463	nC
Source-drain diode						
Q_r	recovered charge	$I_S = 25\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 40\text{ V}; T_j = 25^{\circ}\text{C}$; Fig. 17	-	94	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source		
3	S	source		
4	S	source		
5	S	source		
6	S	source		
7	D	drain		
8	D	drain		
9	D	drain		
10	D	drain		
11	D	drain		
12	D	drain		
mb	D	mounting base; connected to drain		



6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR90-80ASF	CCPAK1212	Plastic, surface mounted copper clip package (CCPAK1212); 13 terminals; 2.0 mm pitch, 12 mm x 12 mm x 2.5 mm body	SOT8000A

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR90-80ASF	XPF90S80A

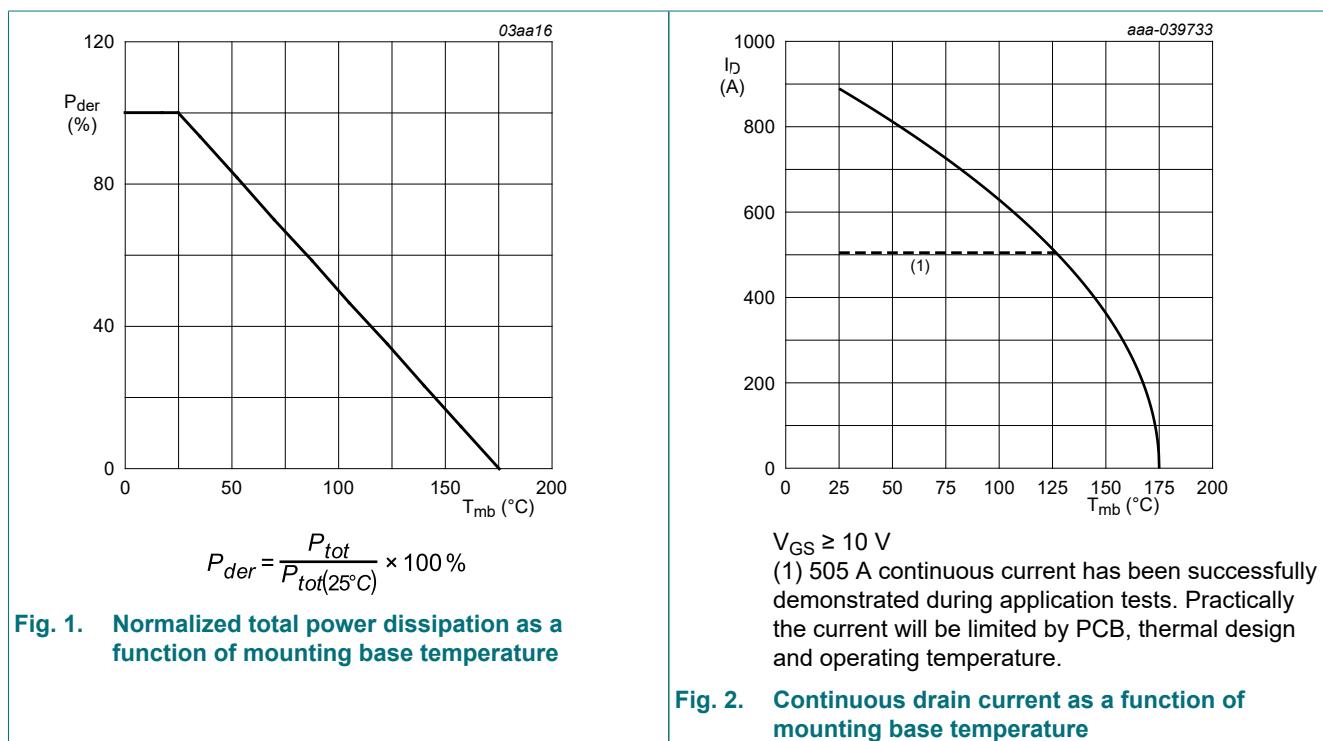
8. Limiting values

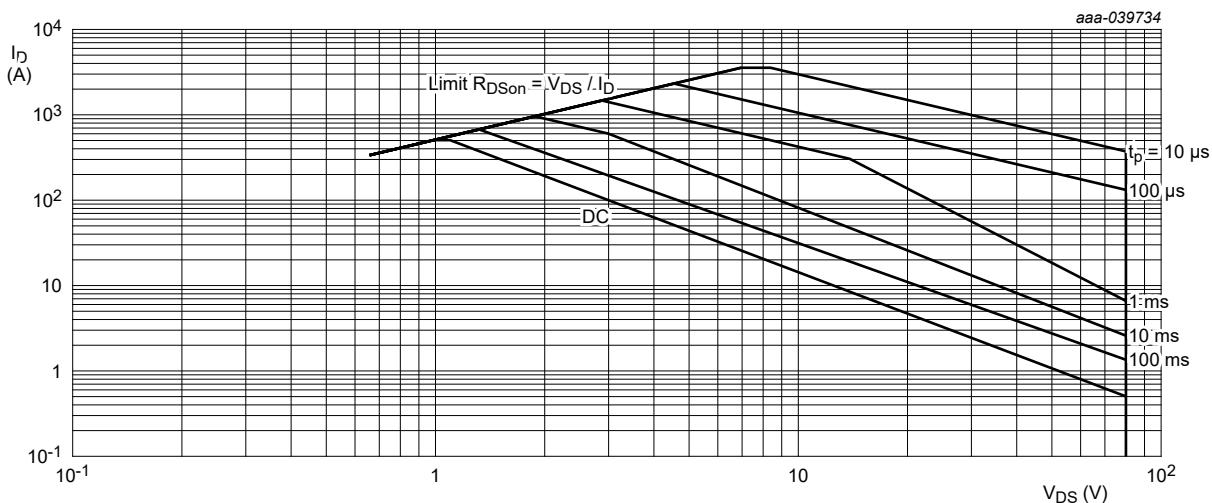
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25^\circ\text{C} \leq T_j \leq 175^\circ\text{C}$		-	80	V
V_{DGR}	drain-gate voltage	$25^\circ\text{C} \leq T_j \leq 175^\circ\text{C}; R_{GS} = 20\text{ k}\Omega$		-	80	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25^\circ\text{C}$; Fig. 1		-	1.55	kW
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25^\circ\text{C}$; Fig. 2		-	505	A
		$V_{GS} = 10\text{ V}; T_{mb} = 100^\circ\text{C}$; Fig. 2		-	505	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25^\circ\text{C}$; Fig. 3		-	3558	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25^\circ\text{C}$		-	505	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25^\circ\text{C}$		-	3558	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 129\text{ A}; V_{sup} \leq 80\text{ V}; R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}; T_{j(init)} = 25^\circ\text{C}$; unclamped; $t_p = 282\text{ }\mu\text{s}$; Fig. 4	[1]	-	1890	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 80\text{ V}; V_{GS} = 10\text{ V}; T_{j(init)} = 25^\circ\text{C}$; $R_{GS} = 50\text{ }\Omega$; Fig. 4	[1]	-	129	A

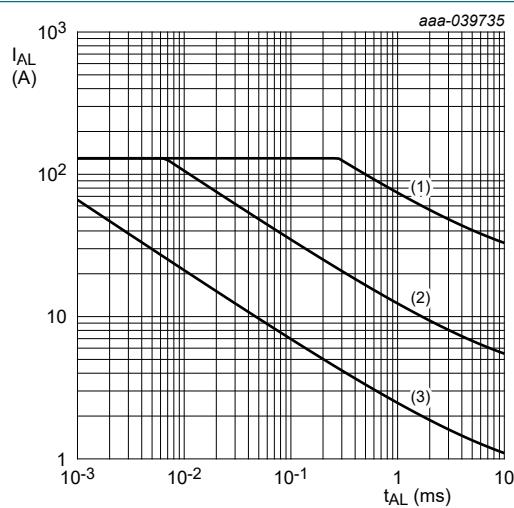
[1] Protected by 100% test





$T_{mb} = 25^\circ\text{C}$; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_j \text{ (init)} = 25^\circ\text{C}$; (2) $T_j \text{ (init)} = 150^\circ\text{C}$; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.075	0.1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6 Fig. 7	-	58	-	K/W

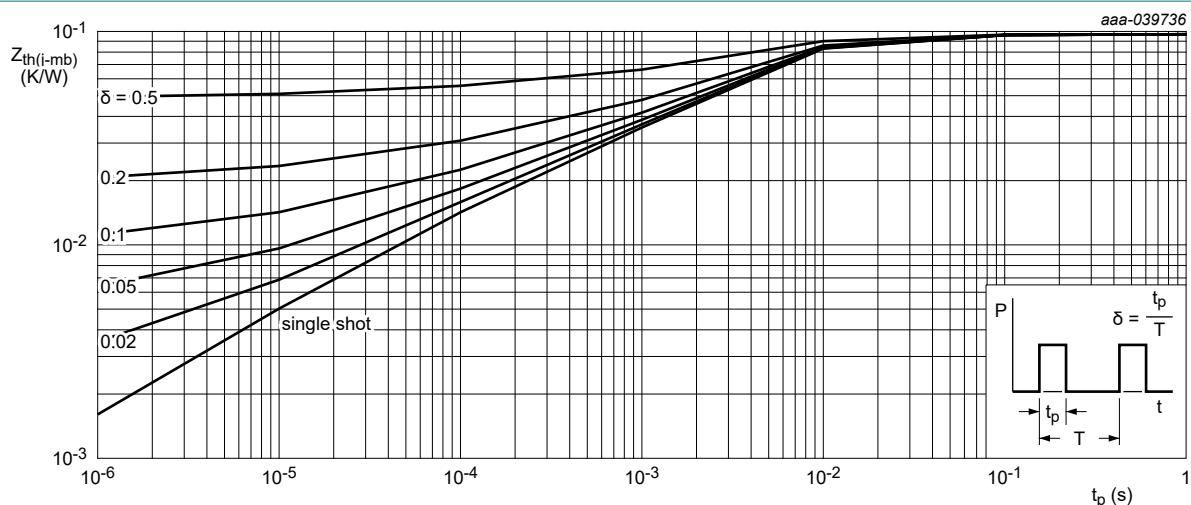
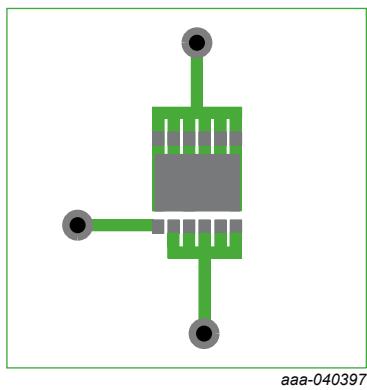
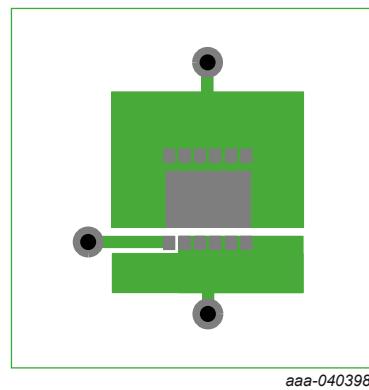


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration



70 μ m thick copper on FR4 board

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient



Copper area 25.4 mm square; 70 μ m thick on FR4 board

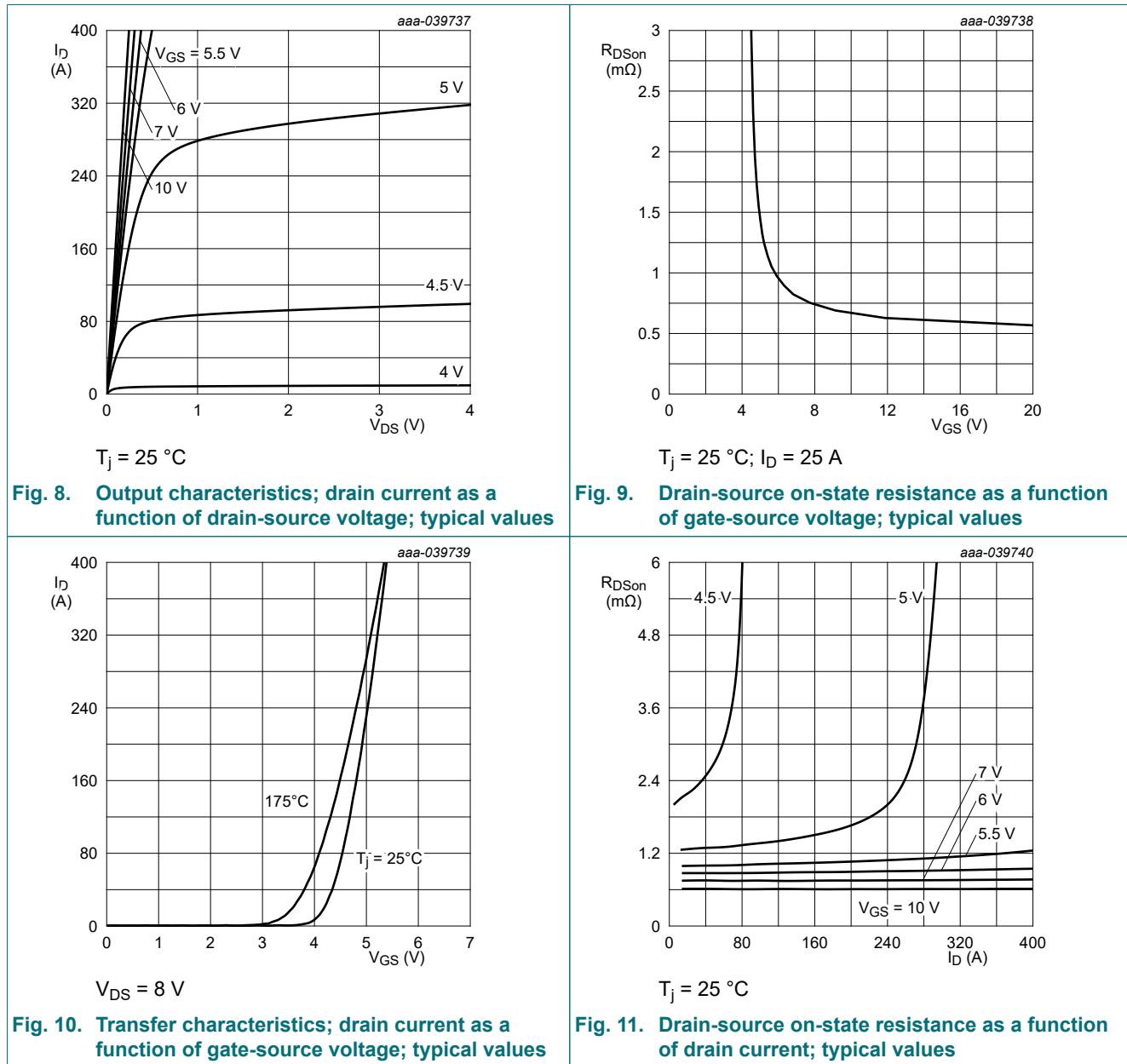
Fig. 7. PCB layout for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit	
Static characteristics								
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$ $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55^\circ C$		80	-	-	V	
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25^\circ C$		2	3	4	V	
		$I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175^\circ C$		-	1.56	-	V	
		$I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55^\circ C$		-	3.6	-	V	
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25^\circ C \leq T_j \leq 150^\circ C$		-	-9.28	-	mV/K	
I_{DSS}	drain leakage current	$V_{DS} = 80 V; V_{GS} = 0 V; T_j = 25^\circ C$		-	0.22	2	μA	
		$V_{DS} = 80 V; V_{GS} = 0 V; T_j = 125^\circ C$		-	49	200	μA	
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	2	100	nA	
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	2	100	nA	
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 25^\circ C$ Fig. 11		-	0.67	0.85	$m\Omega$	
		$V_{GS} = 10 V; I_D = 25 A; T_j = 100^\circ C$ Fig. 12		-	1	1.3	$m\Omega$	
		$V_{GS} = 10 V; I_D = 25 A; T_j = 175^\circ C$ Fig. 12		-	1.4	2	$m\Omega$	
		$V_{GS} = 7 V; I_D = 25 A; T_j = 25^\circ C$; Fig. 11		-	0.81	1.22	$m\Omega$	
R_G	gate resistance	$f = 1 MHz; T_j = 25^\circ C$		0.68	1.35	2.7	Ω	
Dynamic characteristics								
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; T_j = 25^\circ C$; Fig. 13 ; Fig. 14		154	309	463	nC	
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V; T_j = 25^\circ C$		-	284	-	nC	
Q_{GS}	gate-source charge	$I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; T_j = 25^\circ C$; Fig. 13 ; Fig. 14		58	97	136	nC	
$Q_{GS(th)}$	pre-threshold gate-source charge			-	66.1	-	nC	
				-	31.2	-	nC	
$Q_{GS(th-pl)}$	post-threshold gate-source charge			12	42	96	nC	
Q_{GD}	gate-drain charge			-	4.3	-	V	
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 A; V_{DS} = 40 V; T_j = 25^\circ C$; Fig. 13 ; Fig. 14		-	13764	22939	32115	pF
C_{iss}	input capacitance	$V_{DS} = 40 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25^\circ C$; Fig. 15		3685	6142	9827	pF	
C_{oss}	output capacitance			9	93	278	pF	
C_{rss}	reverse transfer capacitance			-	91	-	ns	
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 V; R_L = 1.6 \Omega; V_{GS} = 10 V; R_{G(ext)} = 5 \Omega; T_j = 25^\circ C$		-	91	-	ns	
t_r	rise time			-	69	-	ns	
$t_{d(off)}$	turn-off delay time			-	203	-	ns	
t_f	fall time			-	91	-	ns	
Source-drain diode								
V_{SD}	source-drain voltage	$I_S = 25 A; V_{GS} = 0 V; T_j = 25^\circ C$; Fig. 16		-	0.74	1	V	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}$; $dI_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 40 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 17	-	77	-	ns
Q_r	recovered charge		-	94	-	nC



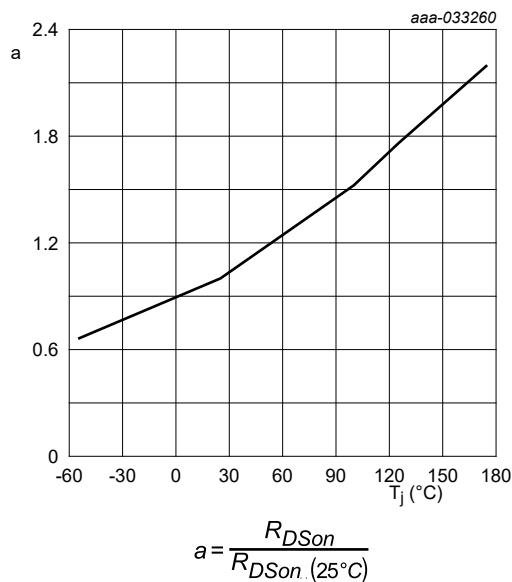


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

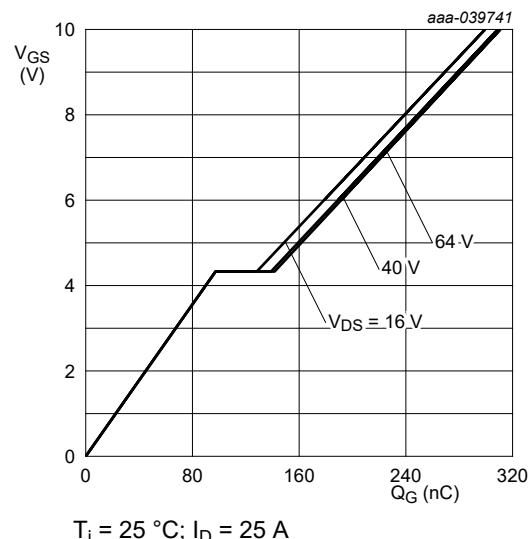


Fig. 13. Gate-source voltage as a function of gate charge; typical values

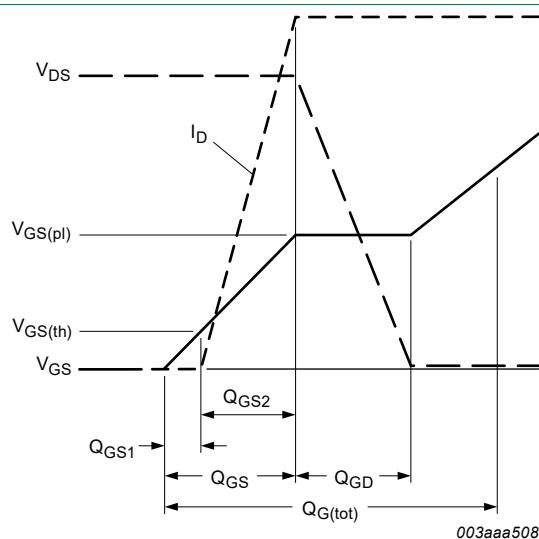


Fig. 14. Gate charge waveform definitions

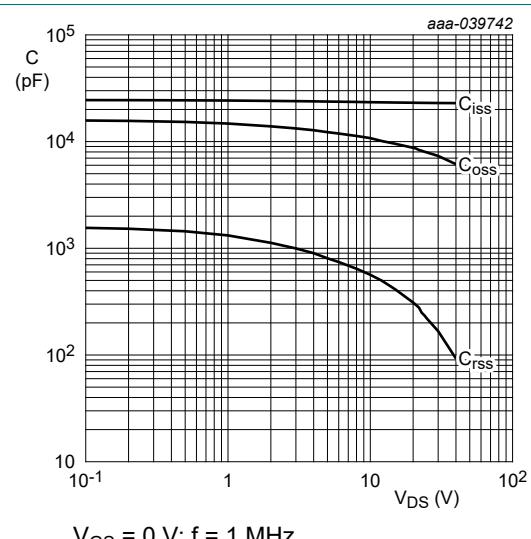


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

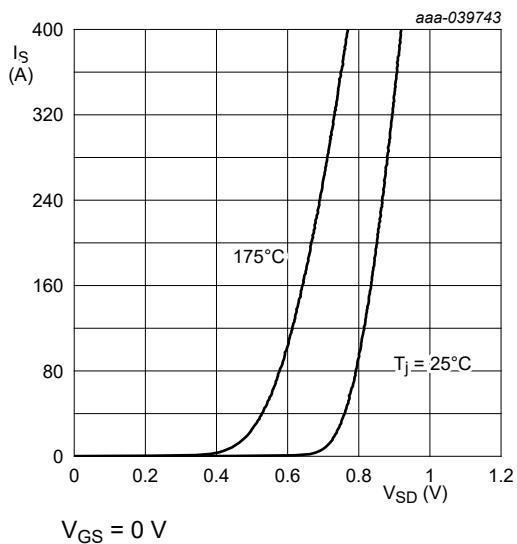


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

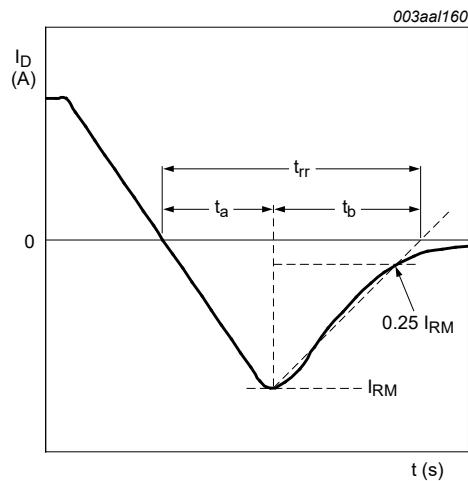


Fig. 17. Reverse recovery timing definition

11. Package outline

Plastic, surface mounted copper clip package (CCPAK1212);
13 terminals; 2.0 mm pitch, 12 mm x 12 mm x 2.5 mm body

SOT8000A

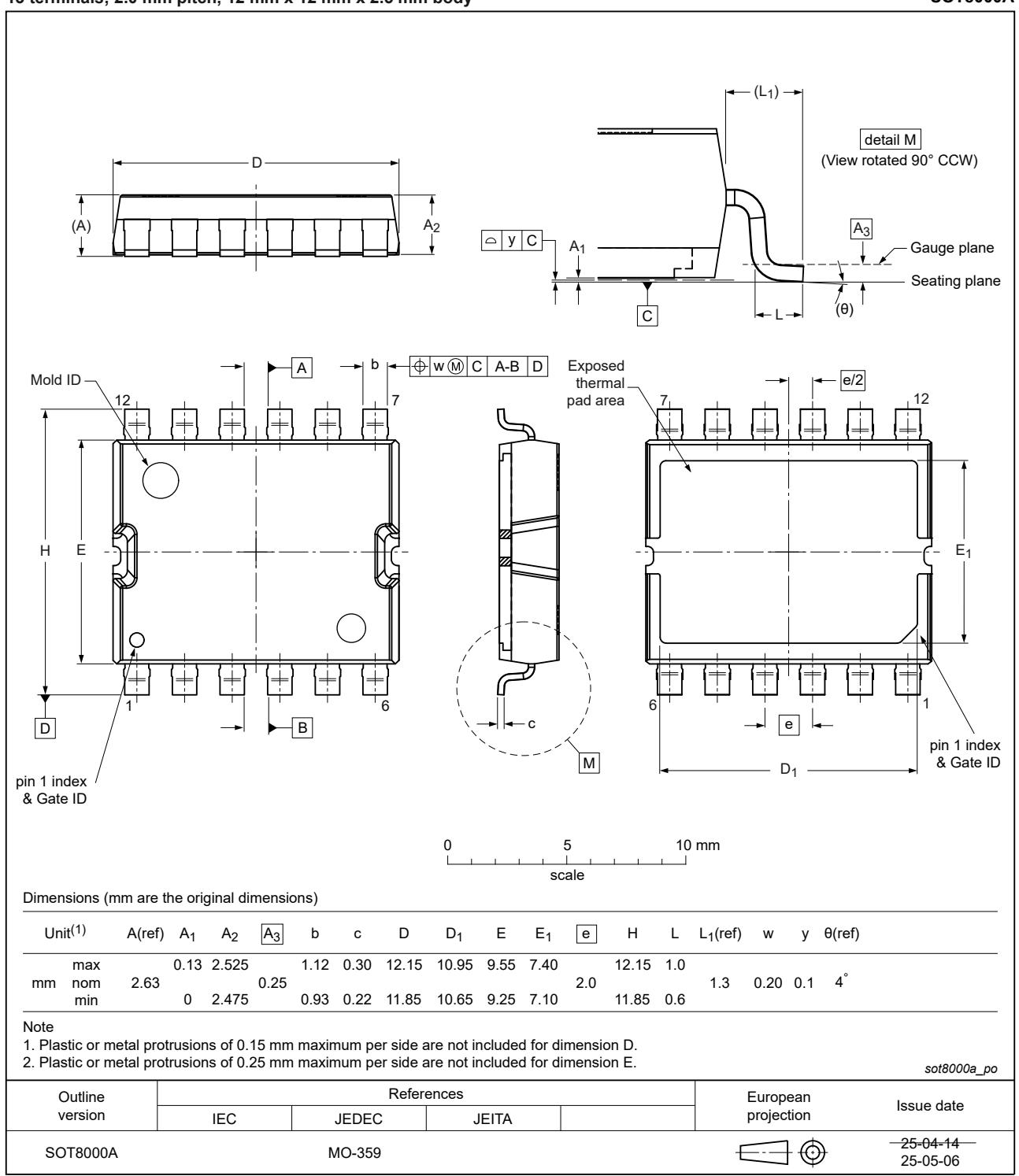
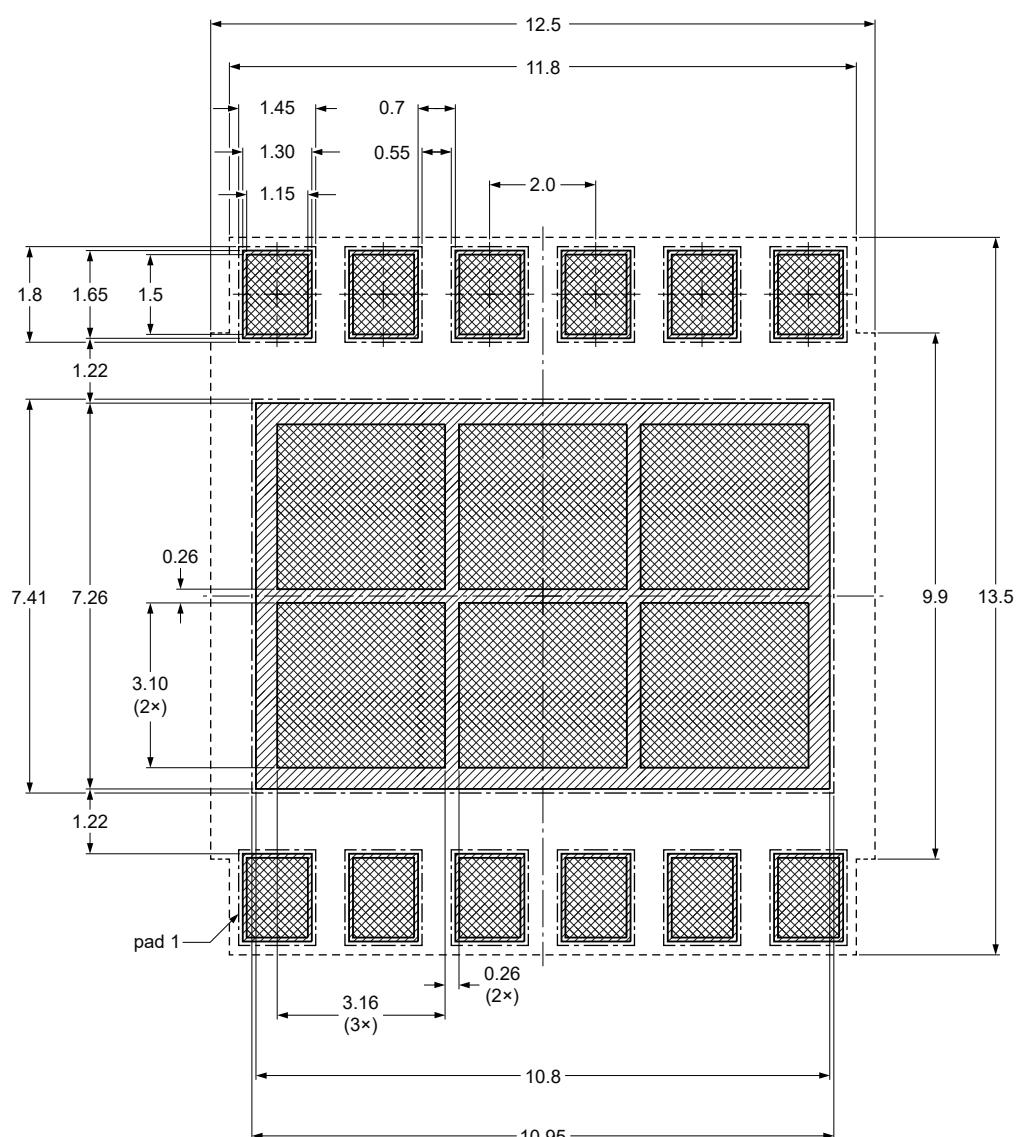


Fig. 18. Package outline CCPAK1212 (SOT8000A)

12. Soldering

Footprint information for reflow soldering of CCPAK1212 package

SOT8000A



[] occupied area
 [] solder resist

[] solder land
 [] solder paste

Dimensions in mm

Issue date 24-08-26

sot8000a_fr

Fig. 19. Reflow soldering footprint for CCPAK1212 (SOT8000A)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 20 October 2025
