Dual Precision Monostable Multivibrator

CD4538 **Logic**

1 Introduction

The CD4538 is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has an active LOW trigger/retrigger input (/nA), an active HIGH trigger/retrigger input (nB), an overriding active LOW direct reset input (/nCD), an output (nQ) and its complement (/nQ), and two pins (nREXT/CEXT, and nCEXT, always connected to ground) for connecting the external timing components C_{EXT} and R_{EXT}. Typical pulse width variation over the specified temperature range is ±0.2%.

The multivibrator may be triggered by either the positive or the negative edges of the input pulse and will produce an accurate output pulse with a pulse width range of 10us to infinity. The duration and accuracy of the output pulse are determined by the external timing components C_{EXT} and R_{EXT}. The output pulse width (t_W) is equal to $R_{EXT}xC_{EXT}$. The linear design techniques in LOCMOS (Local Oxide CMOS) guarantee precise control of the output pulse width. A LOW level at /nCD terminates the output pulse immediately.

It operates over a recommended V_{DD} power supply range of 3V to 12V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2 Available Packages

PART NUMBER	PACKAGE
CD4538	SOP16
	TSSOP16

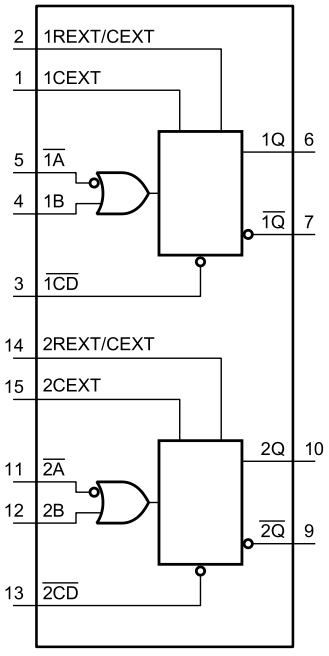
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range from 3V to 12V
- Tolerant of slow trigger rise and fall times
- Fully static operation
- 5V and 10V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C

4 Applications

- Pulse delay and timing
- Pulse shaping



Function block diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CD4538AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CD4538BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

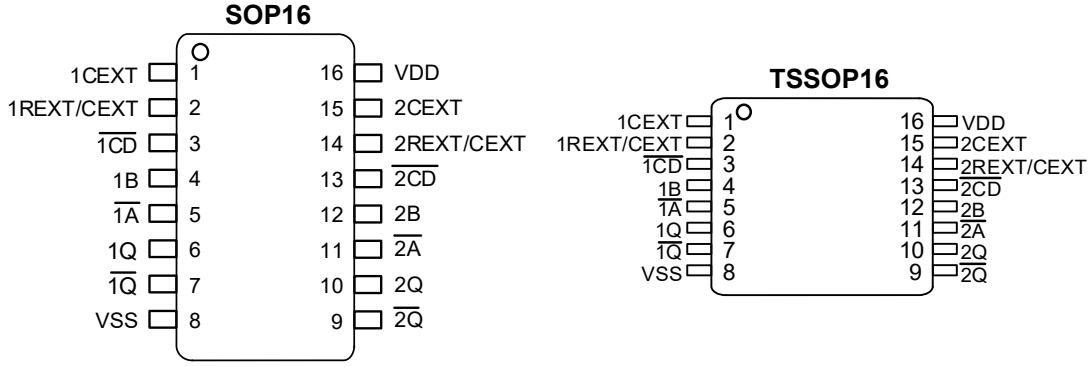


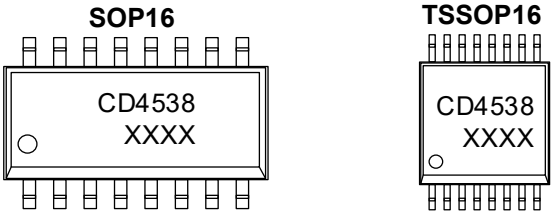
Figure 6-1 Pin configuration

6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	1CEXT	-	External capacitor connection (always connected to ground)
2	1REXT/CEXT	-	External capacitor/resistor connection
3	$\overline{1CD}$	I	Direct reset input (active LOW)
4	1B	I	Input (LOW-to-HIGH triggered)
5	$\overline{1A}$	I	Input (HIGH-to-LOW triggered)
6	1Q	O	Output
7	$\overline{1Q}$	O	Complementary output (active LOW)
8	VSS	G	Ground (0V)
9	$\overline{2Q}$	O	Complementary output (active LOW)
10	2Q	O	Output
11	$\overline{2A}$	I	Input (HIGH-to-LOW triggered)
12	2B	I	Input (LOW-to-HIGH triggered)
13	$\overline{2CD}$	I	Clear direct input (active LOW)
14	2REXT/ CEXT	-	External capacitor/resistor connection
15	2CEXT	-	External capacitor connection (always connected to ground)
16	VDD	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{DD}	Supply voltage	-		-0.5	+14	V
I_{IK}	DC input current	Any one input		-	±10	mA
V_I	Input voltage	All inputs		-0.5	V_{DD}+0.5	V
T_{stg}	Storage temperature	-		-65	+150	°C
P_{tot}	Total power dissipation	-		-	500	mW
P	Device dissipation	Per output transistor		-	100	mW
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	-	3	-	12	V
T_{amb}	Ambient temperature	In free air	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM)(1)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			T_{amb}=25°C			UNIT
		$\|I_O\|$(uA)	V_O(V)	V_{DD}(V)	MIN.	TYP.	MAX.	
I_{DD}	Supply current	Active state V_I=V_{SS} or V_{DD}		5	-	55	-	uA
				10	-	150	-	uA
I_{OL}	LOW-level output current	-	0.4	5	0.5	-	-	mA
		-	0.5	10	1.3	-	-	mA
I_{OH}	HIGH-level output current	-	2.5	5	-	-	-1.4	mA
		-	4.6	5	-	-	-0.5	mA
		-	9.5	10	-	-	-1.3	mA
V_{OL}	LOW-level output voltage	<1	-	5	-	-	0.05	V
		<1	-	10	-	-	0.05	V
V_{OH}	HIGH-level output voltage	<1	-	5	4.95	-	-	V
		<1	-	10	9.95	-	-	V
V_{IL}	LOW-level input voltage	<1	-	5	-	-	1.5	V
		<1	-	10	-	-	3	V
V_{IH}	HIGH-level input voltage	<1	-	5	3.5	-	-	V
		<1	-	10	7	-	-	V
I_I	Input leakage current	$\overline{nA}$, nB		12	-	-	±1.0	uA
		nREXT/CEXT		12	-	-	±1.0	uA

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			T_{amb}=-40°C		T_{amb}=+85°C		T_{amb}=+125°C		UNIT
		$\|I_O\|$(uA)	V_O(V)	V_{DD}(V)	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
I_{OL}	LOW-level output current	-	0.4	5	0.64	-	0.36	-	0.36	-	mA
		-	0.5	10	1.6	-	0.9	-	0.9	-	mA
I_{OH}	HIGH-level output current	-	2.5	5	-	-1.7	-	-1.1	-	-1.1	mA
		-	4.6	5	-	-0.64	-	-0.36	-	-0.36	mA
		-	9.5	10	-	-1.6	-	-0.9	-	-0.9	mA
V_{OL}	LOW-level output voltage	<1	-	5	-	0.05	-	0.05	-	0.05	V
		<1	-	10	-	0.05	-	0.05	-	0.05	V
V_{OH}	HIGH-level output voltage	<1	-	5	4.95	-	4.95	-	4.95	-	V
		<1	-	10	9.95	-	9.95	-	9.95	-	V
V_{IL}	LOW-level input voltage	<1	-	5	-	1.5	-	1.5	-	1.5	V
		<1	-	10	-	3.0	-	3.0	-	3.0	V
V_{IH}	HIGH-level input voltage	<1	-	5	3.5	-	3.5	-	3.5	-	V
		<1	-	10	7.0	-	7.0	-	7.0	-	V
I_I	Input leakage current	$\overline{nA}$, nB		12	-	±0.1	-	±1.0	-	±1.0	uA
		nREXT/CEXT		12	-	±1.0	-	±1.0	-	±1.0	uA

7.4.3 AC Characteristics

T_{amb}=25°C, V_{SS}=0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{PHL}	HIGH to LOW propagation delay	$\overline{nA}$ or nB to $\overline{nQ}$; See Figure 8-4	V_{DD}=5V	-	220	440	ns
			V_{DD}=10V	-	85	190	ns
		$\overline{nCD}$ to nQ; See Figure 8-4	V_{DD}=5V	-	125	250	ns
			V_{DD}=10V	-	55	110	ns
t_{PLH}	LOW to HIGH propagation delay	$\overline{nA}$ or nB to nQ; See Figure 8-4	V_{DD}=5V	-	200	460	ns
			V_{DD}=10V	-	90	180	ns
		$\overline{nCD}$ to $\overline{nQ}$; See Figure 8-4	V_{DD}=5V	-	125	250	ns
			V_{DD}=10V	-	55	110	ns
t_t	Transition time	See Figure 8-4	V_{DD}=5V	-	60	120	ns
			V_{DD}=10V	-	30	60	ns
t_{rec}	Recovery time	$\overline{nCD}$ to $\overline{nA}$ or nB; See Figure 8-5	V_{DD}=5V	-	20	40	ns
			V_{DD}=10V	-	10	20	ns
t_{rtrig}	Retrigger time	nQ, $\overline{nQ}$ to $\overline{nA}$, nB; See Figure 8-5	V_{DD}=5V	0	-	-	ns
			V_{DD}=10V	0	-	-	ns
t_W	Pulse width	$\overline{nA}$ LOW;	V_{DD}=5V	90	-	-	ns

		Minimum width; See Figure 8-5	V_{DD}=10V	30	-	-	ns
		nB HIGH; Minimum width; See Figure 8-5	V_{DD}=5V	50	-	-	ns
			V_{DD}=10V	24	-	-	ns
		$\overline{nCD}$ LOW; Minimum width; See Figure 8-5	V_{DD}=5V	55	-	-	ns
			V_{DD}=10V	25	-	-	ns
		nQ or $n\overline{Q}$; R_{EXT}=100kΩ; C_{EXT}=2nF; See Figure 8-5	V_{DD}=5V	218	-	242	us
			V_{DD}=10V	213	-	235	us
		nQ or $n\overline{Q}$; R_{EXT}=100kΩ; C_{EXT}=0.1uF; See Figure 8-5	V_{DD}=5V	10.3	-	11.3	ms
			V_{DD}=10V	10.2	-	11.2	ms
		nQ or $n\overline{Q}$; R_{EXT}=100kΩ; C_{EXT}=10uF; See Figure 8-5	V_{DD}=5V	1.01	-	1.11	s
			V_{DD}=10V	0.99	-	1.09	s
Δt_W	Pulse width variation	nQ or $n\overline{Q}$ variation over temperature range; See Figure 8-6	V_{DD}=5V	-	±0.2	-	%
			V_{DD}=10V	-	±0.2	-	%
		nQ or $n\overline{Q}$ variation over V_{DD} voltage range 5V to 12V; See Figure 8-7		-	±1.5	-	%
		nQ or $n\overline{Q}$ variation between monostables in the same device; R_{EXT}=100kΩ; C_{EXT}=2nF to 10uF	V_{DD}=5V	-	±1	-	%
			V_{DD}=10V	-	±1	-	%
R_{EXT}	External timing resistor	-		5	-	-	kΩ
C_{EXT}	External timing capacitor	-		2000	-	No limits	pF
C_I	Input capacitance	-		-	-	7.5	pF

Note:

(1) t_t is the same as t_{TLH} and t_{THL}.

(2) The maximum permissible resistance R_{EXT}, which holds the specified accuracy of t_W (nQ, $n\overline{Q}$ output), depends on the leakage current of the capacitor C_{EXT} and the leakage current of the CD4538.

8 Detailed Description

8.1 Overview

The CD4538 is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has an active LOW trigger/retrigger input (/nA), an active HIGH trigger/retrigger input (nB), an overriding active LOW direct reset input (/nCD), an output (nQ) and its complement (/nQ), and two pins (nREXT/CEXT, and nCEXT, always connected to ground) for connecting the external timing components C_{EXT} and R_{EXT}. Typical pulse width variation over the specified temperature range is ±0.2%.

The multivibrator may be triggered by either the positive or the negative edges of the input pulse and will produce an accurate output pulse with a pulse width range of 10us to infinity. The duration and accuracy of the output pulse are determined by the external timing components C_{EXT} and R_{EXT}. The output pulse width (t_W) is equal to $R_{EXT}xC_{EXT}$. The linear design techniques in LOCMOS (Local Oxide CMOS) guarantee precise control of the output pulse width. A LOW level at /nCD terminates the output pulse immediately.

It operates over a recommended V_{DD} power supply range of 3V to 12V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

8.2 Functional Block Diagram

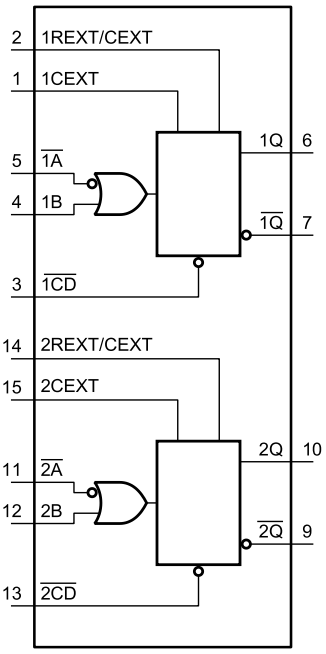


Figure 8-1 Functional diagram

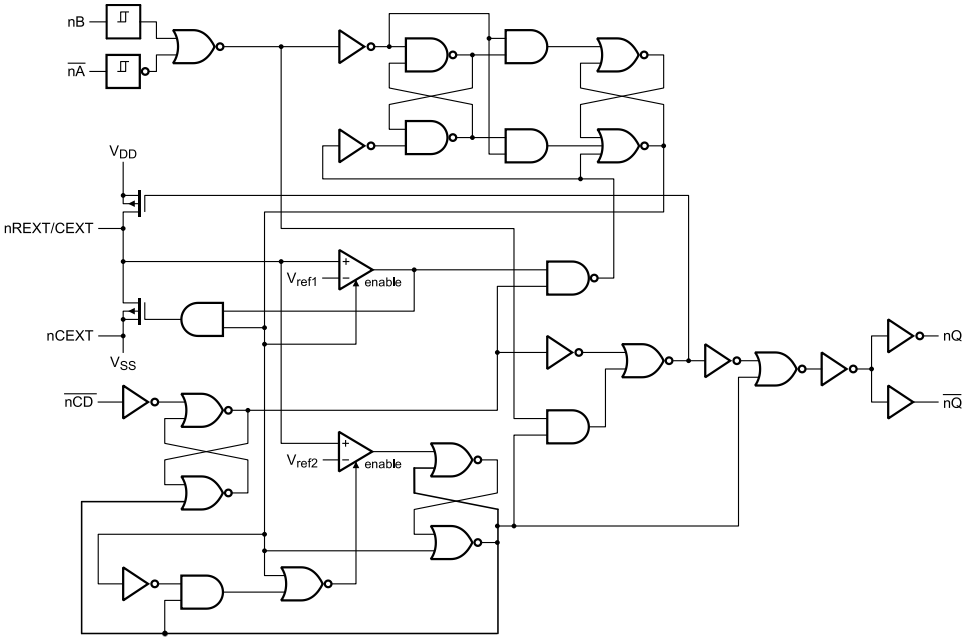


Figure 8-2 Logic diagram (one multivibrator)

8.3 Function Table

INPUT			OUTPUT	
$\overline{nA}$	nB	$\overline{nCD}$	nQ	$\overline{nQ}$
↓	L	H		
H	↑	H		
X	X	L	L	H

Note:

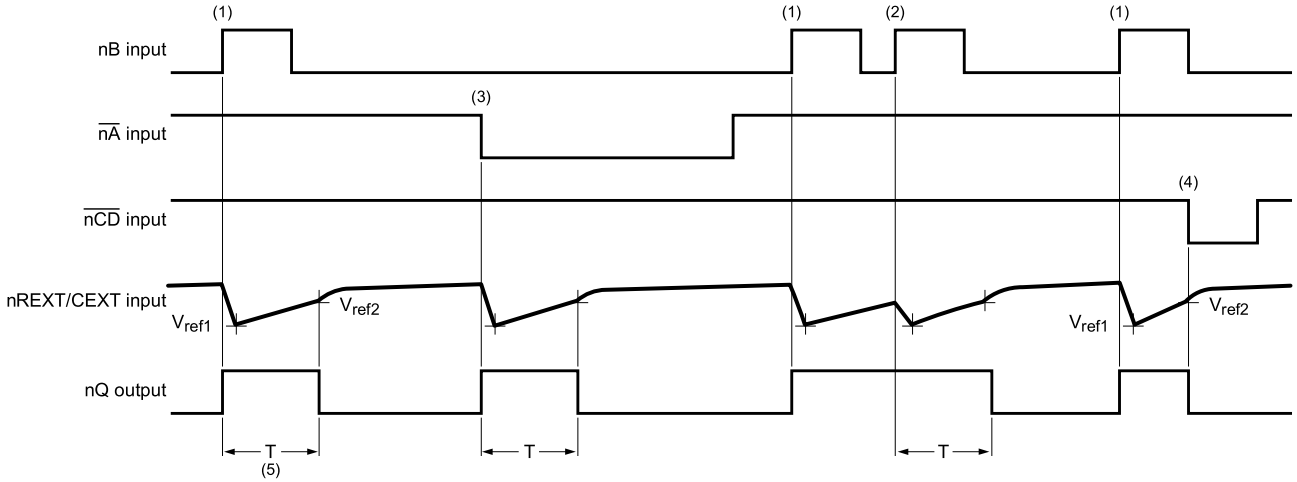
(1) H=HIGH voltage level; L=LOW voltage level; X=don't care;

(2) ↑=positive-going clock transition; ↓=negative-going transition;

(3)  =one HIGH level output pulse, with the pule width determined by C_{EXT} and R_{EXT};

(4)  =one LOW level output pulse, with the pulse width determined by C_{EXT} and R_{EXT}.

8.3.1 Timing Diagram



(1) Positive edge triggering.

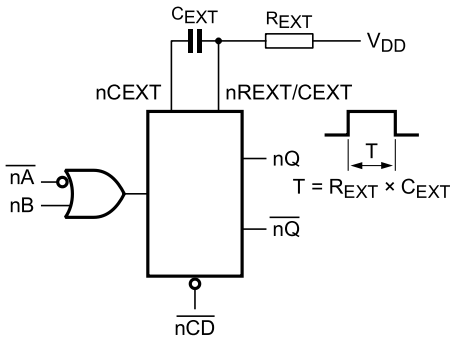
(2) Positive edge re-triggering (pulse lengthening).

(3) Negative edge triggering.

(4) Reset (pulse shortening).

(5) T = REXT×CEXT.

8.3.2 Connection Of The External Timing Components REXT And CEXT



8.4 Testing Circuit

8.4.1 AC Testing Circuit

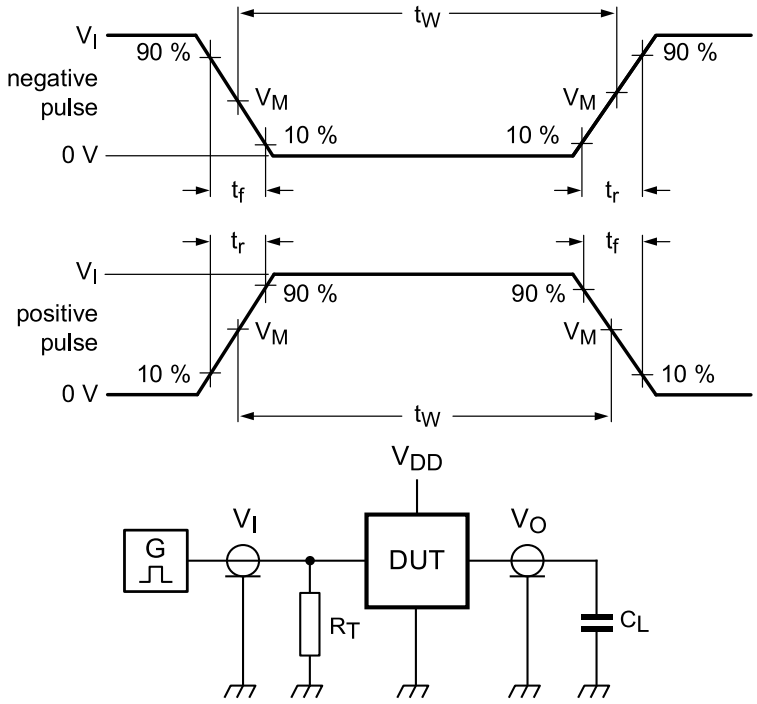


Figure 8-3 Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

8.4.2 AC Testing Waveforms

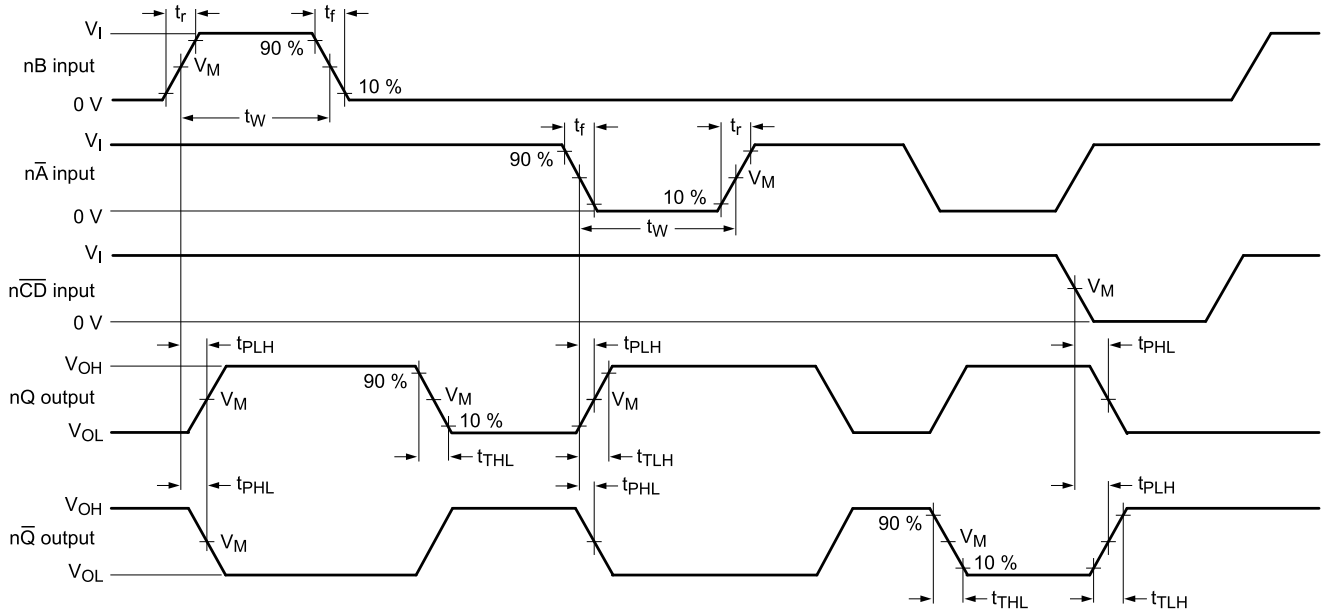


Figure 8-4 Waveforms showing propagation delays

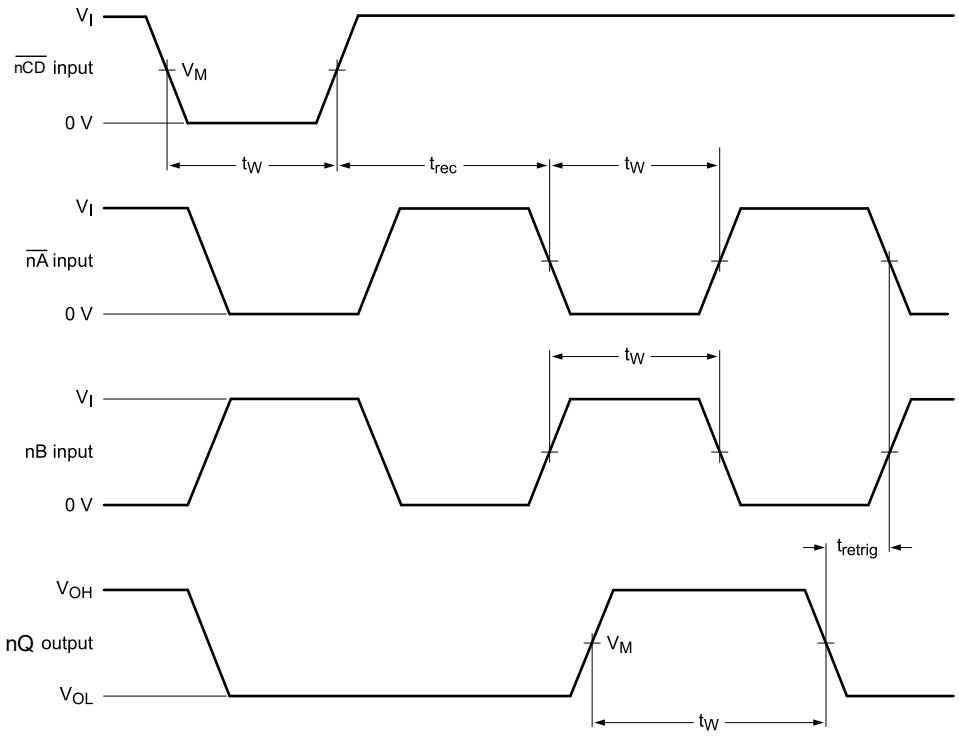
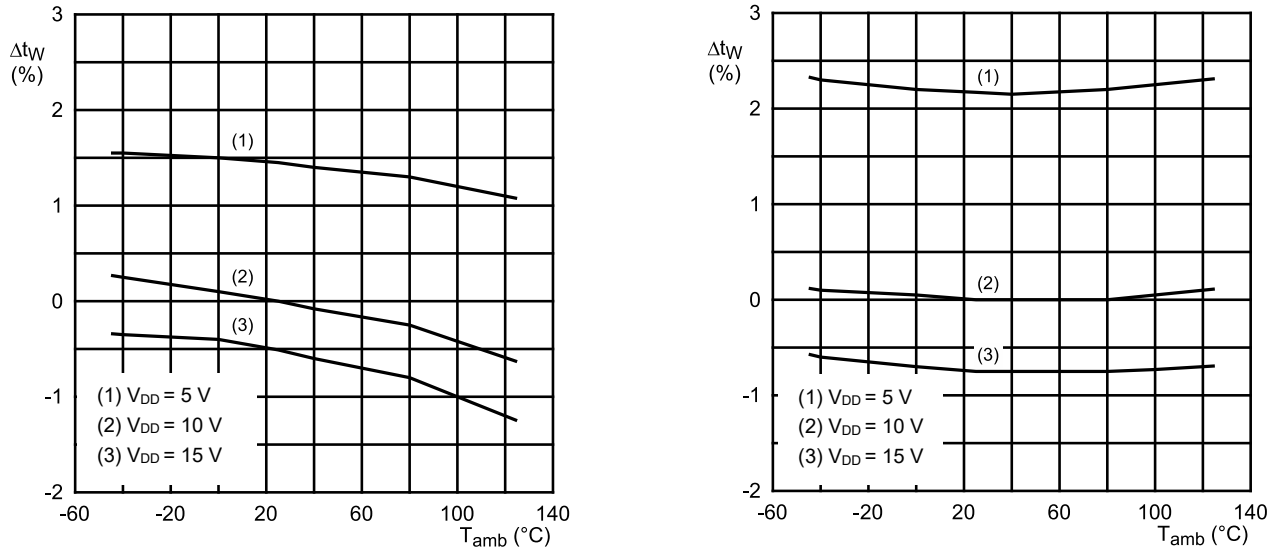


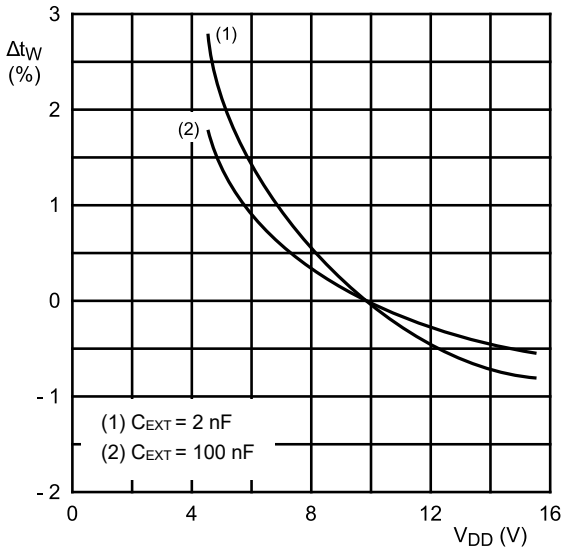
Figure 8-5 Waveforms showing minimum $\overline{nCD}$, $\overline{nA}$, nB, and nQ pulse widths, recovery and retrigger times



a. R_{EXT} = 100 kΩ; C_{EXT} = 100 nF;
Δt_W = 0 % at V_{DD} = 10 V and T_{amb} = 25°C

b. R_{EXT} = 100 kΩ; C_{EXT} = 2 nF;
Δt_W = 0 % at V_{DD} = 10 V and T_{amb} = 25°C

Figure 8-6 Typical normalized change in output pulse width as a function of ambient temperature



T_{amb} = 25°C; Δt_W = 0 % at V_{DD} = 10 V; R_{EXT} = 100 kΩ

Figure 8-7 Typical normalized change in output pulse width as a function of the supply voltage

8.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{DD}	V_M	V_M
5V to 12V	0.5xV_{DD}	0.5xV_{DD}

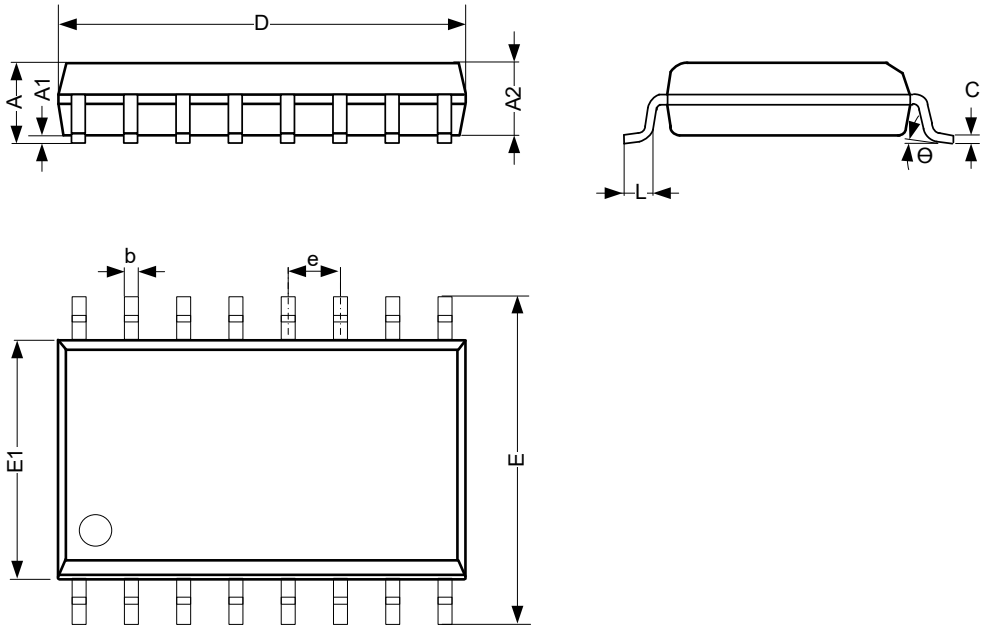
8.4.4 Test Data

SUPPLY VOLTAGE	INPUT		LOAD
V_{DD}	V_I	t_r , t_f	C_L
5V to 12V	V_{SS} or V_{DD}	≤ 20ns	50pF

9 Mechanical Information

9.1 SOP16 Mechanical Information

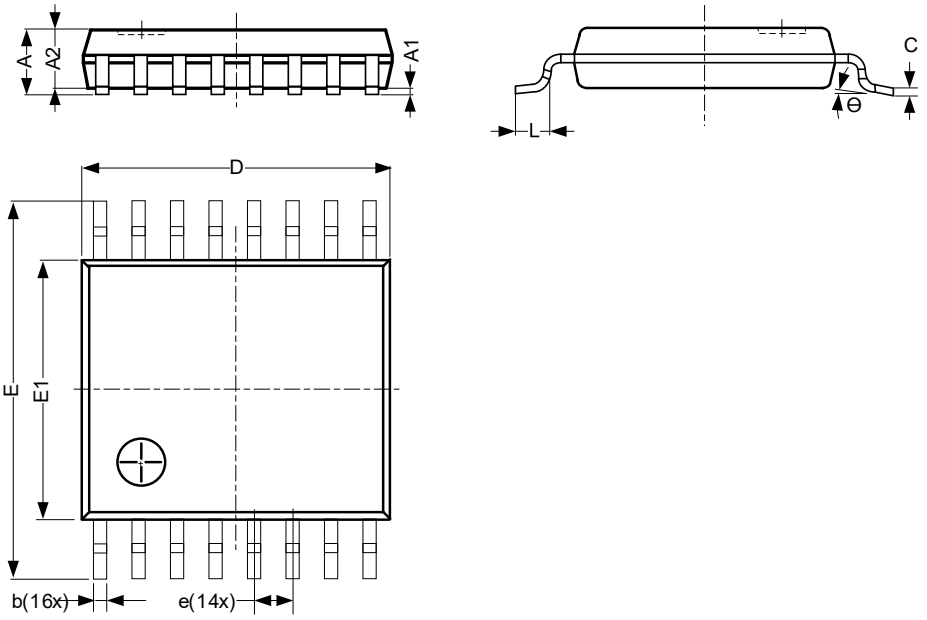
9.1.1 SOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.80
A1	0.10	-	0.25
A2	1.25	-	1.55
b	0.33	-	0.51
c	0.19	-	0.25
D	9.50	-	10.10
E	5.80	-	6.30
E1	3.70	-	4.10
e	1.27 BSC		
L	0.35	-	0.89
θ	0°	-	8°
Unit: mm			

9.2 TSSOP16 Mechanical Information

9.2.1 TSSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

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