8-bit Shift Register with Output Register

CJ74HC/HCT594 Logic

1 Introduction

The CJ74HC594/CJ74HCT594 is an 8-bit serial-in/serial or parallel-out shift register with a storage register.

2 Available Packages

PART NUMBER	PACKAGE
CJ74HC594	SOP16
	TSSOP16
CJ74HCT594	SOP16
	TSSOP16

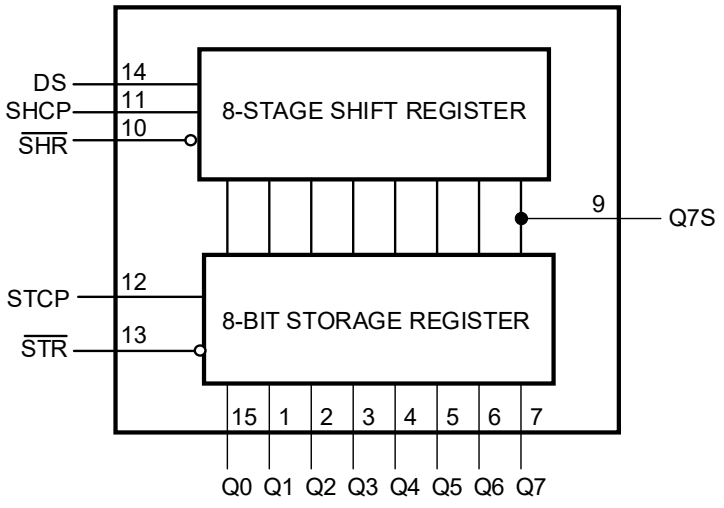
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Supply voltage range:
  - For CJ74HC594: 2~6V
  - For CJ74HCT594: 4.5~5.5V
- Input levels:
  - For CJ74HC594: CMOS level
  - For CJ74HCT594: TTL level
- Temperature range: -40°C to +125°C

4 Applications

- Pro Audio Mixer
- Elevators and Escalators
- Human Machine Interface (HMI): Industrial Monitor
- Entertainment Systems
- Grid Infrastructure: Grid Control
- Access Control and Security: DVR and DVS



Function diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74HC594AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HCT594AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HC594BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active
CJ74HCT594BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

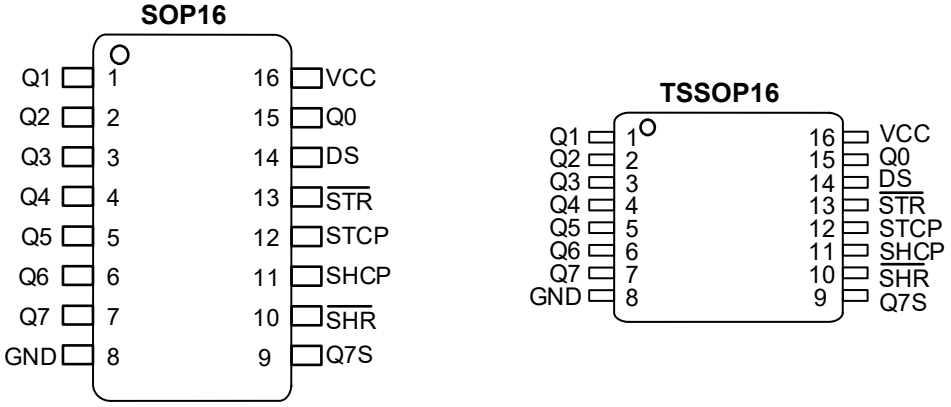


Figure 6-1 Pin configuration

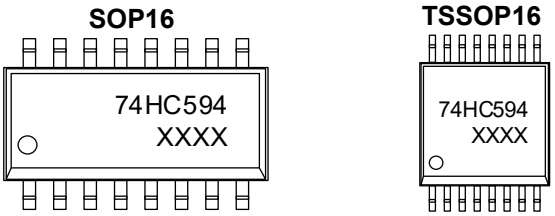
6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	Q1	O	Parallel data output
2	Q2	O	Parallel data output
3	Q3	O	Parallel data output
4	Q4	O	Parallel data output
5	Q5	O	Parallel data output
6	Q6	O	Parallel data output
7	Q7	O	Parallel data output
8	GND	G	Ground (0V)
9	Q7S	O	Serial data output
10	$\overline{SHR}$	I	Shift register reset (active LOW)
11	SHCP	I	Shift register clock input
12	STCP	I	Storage register clock input
13	$\overline{STR}$	I	Storage register reset (active LOW)
14	DS	I	Serial data input
15	Q0	O	Parallel data output
16	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

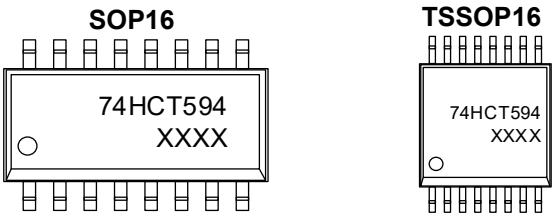
6.3 Marking Information

6.3.1 CJ74HC594



XXXX: Code, indicates weekly record information.

6.3.2 CJ74HCT594



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-		-0.5	+7	V
I_{CC}	Supply current	-		-	50	mA
I_{GND}	Ground current	-		-50	-	mA
I_{IK}	Input clamping current	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
I_{OK}	Output clamping current	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
I_O	Output current	-0.5V < V_O < V_{CC}+0.5V		-	±25	mA
T_{stg}	Storage temperature	-		-65	+150	°C
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC594						
V_{CC}	Supply voltage	-	2.0	5.0	6.0	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C
CJ74HCT594						
V_{CC}	Supply voltage	-	4.5	5.0	5.5	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM)(1)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC594							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	Serial data output Q7S	I_O=-4.0mA; V_{CC}=4.5V	3.84	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	5.81	-	V
		Parallel data outputs	I_O=-6.0mA; V_{CC}=4.5V	3.84	4.32	-	V
			I_O=-7.8mA; V_{CC}=6.0V	5.34	5.81	-	V
V_{OL}	LOW-level output voltage	Serial data output Q7S	I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.33	V
		Parallel data outputs	I_O=6.0mA; V_{CC}=4.5V	-	0.15	0.33	V
			I_O=7.8mA; V_{CC}=6.0V		0.16	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±2	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
CJ74HCT594							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	I_O=-4.0mA; V_{CC}=4.5V Serial data output Q7S		3.84	4.32	-	V
		I_O=-6.0mA; V_{CC}=4.5V Parallel data outputs		3.84	4.32	-	V
V_{OL}	LOW-level output voltage	I_O=4.0mA; V_{CC}=4.5V Serial data output Q7S		-	0.15	0.33	V
		I_O=6.0mA; V_{CC}=4.5V Parallel data outputs		-	0.16	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±2	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
ΔI_{CC}	Additional supply current	One input at V_I=V_{CC}-2.1V. Other inputs at V_{CC} or GND. I_O=0A; V_{CC}=4.5V to 5.5V		-	-	135	uA

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC594							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	Serial data output Q7S	I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
		Parallel data outputs	I_O=-6.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-7.8mA; V_{CC}=6.0V	5.2	-	-	V
V_{OL}	LOW-level output voltage	Serial data output Q7	I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
		Parallel data outputs	I_O=6.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=7.8mA; V_{CC}=6.0V	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±4	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
CJ74HCT594							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	I_O=-4.0mA; V_{CC}=4.5V Serial data output Q7S		3.7	-	-	V
		I_O=-6.0mA; V_{CC}=4.5V Parallel data outputs		3.7	-	-	V
V_{OL}	LOW-level output voltage	I_O=4.0mA; V_{CC}=4.5V Serial data output Q7S		-	-	0.4	V
		I_O=6.0mA; V_{CC}=4.5V Parallel data outputs		-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±4	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
ΔI_{CC}	Additional supply current	One input at V_I=V_{CC}-2.1V. Other inputs at V_{CC} or GND. I_O=0A; V_{CC}=4.5V to 5.5V		-	-	147	uA

7.4.3 AC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC594							
t_{PLH}, t_{PHL}	SHCP to Q7S propagation delay	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	-	44	185	ns
			V_{CC}=4.5V; C_L=50pF	-	16	37	ns
			V_{CC}=5.0V; C_L=15pF	-	13	-	ns
			V_{CC}=6.0V; C_L=50pF	-	14	31	ns
	STCP to Qn propagation delay	See Figure 8-4	V_{CC}=2.0V; C_L=50pF	-	44	185	ns
			V_{CC}=4.5V; C_L=50pF	-	16	37	ns
			V_{CC}=5.0V; C_L=15pF	-	13	-	ns
			V_{CC}=6.0V; C_L=50pF	-	14	31	ns
t_{PHL}	$\overline{SHR}$ to Q7S HIGH to LOW propagation delay	See Figure 8-7	V_{CC}=2.0V; C_L=50pF	-	39	185	ns
			V_{CC}=4.5V; C_L=50pF	-	14	37	ns
			V_{CC}=5.0V; C_L=15pF	-	11	-	ns
			V_{CC}=6.0V; C_L=50pF	-	12	31	ns
	$\overline{STR}$ to Qn HIGH to LOW propagation delay	See Figure 8-8	V_{CC}=2.0V; C_L=50pF	-	39	155	ns
			V_{CC}=4.5V; C_L=50pF	-	14	31	ns
			V_{CC}=5.0V; C_L=15pF	-	11	-	ns
			V_{CC}=6.0V; C_L=50pF	-	12	26	ns
t_{THL}, t_{TLH}	Q7S transition time	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	-	19	95	ns
			V_{CC}=4.5V; C_L=50pF	-	7	19	ns
			V_{CC}=6.0V; C_L=50pF	-	6	16	ns
	Qn transition time		V_{CC}=2.0V; C_L=50pF	-	14	75	ns
			V_{CC}=4.5V; C_L=50pF	-	5	15	ns
			V_{CC}=6.0V; C_L=50pF	-	4	13	ns
t_W	SHCP(HIGH or LOW) pulse width	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	100	-	-	ns
			V_{CC}=4.5V; C_L=50pF	20	-	-	ns
			V_{CC}=6.0V; C_L=50pF	17	-	-	ns
	STCP(HIGH or LOW) pulse width	See Figure 8-4	V_{CC}=2.0V; C_L=50pF	100	-	-	ns
			V_{CC}=4.5V; C_L=50pF	20	-	-	ns
			V_{CC}=6.0V; C_L=50pF	17	-	-	ns
	$\overline{SHR}$ and $\overline{STR}$ (HIGH or LOW)	See Figure 8-7 and Figure 8-8	V_{CC}=2.0V; C_L=50pF	100	-	-	ns
			V_{CC}=4.5V; C_L=50pF	20	-	-	ns
			V_{CC}=6.0V; C_L=50pF	17	-	-	ns
t_{su}	DS to SHCP set_up time	See Figure 8-5	V_{CC}=2.0V; C_L=50pF	125	-	-	ns
			V_{CC}=4.5V; C_L=50pF	25	-	-	ns
			V_{CC}=6.0V; C_L=50pF	21	-	-	ns

	$\overline{SHR}$ to STCP set_up time	See Figure 8-6	V_{CC}=2.0V; C_L=50pF	125	-	-	ns
			V_{CC}=4.5V; C_L=50pF	25	-	-	ns
			V_{CC}=6.0V; C_L=50pF	21	-	-	ns
	SHCP to STCP set_up time	See Figure 8-4	V_{CC}=2.0V; C_L=50pF	125	-	-	ns
			V_{CC}=4.5V; C_L=50pF	25	-	-	ns
			V_{CC}=6.0V; C_L=50pF	21	-	-	ns
t_h	DS to SHCP hold time	See Figure 8-5	V_{CC}=2.0V; C_L=50pF	30	-	-	ns
			V_{CC}=4.5V; C_L=50pF	6	-	-	ns
			V_{CC}=6.0V; C_L=50pF	5	-	-	ns
t_{rec}	$\overline{SHR}$ to SHCP $\overline{STR}$ to STCP recovery time	See Figure 8-7 and Figure 8-8	V_{CC}=2.0V; C_L=50pF	65	-	-	ns
			V_{CC}=4.5V; C_L=50pF	13	-	-	ns
			V_{CC}=6.0V; C_L=50pF	11	-	-	ns
f_{max}	Maximum frequency	See Figure 8-3 and Figure 8-4	V_{CC}=2.0V; C_L=50pF	4.8	30	-	MHz
			V_{CC}=4.5V; C_L=50pF	24	92	-	MHz
			V_{CC}=5.0V; C_L=15pF	-	100	-	MHz
			V_{CC}=6.0V; C_L=50pF	28	109	-	MHz
CJ74HCT594							
t_{PLH}, t_{PHL}	SHCP to Q7S propagation delay	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	-	18	40	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
	STCP to Qn propagation delay	See Figure 8-4	V_{CC}=4.5V; C_L=50pF	-	18	40	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
t_{PHL}	$\overline{SHR}$ to Q7S HIGH to LOW propagation delay	See Figure 8-7	V_{CC}=4.5V; C_L=50pF	-	17	38	ns
			V_{CC}=5.0V; C_L=15pF	-	14	-	ns
	$\overline{STR}$ to Qn HIGH to LOW propagation delay	See Figure 8-8	V_{CC}=4.5V; C_L=50pF	-	17	38	ns
			V_{CC}=5.0V; C_L=15pF	-	14	-	ns
t_{THL}, t_{TLH}	Q7S transition time	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	-	7	19	ns
	Qn transition time		V_{CC}=4.5V; C_L=50pF	-	5	15	ns
t_W	SHCP(HIGH or LOW) pulse width	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	20	-	-	ns
	STCP(HIGH or LOW) pulse width	See Figure 8-4	V_{CC}=4.5V; C_L=50pF	20	-	-	ns
	$\overline{SHR}$ and $\overline{STR}$ (HIGH OR LOW)	See Figure 8-7 and Figure 8-8	V_{CC}=4.5V; C_L=50pF	20	-	-	ns
t_{su}	DS to SHCP set_up time	See Figure 8-5	V_{CC}=4.5V; C_L=50pF	25	-	-	ns
	$\overline{SHR}$ to STCP set_up time	See Figure 8-6	V_{CC}=4.5V; C_L=50pF	25	-	-	ns
	SHCP to STCP set_up time	See Figure 8-4	V_{CC}=4.5V; C_L=50pF	25	-	-	ns
t_h	DS to SHCP hold time	See Figure 8-5	V_{CC}=4.5V; C_L=50pF	6	-	-	ns
t_{rec}	$\overline{SHR}$ to SHCP $\overline{STR}$ to STCP recovery time	See Figure 8-7 and Figure 8-8	V_{CC}=4.5V; C_L=50pF	13	-	-	ns

f_{max}	Maximum frequency	See Figure 8-3 and Figure 8-4	V_{CC}=4.5V; C_L=15pF	24	92	-	MHz

7.4.4 AC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC594							
t_{PLH}, t_{PHL}	SHCP to Q7S propagation delay	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	-	-	225	ns
			V_{CC}=4.5V; C_L=50pF	-	-	45	ns
			V_{CC}=6.0V; C_L=50pF	-	-	38	ns
	STCP to Qn propagation delay	See Figure 8-4	V_{CC}=2.0V; C_L=50pF	-	-	225	ns
			V_{CC}=4.5V; C_L=50pF	-	-	45	ns
			V_{CC}=6.0V; C_L=50pF	-	-	38	ns
t_{PHL}	$\overline{SHR}$ to Q7S HIGH to LOW propagation delay	See Figure 8-7	V_{CC}=2.0V; C_L=50pF	-	-	225	ns
			V_{CC}=4.5V; C_L=50pF	-	-	45	ns
			V_{CC}=6.0V; C_L=50pF	-	-	38	ns
	$\overline{STR}$ to Qn HIGH to LOW propagation delay	See Figure 8-8	V_{CC}=2.0V; C_L=50pF	-	-	185	ns
			V_{CC}=4.5V; C_L=50pF	-	-	37	ns
			V_{CC}=6.0V; C_L=50pF	-	-	31	ns
t_{THL}, t_{TLH}	Q7S transition time	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	-	-	110	ns
			V_{CC}=4.5V; C_L=50pF	-	-	22	ns
			V_{CC}=6.0V; C_L=50pF	-	-	19	ns
	Qn transition time		V_{CC}=2.0V; C_L=50pF	-	-	90	ns
			V_{CC}=4.5V; C_L=50pF	-	-	18	ns
			V_{CC}=6.0V; C_L=50pF	-	-	15	ns
t_W	SHCP(HIGH or LOW) pulse width	See Figure 8-3	V_{CC}=2.0V; C_L=50pF	120	-	-	ns
			V_{CC}=4.5V; C_L=50pF	24	-	-	ns
			V_{CC}=6.0V; C_L=50pF	20	-	-	ns
	STCP(HIGH or LOW) pulse width	See Figure 8-4	V_{CC}=2.0V; C_L=50pF	120	-	-	ns
			V_{CC}=4.5V; C_L=50pF	24	-	-	ns
			V_{CC}=6.0V; C_L=50pF	20	-	-	ns
	$\overline{SHR}$ and $\overline{STR}$ (HIGH or LOW)	See Figure 8-7 and Figure 8-8	V_{CC}=2.0V; C_L=50pF	120	-	-	ns
			V_{CC}=4.5V; C_L=50pF	24	-	-	ns
			V_{CC}=6.0V; C_L=50pF	20	-	-	ns
t_{su}	DS to SHCP set_up time	See Figure 8-5	V_{CC}=2.0V; C_L=50pF	150	-	-	ns
			V_{CC}=4.5V; C_L=50pF	30	-	-	ns
			V_{CC}=6.0V; C_L=50pF	26	-	-	ns
	$\overline{SHR}$ to STCP set_up time	See Figure 8-6	V_{CC}=2.0V; C_L=50pF	150	-	-	ns
			V_{CC}=4.5V; C_L=50pF	30	-	-	ns

			V_{CC}=6.0V; C_L=50pF	26	-	-	ns
	SHCP to STCP set_up time	See Figure 8-5	V_{CC}=2.0V; C_L=50pF	150	-	-	ns
			V_{CC}=4.5V; C_L=50pF	30	-	-	ns
			V_{CC}=6.0V; C_L=50pF	26	-	-	ns
t_h	DS to SHCP hold time	See Figure 5	V_{CC}=2.0V; C_L=50pF	35	-	-	ns
			V_{CC}=4.5V; C_L=50pF	7	-	-	ns
			V_{CC}=6.0V; C_L=50pF	6	-	-	ns
t_{rec}	$\overline{SHR}$ to SHCP $\overline{STR}$ to STCP recovery time	See Figure 8-7 and Figure 8-8	V_{CC}=2.0V; C_L=50pF	75	-	-	ns
			V_{CC}=4.5V; C_L=50pF	15	-	-	ns
			V_{CC}=6.0V; C_L=50pF	13	-	-	ns
f_{max}	Maximum frequency	See Figure 8-3 and Figure 8-4	V_{CC}=2.0V; C_L=50pF	4	-	-	MHz
			V_{CC}=4.5V; C_L=50pF	20	-	-	MHz
			V_{CC}=6.0V; C_L=50pF	24	-	-	MHz
CJ74HCT594							
t_{PLH}, t_{PHL}	SHCP to Q7S propagation delay	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	-	-	48	ns
	STCP to Qn propagation delay	See Figure 8-4	V_{CC}=4.5V; C_L=50pF	-	-	48	ns
t_{PHL}	$\overline{SHR}$ to Q7S HIGH to LOW propagation delay	See Figure 8-7	V_{CC}=4.5V; C_L=50pF	-	-	45	ns
	$\overline{STR}$ to Qn HIGH to LOW propagation delay	See Figure 8-8	V_{CC}=4.5V; C_L=50pF	-	-	45	ns
t_{THL}, t_{TLH}	Q7S transition time	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	-	-	22	ns
	Qn transition time		V_{CC}=4.5V; C_L=50pF	-	-	18	ns
t_W	SHCP(HIGH or LOW) pulse width	See Figure 8-3	V_{CC}=4.5V; C_L=50pF	24	-	-	ns
	STCP(HIGH or LOW) pulse width	See Figure 8-4	V_{CC}=4.5V; C_L=50pF	24	-	-	ns
	$\overline{SHR}$ and $\overline{STR}$ (HIGH OR LOW)	See Figure 8-7 and Figure 8-8	V_{CC}=4.5V; C_L=50pF	24	-	-	ns
t_{su}	DS to SHCP set_up time	See Figure 8-5	V_{CC}=4.5V; C_L=50pF	30	-	-	ns
	$\overline{SHR}$ to STCP set_up time	See Figure 8-6	V_{CC}=4.5V; C_L=50pF	30	-	-	ns
	SHCP to STCP set_up time	See Figure 8-4	V_{CC}=4.5V; C_L=50pF	30	-	-	ns
t_h	DS to SHCP hold time	See Figure 8-5	V_{CC}=4.5V; C_L=50pF	7	-	-	ns
t_{rec}	$\overline{SHR}$ to SHCP $\overline{STR}$ to STCP recovery time	See Figure 8-7 and Figure 8-8	V_{CC}=4.5V; C_L=50pF	15	-	-	ns
f_{max}	Maximum frequency	See Figure 8-3 and Figure 8-4	V_{CC}=4.5V; C_L=15pF	20	-	-	MHz

8 Detailed Description

8.1 Overview

The CJ74HC594/CJ74HCT594 is an 8-bit serial-in/serial or parallel-out shift register with a storage register.

8.2 Functional Block Diagram

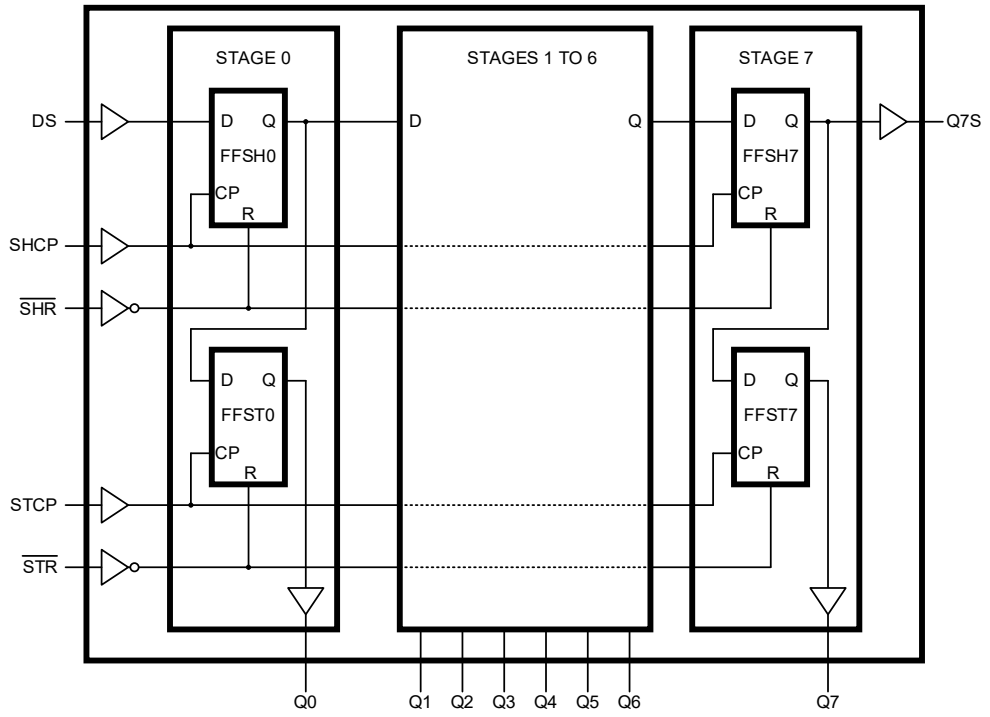


Figure 8-1 Logic symbol

8.3 Function Table(1)

INPUT					FUNCTION
$\overline{SHR}$	$\overline{STR}$	SHCP	STCP	DS	
L	X	X	X	X	Clear shift register
X	L	X	X	X	Clear storage register
H	X	↑	X	H or L	Load DS into shift register stage 0, advance previous stage data to the next stage
X	H	X	↑	X	Transfer shift register data to storage register and outputs Qn
H	H	↑	↑	X	Shift register one count pulse ahead of storage register

(1) H=HIGH voltage level; L=LOW voltage level; ↑ =LOW-to-HIGH transition; X=don't care

8.4 Testing Circuit

8.4.1 AC Testing Circuit

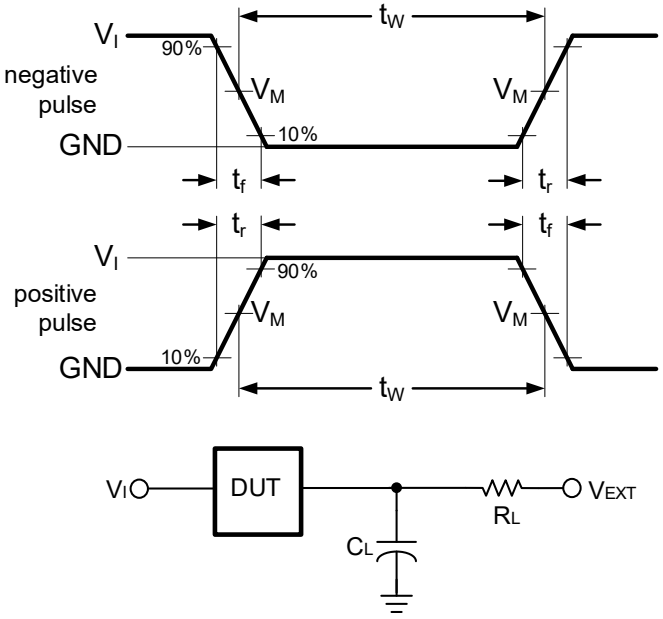


Figure 8-2 Test circuit for measuring switching times

Definitions for test circuit:

C_L= includes probe and jig capacitance.

8.4.2 AC Testing Waveforms

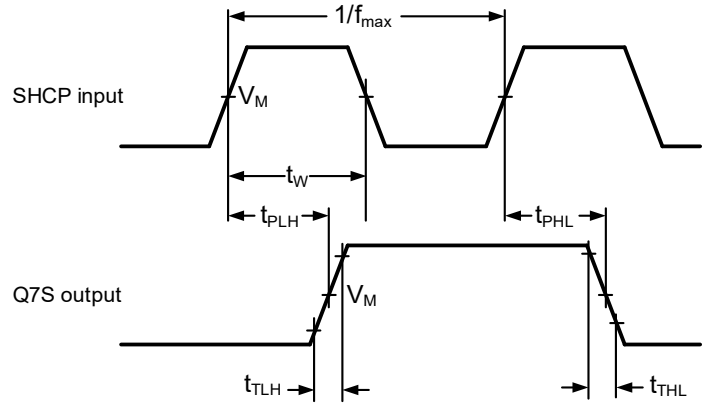


Figure 8-3 The shift clock (SHCP) to output (Q7S) propagation delays, the shift clock pulse width, the maximum shift clock frequency, and output transition times

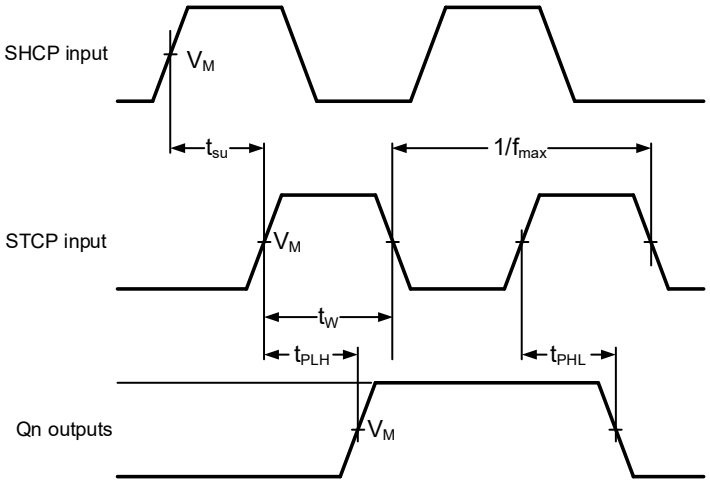


Figure 8-4 The storage clock (STCP) to output (Qn), propagation delays, the storage clock pulse width, the maximum storage clock pulse frequency and the shift clock to storage clock set-up time

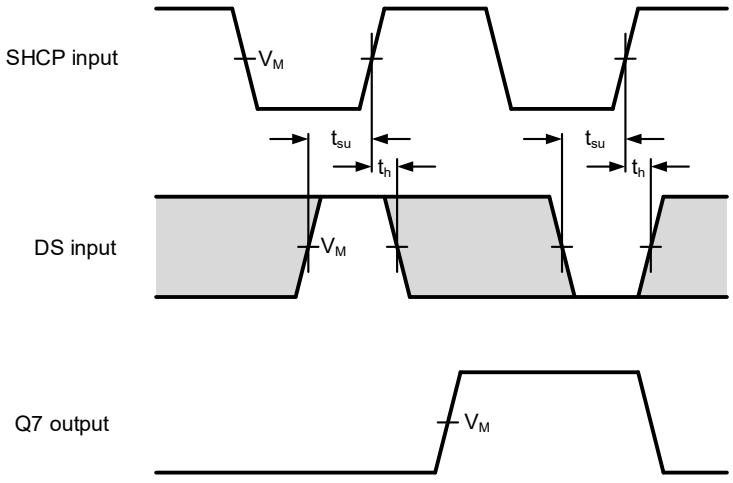


Figure 8-5 The data set-up time and hold times for DS input to SHCP

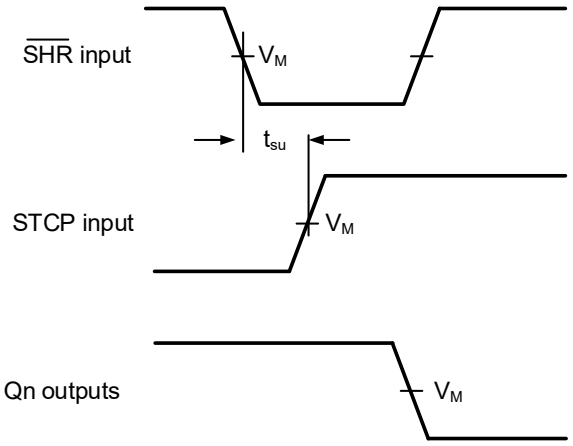


Figure 8-6 The set-up time shift reset ($\overline{SHR}$) to storage clock (STCP)

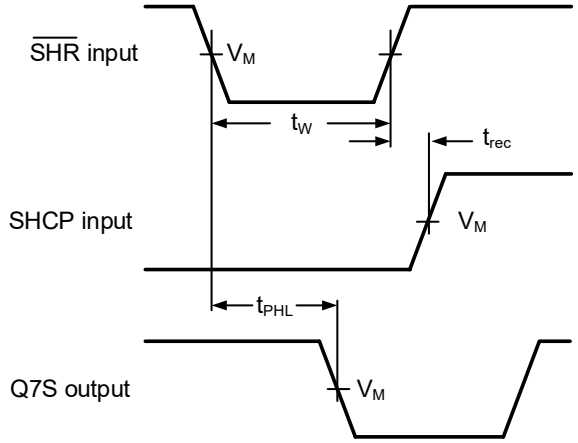


Figure 8-7 The shift reset ($\overline{SHR}$) pulse width, the shift reset to output (Q7S) propagation delay and the shift reset to shift clock (SHCP) recovery time

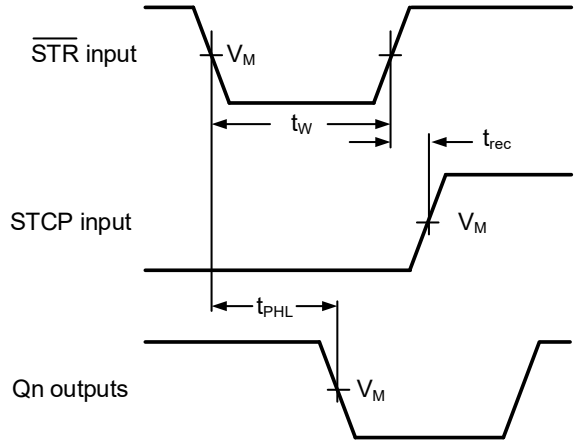


Figure 8-8 The storage reset ($\overline{STR}$) pulse width, the storage reset to output (Qn) propagation delay and the storage reset to storage clock (STCP) recovery time

8.4.3 Measurement Points

TYPE	INPUT	OUTPUT
	V_M	V_M
CJ74HC594	0.5xV_{CC}	0.5xV_{CC}
CJ74HCT594	1.3V	1.3V

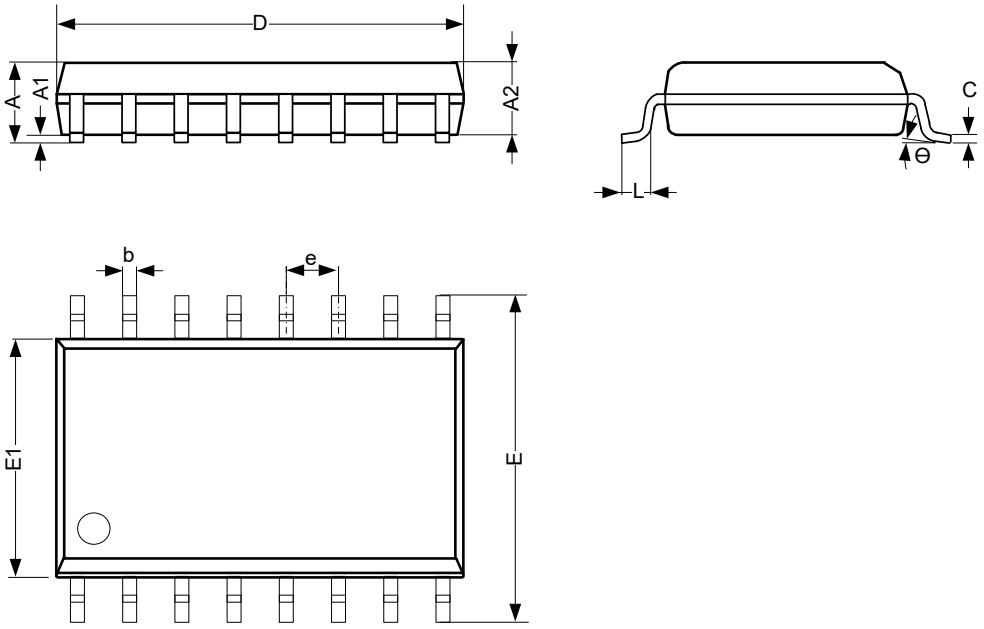
8.4.4 Test Data

TYPE	INPUT		LOAD		V_{EXT}		
	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ},t_{PZL}	t_{PHZ},t_{PZH}
CJ74HC594	V_{CC}	3.0ns	15pF, 50pF	1kΩ	Open	V_{CC}	GND
CJ74HCT594	3V	3.0ns	15pF, 50pF	1kΩ	Open	V_{CC}	GND

9 Mechanical Information

9.1 SOP16 Mechanical Information

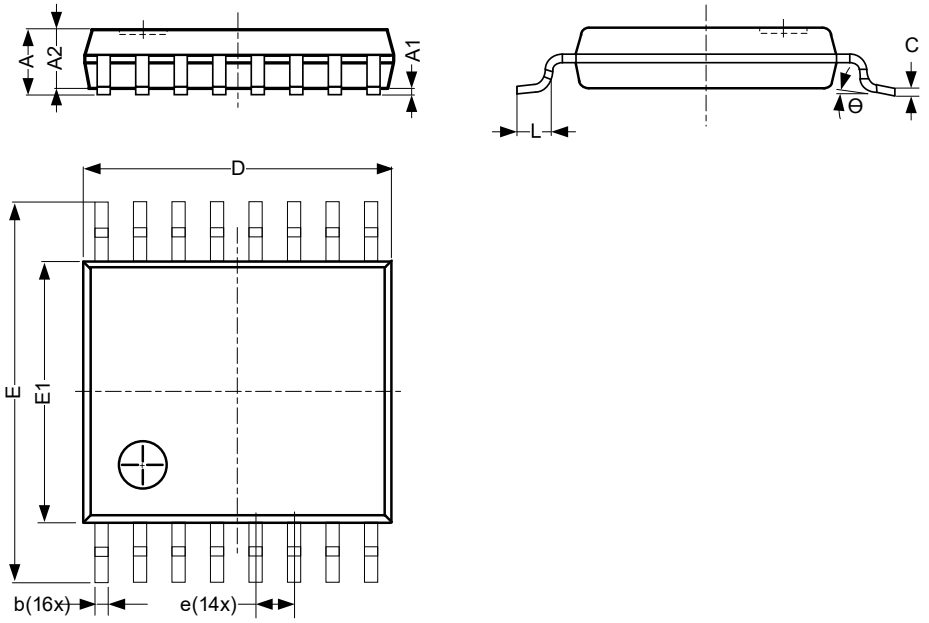
9.1.1 SOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.80
A1	0.10	-	0.25
A2	1.25	-	1.55
b	0.33	-	0.51
c	0.19	-	0.25
D	9.50	-	10.10
E	5.80	-	6.30
E1	3.70	-	4.10
e	1.27 BSC		
L	0.35	-	0.89
θ	0°	-	8°
Unit: mm			

9.2 TSSOP16 Mechanical Information

9.2.1 TSSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of JSCJ, this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. JSCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

Official Website: www.jscj-elec.com