

Dual 4-channel Analog Multiplexer/Demultiplexer

CD4052H

Logic

1 Introduction

The CD4052H is a dual 4-channel analogue multiplexer/demultiplexer with common channel select logic. Each multiplexer/demultiplexer has four independent inputs/outputs (nY0 to nY3) and a common input/output (nZ). The common channel select logic includes two select inputs (S1 and S2) and an active LOW enable input(/E). Both multiplexers/demultiplexers contain four bidirectional analog switches, each with one side connected to an independent input/output (nY0 to nY3) and the other side connected to a common input/output (nZ). With /E LOW, one of the four switches is selected (low-impedance ON-state) by S1 and S2. With /E HIGH, all switches are in the high-impedance OFF-state, independent of S1 and S2. If break before make is needed, then it is necessary to use the enable input.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S1 and S2, and /E). The V_{DD} to V_{SS} range is 3V to 18V. The analog inputs/outputs (nY0 to nY3, and nZ) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}-V_{EE} may not exceed 18V. Unused inputs must be connected to V_{DD}, V_{SS}, or another input. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground). V_{EE} and V_{SS} are the supply voltage connections for the switches.

2 Available Packages

PART NUMBER	PACKAGE
CD4052H	SOP16
	TSSOP16

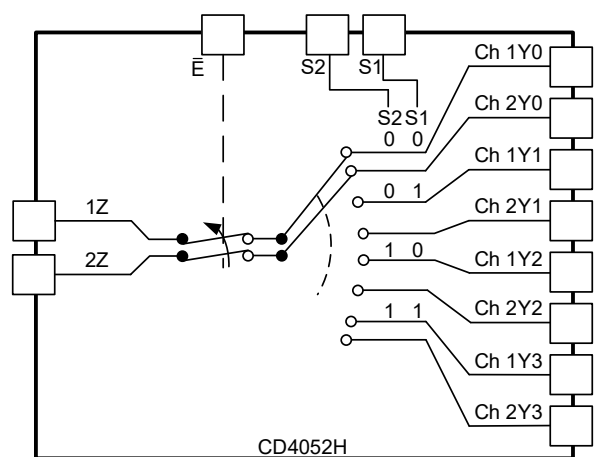
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range from 3V to 18V
- Fully static operation
- 5V, 10V and 18V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C

4 Applications

- Analog and digital multiplexing and demultiplexing
- Analog to digital and digital to analog conversion
- Signal gating
- Factory automation
- Televisions
- Appliances
- Consumer audio
- Programmable logic circuits
- Sensors



Functional Diagrams

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CD4052HAEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units/Reel	Active
CD4052HBEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units/Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

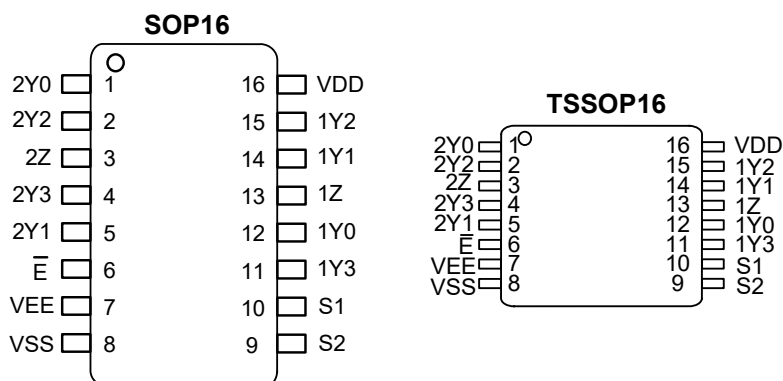


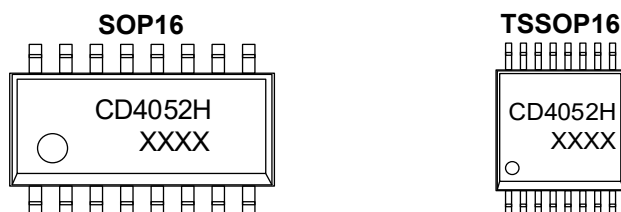
Figure 6-1 Pin Configuration

6.2 Pin Function

PIN		I/O ⁽¹⁾	DESCRIPTION
No.	NAME		
1	2Y0	I/O	Independent input or output
2	2Y2	I/O	Independent input or output
3	2Z	I/O	Common output or input
4	2Y3	I/O	Independent input or output
5	2Y1	I/O	Independent input or output
6	$\bar{E}$	I	Enable input (active LOW)
7	VEE	P	Supply voltage
8	VSS	G	Ground (0V)
9	S2	I	Select input
10	S1	I	Select input
11	1Y3	I/O	Independent input or output
12	1Y0	I/O	Independent input or output
13	1Z	I/O	Common output or input
14	1Y1	I/O	Independent input or output
15	1Y2	I/O	Independent input or output
16	VDD	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground.

6.3 Marking Information



CD4052H: Device number.
XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

$T_{amb}=25^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	CONDITIONS		MIN.	MAX.	UNIT
V_{DD}	Supply voltage	-		-0.5	+21	V
V_{EE}	Supply voltage	Referenced to V_{DD}		-21	+0.5	V
V_I	Input voltage	-		-0.5	$V_{DD}+0.5$	V
I_{IK}	Input clamping current	$V_I < -0.5\text{V}$ or $V_I > V_{DD}+0.5\text{V}$		-	± 10	mA
I_{IO}	Input/output current	-		-	± 10	mA
I_{DD}	Supply current	-		-	50	mA
T_{stg}	Storage temperature	-		-65	+150	$^{\circ}\text{C}$
T_{amb}	Ambient temperature	-		-40	+125	$^{\circ}\text{C}$
P_{tot}	Total power dissipation	-		-	500	mW
P	Device dissipation	Per output transistor		-	100	mW
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	$^{\circ}\text{C}$

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

$T_{amb}=25^{\circ}\text{C}$; $R_L=10\text{k}\Omega$; $C_L=50\text{pF}$; $/E=V_{DD}$; $V_{IS}=V_{DD}=5\text{V}$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	-	3	-	18	V
V_{EE}	Supply voltage	-	-15	-	0	V
$V_{DD}-V_{EE}$	Supply voltage	-	3	-	18	V
V_I	Input voltage	-	0	-	V_{DD}	V
T_{amb}	Ambient temperature	In free air	-40	-	+125	$^{\circ}\text{C}$
$\Delta t/\Delta V$	Input transition rise and fall rate	$V_{DD}=5\text{V}$	-	-	3.75	us/V
		$V_{DD}=10\text{V}$	-	-	0.5	us/V
		$V_{DD}=18\text{V}$	-	-	0.08	us/V

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) ⁽¹⁾	± 2000	V

(1) JEDEC document JEP155 states that 500-V H1BM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

$T_{amb}=25^{\circ}\text{C}$, $V_{SS}=V_{EE}=0\text{V}$; $V_I=V_{SS}$ or V_{DD} , $I_{SW}=200\mu\text{A}$, unless otherwise specified.

SYMBOL	CHARACTERISTIC	CONDITIONS		T _{amb} =25°C			UNIT
				MIN.	TYP.	MAX.	
V _{IH}	HIGH-level input voltage	I _O <1uA	V _{DD} =5V	3.5	-	-	V
			V _{DD} =10V	7.0	-	-	V
			V _{DD} =18V	12.6	-	-	V
V _{IL}	LOW-level input voltage	I _O <1uA	V _{DD} =5V	-	-	1.5	V
			V _{DD} =10V	-	-	3.0	V
			V _{DD} =18V	-	-	5.4	V
I _{DD}	Supply current	I _O =0A	V _{DD} =5V	-	-	5	uA
			V _{DD} =10V	-	-	10	uA
			V _{DD} =18V	-	-	20	uA
I _I	Input leakage current	V _{DD} =18V		-	-	±1.0	uA
I _{S(OFF)}	OFF-state leakage current	V _{DD} =18V	Z port; All channels OFF; See Figure 8-6	-	-	±1.0	uA
			Y port; Per channel; See Figure 8-7	-	-	±1.0	uA
R _{ON(peak)}	ON resistance (peak)	V _I =0V to V _{DD} -V _{EE} ; See Figure 8-8 and Figure 8-9	V _{DD} -V _{EE} =5V	-	117	836	Ω
			V _{DD} -V _{EE} =10V	-	58	178	Ω
			V _{DD} -V _{EE} =15V	-	41	120	Ω
			V _{DD} -V _{EE} =20V	-	36	105	Ω
R _{ON(rail)}	ON resistance (rail)	V _I =0V; See Figure 8-8 and Figure 8-9	V _{DD} -V _{EE} =5V	-	44	130	Ω
			V _{DD} -V _{EE} =10V	-	29	93	Ω
			V _{DD} -V _{EE} =15V	-	24	69	Ω
			V _{DD} -V _{EE} =20V	-	22	63	Ω
		V _I =V _{DD} -V _{EE} ; See Figure 8-8 and Figure 8-9	V _{DD} -V _{EE} =5V	-	82	249	Ω
			V _{DD} -V _{EE} =10V	-	51	157	Ω
			V _{DD} -V _{EE} =15V	-	41	127	Ω
			V _{DD} -V _{EE} =20V	-	36	112	Ω
ΔR _{ON}	ON resistance mismatch between channels	V _I =0V to V _{DD} -V _{EE} ; See Figure 8-8	V _{DD} -V _{EE} =5V	-	25	-	Ω
			V _{DD} -V _{EE} =10V	-	10	-	Ω
			V _{DD} -V _{EE} =15V	-	5	-	Ω
			V _{DD} -V _{EE} =20V	-	5	-	Ω
C _I	Input capacitance	Sn, E inputs		-	-	7.5	pF

7.4.2 DC Characteristics 2

$T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{SS} = V_{EE} = 0\text{V}$; $V_I = V_{SS}$ or V_{DD} , unless otherwise specified.

SYMBOL	CHARACTERISTIC	CONDITIONS		$T_{amb} = -40^{\circ}\text{C}$		$T_{amb} = +85^{\circ}\text{C}$		$T_{amb} = +125^{\circ}\text{C}$		UNIT
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage	$ I_O < 1\mu\text{A}$	$V_{DD} = 5\text{V}$	3.5	-	3.5	-	3.5	-	V
			$V_{DD} = 10\text{V}$	7.0	-	7.0	-	7.0	-	V
			$V_{DD} = 18\text{V}$	12.6	-	12.6	-	12.6	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1\mu\text{A}$	$V_{DD} = 5\text{V}$	-	1.5	-	1.5	-	1.5	V
			$V_{DD} = 10\text{V}$	-	3.0	-	3.0	-	3.0	V
			$V_{DD} = 18\text{V}$	-	5.4	-	5.4	-	5.4	V
I_{DD}	Supply current	$I_O = 0\text{A}$	$V_{DD} = 5\text{V}$	-	5	-	150	-	150	μA
			$V_{DD} = 10\text{V}$	-	10	-	300	-	300	μA
			$V_{DD} = 18\text{V}$	-	20	-	600	-	600	μA
I_I	Input leakage current	$V_{DD} = 18\text{V}$		-	± 1.0	-	± 1.0	-	± 1.0	μA

7.4.3 AC Characteristics 1

$T_{amb} = 25^{\circ}\text{C}$, $V_{EE} = V_{SS} = 0\text{V}$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PHL}	HIGH to LOW propagation delay time	nY_n, nZ to nZ, nY_n ; See Figure 8-11	$V_{DD} = 5\text{V}$	-	10	20 ns
			$V_{DD} = 10\text{V}$	-	5	10 ns
			$V_{DD} = 18\text{V}$	-	5	10 ns
		S_n to nY_n, nZ ; See figure 8-12	$V_{DD} = 5\text{V}$	-	150	305 ns
			$V_{DD} = 10\text{V}$	-	65	135 ns
			$V_{DD} = 18\text{V}$	-	50	100 ns
t_{PLH}	LOW to HIGH propagation delay	nY_n, nZ to nZ, nY_n ; See Figure 8-11	$V_{DD} = 5\text{V}$	-	10	20 ns
			$V_{DD} = 10\text{V}$	-	5	10 ns
			$V_{DD} = 18\text{V}$	-	5	10 ns
		S_n to nY_n, nZ ; See Figure 8-12	$V_{DD} = 5\text{V}$	-	150	300 ns
			$V_{DD} = 10\text{V}$	-	75	150 ns
			$V_{DD} = 18\text{V}$	-	50	100 ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\bar{E}$ to nY_n, nZ ; See Figure 8-13	$V_{DD} = 5\text{V}$	-	95	190 ns
			$V_{DD} = 10\text{V}$	-	90	180 ns
			$V_{DD} = 18\text{V}$	-	85	180 ns
t_{PLZ}	LOW to OFF-state propagation delay	$\bar{E}$ to nY_n, nZ ; See Figure 8-13	$V_{DD} = 5\text{V}$	-	100	205 ns
			$V_{DD} = 10\text{V}$	-	90	180 ns
			$V_{DD} = 18\text{V}$	-	90	180 ns
t_{PZH}	OFF-state to HIGH propagation delay	$\bar{E}$ to nY_n, nZ ; See Figure 8-13	$V_{DD} = 5\text{V}$	-	130	260 ns
			$V_{DD} = 10\text{V}$	-	55	115 ns

			$V_{DD}=18V$	-	45	85	ns
t_{PZL}	OFF-state to LOW propagation delay	$\bar{E}$ to nYn, nZ; See Figure 8-13	$V_{DD}=5V$	-	120	240	ns
			$V_{DD}=10V$	-	50	100	ns
			$V_{DD}=18V$	-	35	75	ns

7.4.4 AC Characteristics 2

$T_{amb}=25^{\circ}C$, $V_{EE}=V_{SS}=0V$, $V_I=0.5V_{DD}$ (p-p), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
THD	Total harmonic distortion	See Figure 8-14; R _L =10kΩ; C _L =15pF; Channel ON; f _i =1kHz	V _{DD} =5V	-	0.25	-	%
			V _{DD} =10V	-	0.04	-	%
			V _{DD} =18V	-	0.04	-	%
f _(-3dB)	-3db frequency response	See Figure 8-15; R _L =1kΩ; C _L =5pF; Channel ON;	V _{DD} =5V	-	13	-	MHz
			V _{DD} =10V	-	40	-	MHz
			V _{DD} =18V	-	70	-	MHz
α _{iso}	Isolation (OFF-state)	See Figure 8-16; f _i =1MHz; R _L =1kΩ; C _L =5pF; Channel OFF; V _{DD} =10V	-	-50	-	dB	
V _{ct}	Crosstalk voltage	Digital inputs to switch; See Figure 8-17; R _L =10kΩ; C _L =15pF; $\bar{E}$ or Sn=V _{DD} (square-wave); V _{DD} =10V	-	50	-	mV	
Xtalk	Crosstalk	Between switches; See Figure 8-18; f _i =1MHz; R _L =1kΩ; V _{DD} =10V	-	-50	-	dB	

(1) f_i is biased at $0.5V_{DD}$; $V_I=0.5V_{DD}$ (p-p).

8 Detailed Description

8.1 Overview

The CD4052H is a dual 4-channel analogue multiplexer/demultiplexer with common channel select logic. Each multiplexer/demultiplexer has four independent inputs/outputs (nY0 to nY3) and a common input/output (nZ). The common channel select logic includes two select inputs (S1 and S2) and an active LOW enable input (/E). Both multiplexers/demultiplexers contain four bidirectional analog switches, each with one side connected to an independent input/output (nY0 to nY3) and the other side connected to a common input/output (nZ). With /E LOW, one of the four switches is selected (low-impedance ON-state) by S1 and S2. With /E HIGH, all switches are in the high-impedance OFF-state, independent of S1 and S2. If break before make is needed, then it is necessary to use the enable input.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S1 and S2, and /E). The V_{DD} to V_{SS} range is 3V to 18V. The analog inputs/outputs (nY0 to nY3, and nZ) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD}-V_{EE}$ may not exceed 18V. Unused inputs must be connected to V_{DD} , V_{SS} , or another input. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground). V_{EE} and V_{SS} are the supply voltage connections for the switches.

8.2 Functional Block Diagram

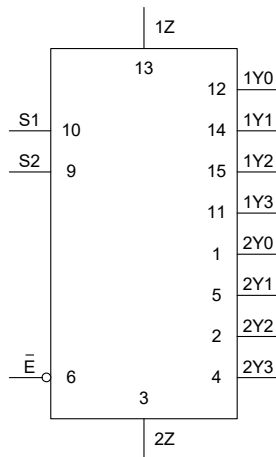


Figure 8-1 Logic symbol

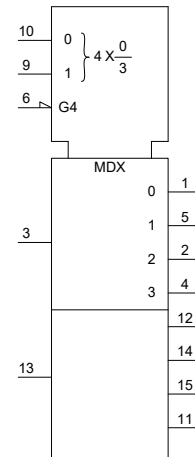


Figure 8-2 IEC logic symbol

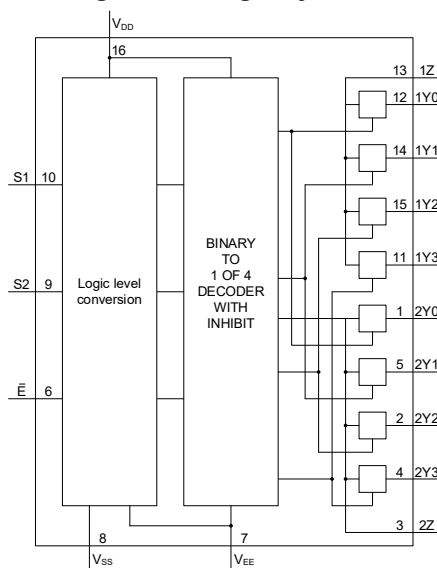


Figure 8-3 Functional diagram

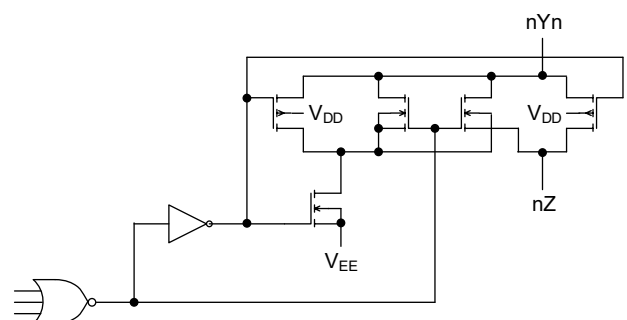


Figure 8-4 Schematic diagram (one switch)

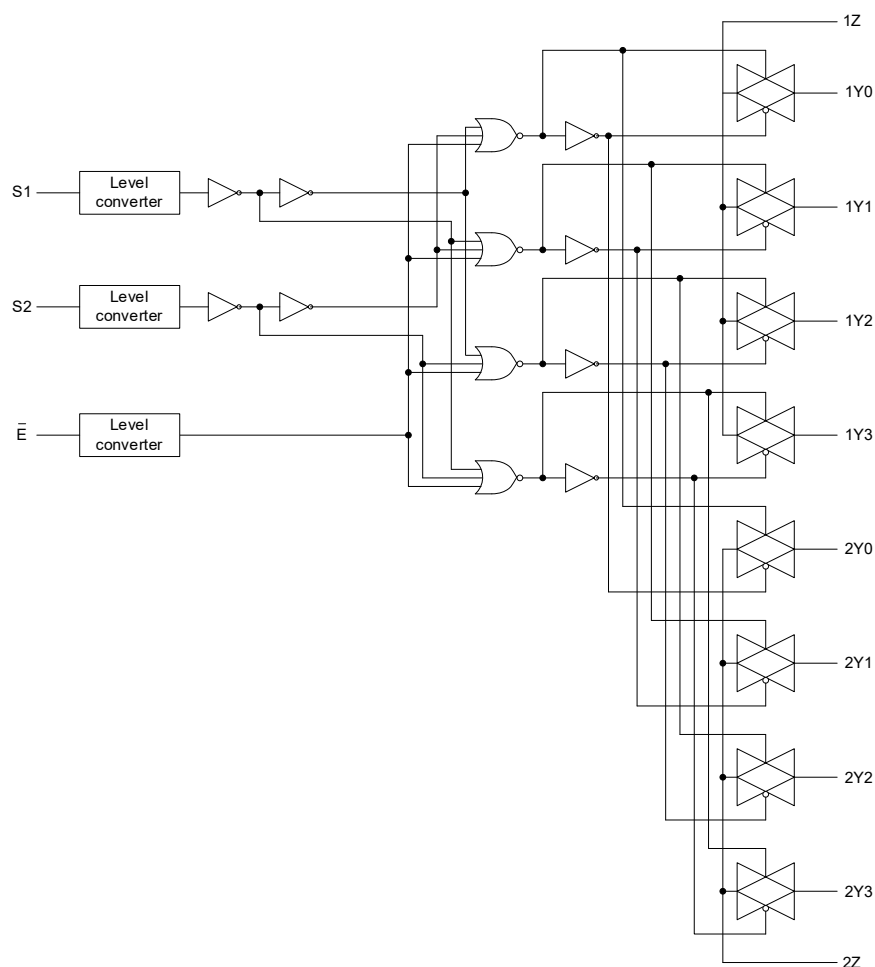


Figure 8-5 Logic diagram

8.3 Function Table⁽¹⁾

INPUT			CHANNEL ON
$\bar{E}$	S2	S1	
L	L	L	nY0 to nZ
L	L	H	nY1 to nZ
L	H	L	nY2 to nZ
L	H	H	nY3 to nZ
H	X	X	Switches off

(1) H=HIGH voltage level; L=LOW voltage level; X=don't care.

8.4 Testing Circuit

8.4.1 DC Testing Circuit

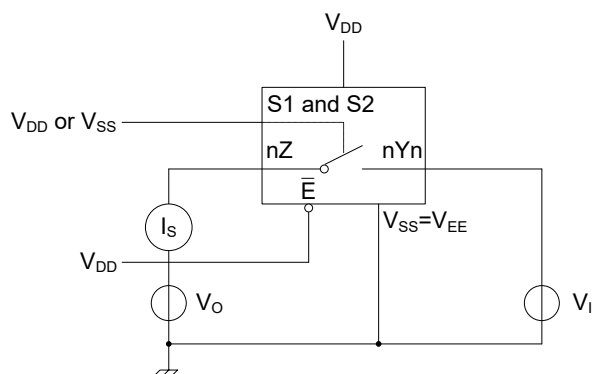


Figure 8-6 Test circuit for measuring OFF-state leakage current Z port

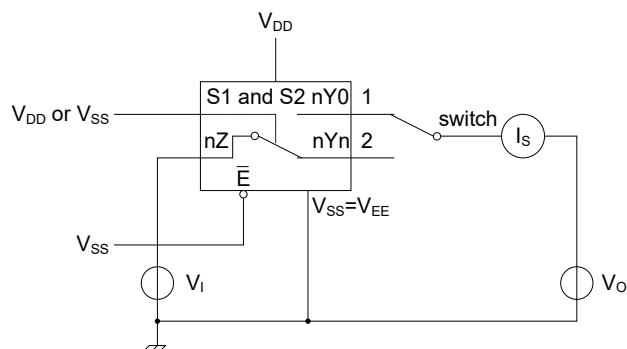


Figure 8-7 Test circuit for measuring OFF-state leakage current nYn port

8.4.2 ON resistance Testing Circuit

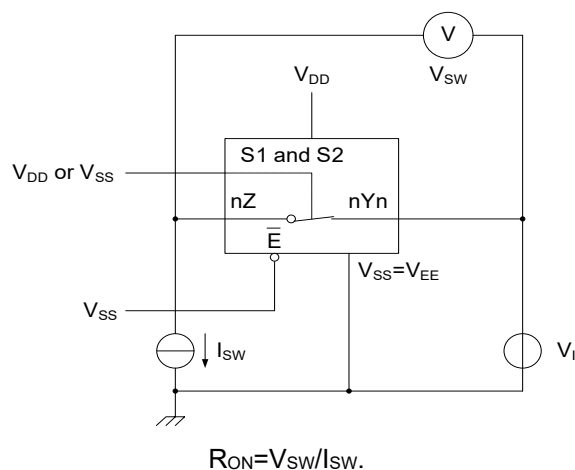


Figure 8-8 Test circuit for measuring R_{ON}

8.4.3 ON resistance Waveforms

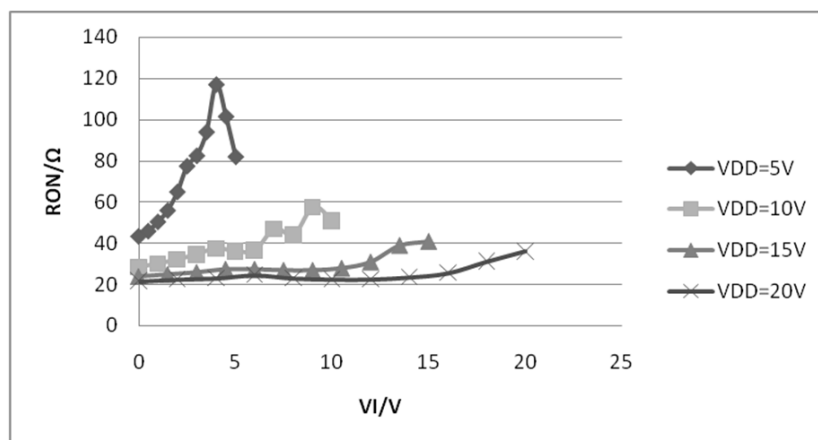


Figure 8-9 Typical R_{ON} as a function of input voltage

8.4.4 AC Testing Circuit 1

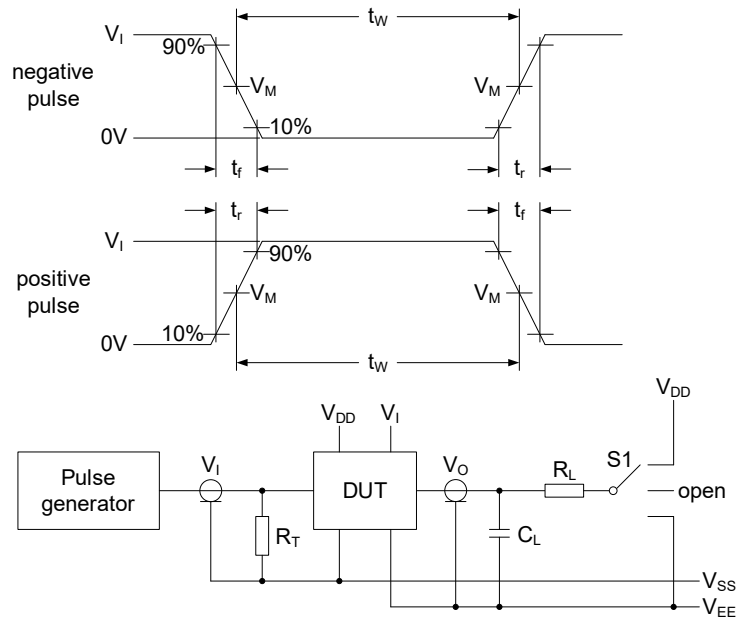


Figure 8-10 Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L =Load resistance.

8.4.5 AC Testing Waveforms

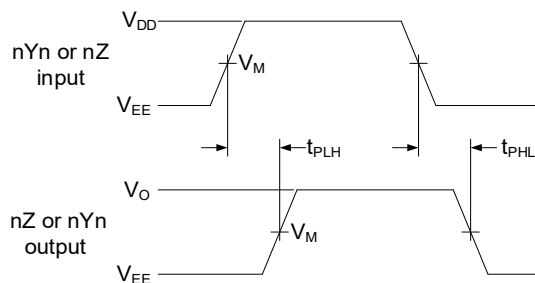


Figure 8-11 nYn, nZ to nZ, nYn propagation delays

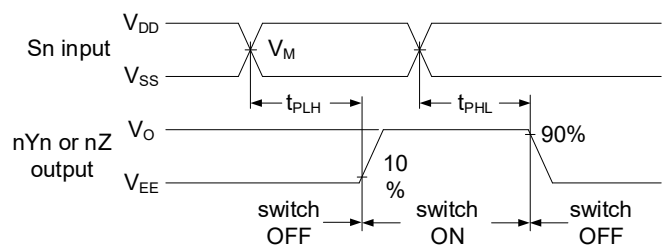


Figure 8-12 S_n to nYn, nZ propagation delays

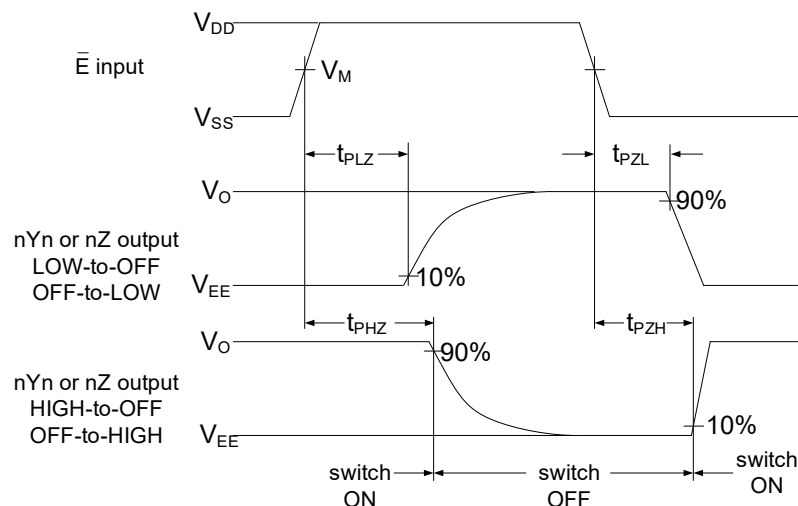


Figure 8-13 Enable and disable times

8.4.6 AC Testing Circuit 2

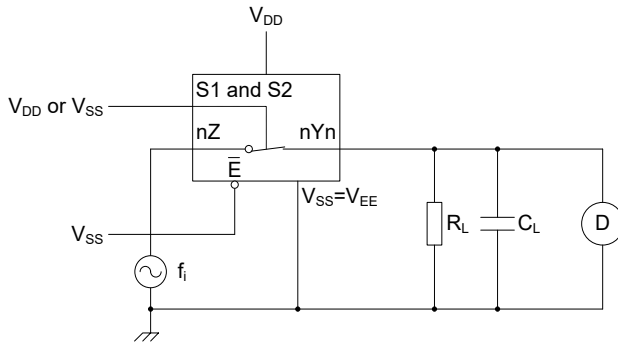


Figure 8-14 Test circuit for measuring total harmonic distortion

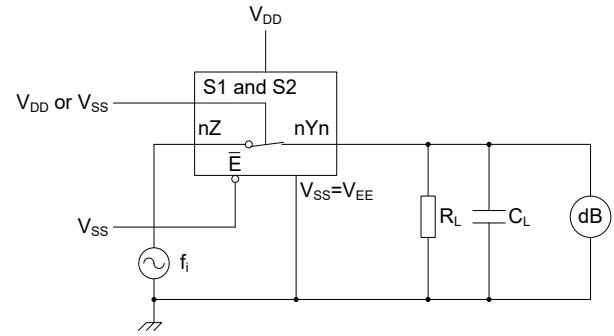


Figure 8-15 Test circuit for measuring frequency response

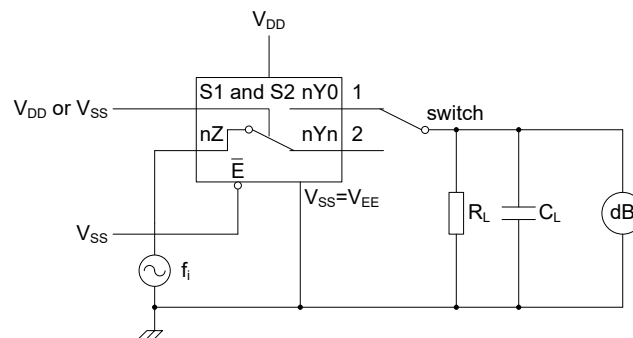
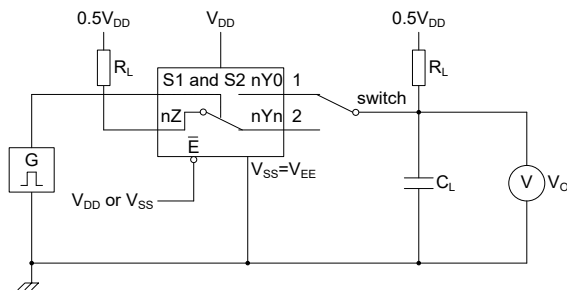
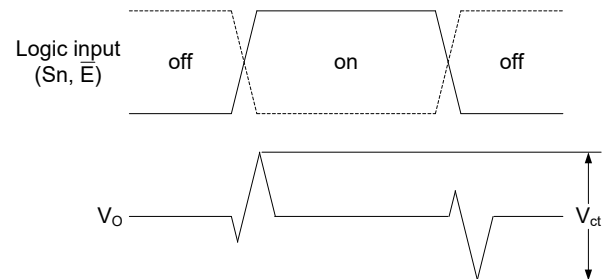


Figure 8-16 Test circuit for measuring isolation (OFF-state)

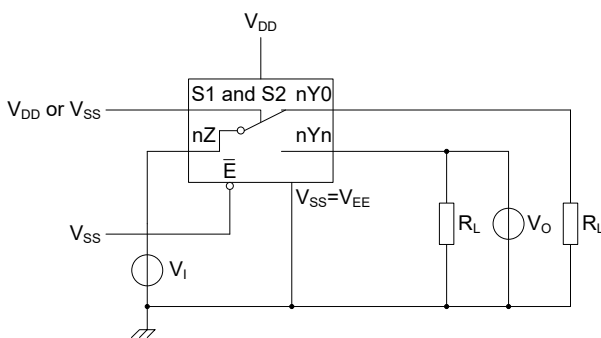


a. Test circuit

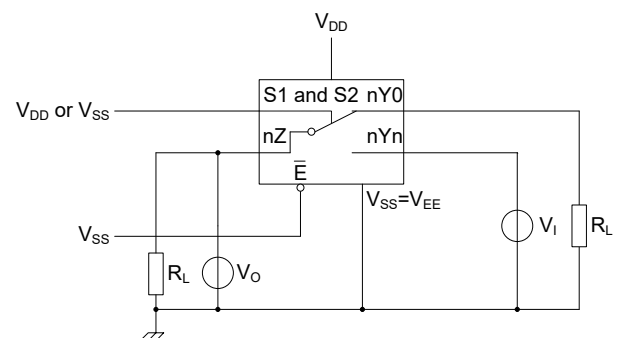


b. Input and output pulse definitions

Figure 17. Test circuit for measuring crosstalk voltage between digital inputs and switch



a. Switch closed condition



b. Switch open condition

Figure 18. Test circuit for measuring crosstalk between switches

8.4.7 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{DD}	V_M	V_M
5V to 18V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

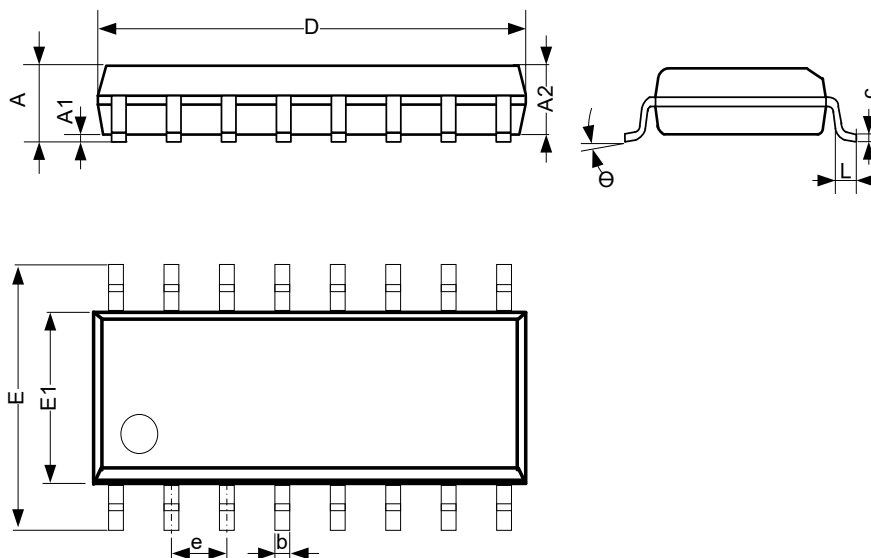
8.4.8 Test Data

INPUT				LOAD		S1 POSITION				
nYn, nZ	Sn and $\bar{E}$	t_r, t_f	V_M	C_L	R_L	t_{PHL}	t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}	Other
V_{DD} or V_{EE}	V_{DD} or V_{SS}	$\leq 20\text{ns}$	$0.5 \times V_{DD}$	50pF	10k Ω	V_{DD} or V_{EE}	V_{EE}	V_{EE}	V_{DD}	V_{EE}

9 Mechanical Information

9.1 SOP16 Mechanical Information

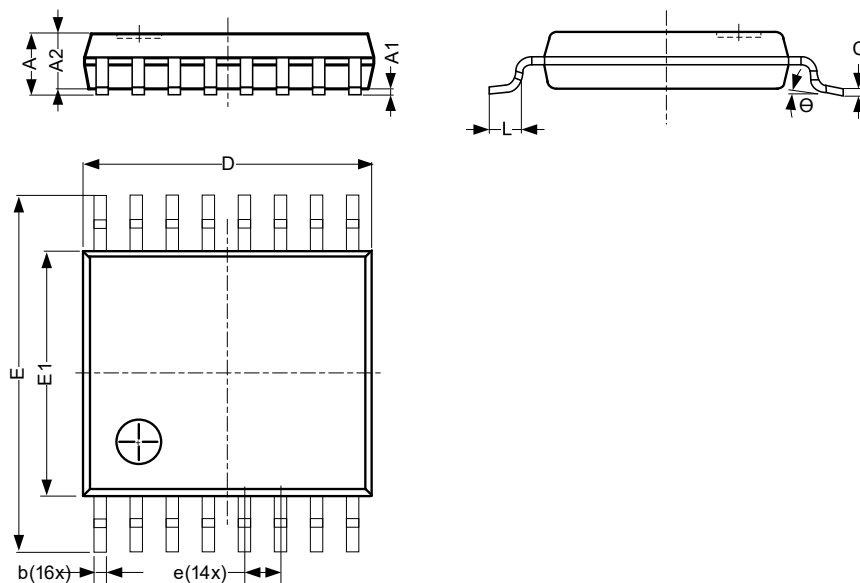
9.1.1 SOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.80
A1	0.10	-	0.25
A2	1.25	-	1.55
b	0.33	-	0.51
c	0.19	-	0.25
D	9.50	-	10.10
E	5.80	-	6.30
E1	3.70	-	4.10
e	1.27 BSC		
L	0.35	-	0.89
θ	0°	-	8°
Unit: mm			

9.2 TSSOP16 Mechanical Information

9.2.1 TSSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- <https://www.jscj-elec.com> for more details.

10.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

June, 2025: rev - 1.1, Correct parameter typo in 8.4.8 Test Data.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

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