Dual Supply Translating Transceiver; 3-State

CJ74LVC/LVCH1T45 Logic

1 Introduction

The CJ74LVC/LVCH1T45 are single bit, dual supply transceivers with 3-state outputs that enable bidirectional level translation. They feature two 1-bit input-output ports (A and B), a direction control input (DIR) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 1.2 V and 5.5 V making the device suitable for translating between any of the low voltage nodes (1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5.0V). Pins A and DIR are referenced to $V_{CC(A)}$ and pin B is referenced to $V_{CC(B)}$. A HIGH on DIR allows transmission from A to B and a LOW on DIR allows transmission from B to A.

The devices are fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both A port and B port are in the high-impedance OFF-state.

Active bus hold circuitry in the CJ74LVCH1T45 holds unused or floating data inputs at a valid logic level.

2 Available Packages

PART NUMBER	PACKAGE
CJ74LVC1T45	SOT-23-6L
	SOT-363
CJ74LVCH1T45	SOT-23-6L
	SOT-363

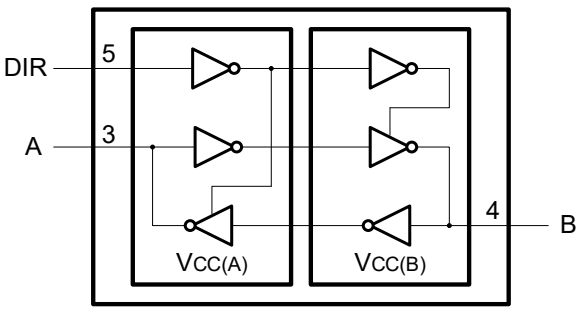
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range:
  - $V_{CC(A)}$: 1.2V to 5.5V
  - $V_{CC(B)}$: 1.2V to 5.5V
- Maximum data rates:
  - 420 Mbps (3.3V to 5.0V translation)
  - 210 Mbps (translate to 3.3V))
  - 140 Mbps (translate to 2.5V)
  - 75 Mbps (translate to 1.8V)
  - 60 Mbps (translate to 1.5V)
- Suspend mode
- ±24mA output drive (V_{CC}=3.0V)
- Inputs accept voltages up to 5.5V
- Low power consumption: 16uA maximum I_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Specified from -40°C to +125°C

4 Applications

- Personal electronic
- Industrial
- Enterprise
- Telecom



Logic symbol

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74LVC1T45M6N	SOT-23-6L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units/Reel	Active
CJ74LVCH1T45M6N	SOT-23-6L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units/Reel	Active
CJ74LVC1T45R6N	SOT-363	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units/Reel	Active
CJ74LVCH1T45R6N	SOT-363	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units/Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

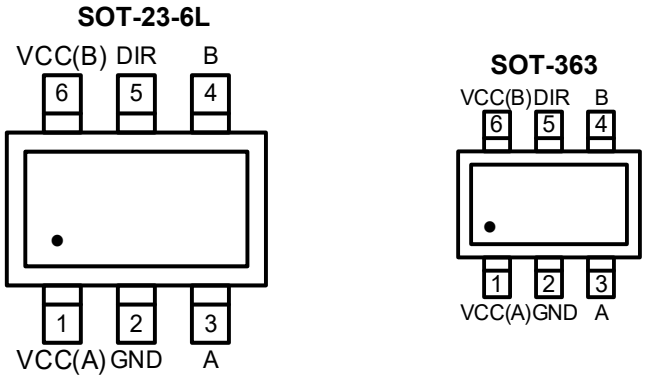


Figure 6-1 Pin configuration

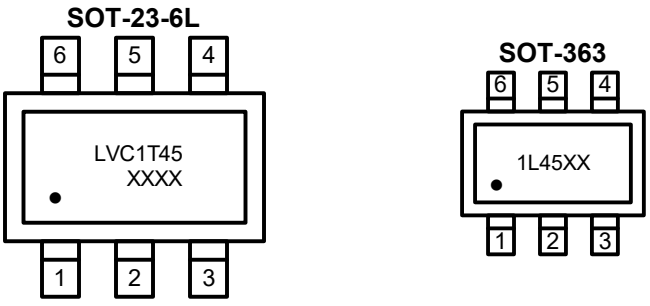
6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	VCC(A)	P	Supply voltage A (port A and DIR)
2	GND	G	Ground (0V)
3	A	I/O	Data input or output
4	B	I/O	Data input or output
5	DIR	-	Direction control
6	VCC(B)	P	Supply voltage B (port B)

(1) I-Input, O-Output, P-Power, G-Ground

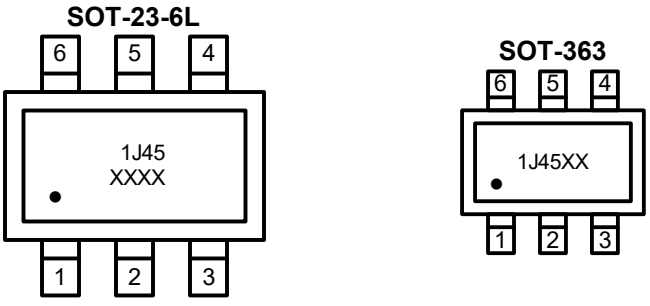
6.3 Marking Information

6.3.1 CJ74LVC1T45



XXXX or XX: Code, indicates weekly record information.

6.3.2 CJ74LVCH1T45



XXXX or XX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND(ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC(A)}$	Supply voltage A	-	-0.5	+6.5	V
$V_{CC(B)}$	Supply voltage B	-	-0.5	+6.5	V
I_{IK}	Input clamping current	V_I<0V	-50	-	mA
V_I	Input voltage	-(1)	-0.5	+6.5	V
I_{OK}	Output clamping current	V_O<0V	-50	-	mA
V_O	Output voltage	Active mode(1) (2) (3)	-0.5	V_{CCO}+0.5	V
		Suspend or 3-state mode(1)	-0.5	+6.5	V
I_O	Output current	V_O=0V to V_{CCO}(2)	-	±50	mA
I_{CC}	Supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
I_{GND}	Ground current	-	-100	-	mA
T_{stg}	Storage temperature	-	-65	+150	°C
P_{tot}	Total power dissipation	-	-	250	mW
T_L	Soldering temperature	10s	-	260	°C

(1) The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

(2) V_{CCO} is the supply voltage associated with the output port.

(3) V_{CCO}+0.5V should not exceed 6.5V.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC(A)}$	Supply voltage A	-	1.2	-	5.5	V
$V_{CC(B)}$	Supply voltage B	-	1.2	-	5.5	V
V_I	Input voltage	-	0	-	5.5	V
V_O	Output voltage	Active mode(1)	0	-	V_{CCO}	V
		Suspend or 3-state mode	0	-	5.5	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C
Δt/ΔV	Input transition rise and fall rate	V_{CCI}=1.2V(2)	-	-	20	ns/V
		V_{CCI}=1.4V to 1.95V	-	-	20	ns/V
		V_{CCI}=2.3V to 2.7V	-	-	20	ns/V
		V_{CCI}=3V to 3.6V	-	-	10	ns/V
		V_{CCI}=4.5V to 5.5V	-	-	5	ns/V

(1) V_{CCO} is the supply voltage associated with the output port.

(2) V_{CCI} is the supply voltage associated with the input port.

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V H1BM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OH}	HIGH-level output voltage	V_I=V_{IH} or V_{IL}; I_O=-3mA; V_{CCO}=1.2V(1)	-	1.09	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IH} or V_{IL}; I_O=3mA; V_{CCO}=1.2V(1)	-	0.07	-	V
I_I	Input leakage current	DIR input; V_I=0V to 5.5V; V_{CCI}=1.2V to 5.5V(2)	-	-	±1	uA
I_{BHL}	Bus hold LOW current	A or B port; V_I=0.42V; V_{CCI}=1.2V(2)	-	19	-	uA
I_{BHH}	Bus hold HIGH current	A or B port; V_I=0.78V; V_{CCI}=1.2V(2)	-	-19	-	uA
I_{BHLO}	Bus hold LOW overdrive current	A or B port; V_{CCI}=1.2V(2)(3)	-	19	-	uA
I_{BHHO}	Bus hold HIGH overdrive current	A or B port; V_{CCI}=1.2V(2)(3)	-	-19	-	uA
I_{OZ}	OFF-state output current	A or B port; V_O=0V or V_{CCO}; V_{CCO}=1.2V to 5.5V(1)	-	-	±1	uA
I_{OFF}	Power-off leakage current	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V	-	-	±1	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V	-	-	±1	uA
C_I	Input capacitance	DIR input; V_I=0V or 3.3V; $V_{CC(A)}$=$V_{CC(B)}$=3.3V	-	2.2	-	pF
$C_{I/O}$	Input/output capacitance	A and B port; suspend mode; V_O=3.3V or 0V; $V_{CC(A)}$=$V_{CC(B)}$=3.3V	-	6.0	-	pF

(1) V_{CCO} is the supply voltage associated with the output port.

(2) V_{CCI} is the supply voltage associated with the data input port.

(3) To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	Data input(1)	V_{CCI}=1.2V	0.8V_{CCI}	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65V_{CCI}	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7V_{CCI}	-	-	V
		DIR input	V_{CCI}=1.2V	0.8$V_{CC(A)}$	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65$V_{CC(A)}$	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7$V_{CC(A)}$	-	-	V
V_{IL}	LOW-level input voltage	Data input(1)	V_{CCI}=1.2V	-	-	0.2V_{CCI}	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35V_{CCI}	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3V_{CCI}	V
		DIR input	V_{CCI}=1.2V	-	-	0.2$V_{CC(A)}$	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35$V_{CC(A)}$	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3$V_{CC(A)}$	V
V_{OH}	HIGH-level output voltage	V_I=V_{IH}	I_O=-100uA; V_{CCO}=1.2V to 4.5V(2)	V_{CCO}-0.1	-	-	V
			I_O=-6mA;V_{CCO}=1.4V	1.0	-	-	V
			I_O=-8mA;V_{CCO}=1.65V	1.2	-	-	V
			I_O=-12mA;V_{CCO}=2.3V	1.9	-	-	V
			I_O=-24mA;V_{CCO}=3.0V	2.4	-	-	V
			I_O=-32mA;V_{CCO}=4.5V	3.8	-	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IH}(2)	I_O=100uA; V_{CCO}=1.2V to 4.5V	-	-	0.1	V
			I_O=6mA; V_{CCO}=1.4V	-	-	0.3	V
			I_O=8mA; V_{CCO}=1.65V	-	-	0.45	V
			I_O=12mA; V_{CCO}=2.3V	-	-	0.3	V
			I_O=24mA; V_{CCO}=3.0V	-	-	0.55	V
			I_O=32mA; V_{CCO}=4.5V	-	-	0.55	V
I_I	Input leakage current	DIR input; V_I=0V to 5.5V; V_{CCI}=1.2V to 5.5V		-	-	±2	uA
I_{BHL}	Bus hold LOW	A or B	V_I=0.49V; V_{CCI}=1.4V	15	-	-	uA

	current	port(1)	V_I=0.58V;V_{CCI}=1.65V	25	-	-	uA
			V_I=0.70V; V_{CCI}=2.3V	45	-	-	uA
			V_I=0.80V; V_{CCI}=3.0V	100	-	-	uA
			V_I=1.35V; V_{CCI}=4.5V	100	-	-	uA
I_{BHH}	Bus hold HIGH current	A or B port(1)	V_I=0.91V; V_{CCI}=1.4V	-15	-	-	uA
			V_I=1.07V;V_{CCI}=1.65V	-25	-	-	uA
			V_I=1.60V; V_{CCI}=2.3V	-45	-	-	uA
			V_I=2.00V; V_{CCI}=3.0V	-100	-	-	uA
			V_I=3.15V; V_{CCI}=4.5V	-100	-	-	uA
I_{BHLO}	Bus hold LOW overdrive current	A or B port(1) (3)	V_{CCI}=1.6V	125	-	-	uA
			V_{CCI}=1.95V	200	-	-	uA
			V_{CCI}=2.7V	300	-	-	uA
			V_{CCI}=3.6V	500	-	-	uA
			V_{CCI}=5.5V	900	-	-	uA
I_{BHHO}	Bus hold HIGH overdrive current	A or B port(1) (3)	V_{CCI}=1.6V	-125	-	-	uA
			V_{CCI}=1.95V	-200	-	-	uA
			V_{CCI}=2.7V	-300	-	-	uA
			V_{CCI}=3.6V	-500	-	-	uA
			V_{CCI}=5.5V	-900	-	-	uA
I_{OZ}	OFF-state output current	A or B port; V_O=0V or V_{CCO}; V_{CCO}=1.2V to 5.5V(2)		-	-	±2	uA
I_{OFF}	Power-off leakage current	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V		-	-	±2	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V		-	-	±2	uA
I_{CC}	Supply current	A port; V_I=0V or V_{CCI}; I_O=0A(1)	$V_{CC(A)}$, $V_{CC(B)}$=1.2V to 5.5V	-	-	8	uA
			$V_{CC(A)}$, $V_{CC(B)}$=1.65V to 5.5V	-	-	3	uA
			$V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V	-	-	2	uA
			$V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V	-2	-	-	uA
		B port; V_I=0V or V_{CCI}; I_O=0A	$V_{CC(A)}$, $V_{CC(B)}$=1.2V to 5.5V	-	-	8	uA
			$V_{CC(A)}$, $V_{CC(B)}$=1.65V to 5.5V	-	-	3	uA
			$V_{CC(B)}$=0V; $V_{CC(A)}$=5.5V	-2	-	-	uA
			$V_{CC(B)}$=5.5V; $V_{CC(A)}$=0V	-	-	2	uA
		A plus B port ($I_{CC(A)}$+ $I_{CC(B)}$); I_O=0A; V_I=0V or V_{CCI}	$V_{CC(A)}$, $V_{CC(B)}$=1.2V to 5.5V	-	-	16	uA
			$V_{CC(A)}$, $V_{CC(B)}$=1.65V to 5.5V	-	-	4	uA

ΔI_{CC}	Additional supply current	Per input; $V_{CC(A)}$, $V_{CC(B)}$= 3.0V to 5.5V	A port; A port at $V_{CC(A)}$-0.6V; DIR at $V_{CC(A)}$; B port=open(4)	-	-	50	uA
			DIR input; DIR at $V_{CC(A)}$-0.6V; A port at $V_{CC(A)}$ or GND; B port=open	-	-	50	uA
			B port; B port at $V_{CC(B)}$-0.6V; DIR at GND; A port=open(4)	-	-	50	uA

(1) V_{CCI} is the supply voltage associated with the data input port.

(2) V_{CCO} is the supply voltage associated with the output port

(3) To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

(4) For non bus hold parts only (CJ74LVC1T45).

7.4.3 DC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	Data input(1)	V_{CCI}=1.2V	0.8V_{CCI}	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65V_{CCI}	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7V_{CCI}	-	-	V
		DIR input	V_{CCI}=1.2V	0.8$V_{CC(A)}$	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65$V_{CC(A)}$	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7$V_{CC(A)}$	-	-	V
V_{IL}	LOW-level input voltage	Data input(1)	V_{CCI}=1.2V	-	-	0.2V_{CCI}	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35V_{CCI}	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3V_{CCI}	V
		DIR input	V_{CCI}=1.2V	-	-	0.2$V_{CC(A)}$	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35$V_{CC(A)}$	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3$V_{CC(A)}$	V
V_{OH}	HIGH-level output voltage	V_I=V_{IH}	I_O=-100uA; V_{CCO}=1.2V to 4.5V(2)	V_{CCO}-0.1	-	-	V

			I_O=-6mA;V_{CCO}=1.4V	1.0	-	-	V
			I_O=-8mA;V_{CCO}=1.65V	1.2	-	-	V
			I_O=-12mA;V_{CCO}=2.3V	1.9	-	-	V
			I_O=-24mA;V_{CCO}=3.0V	2.4	-	-	V
			I_O=-32mA;V_{CCO}=4.5V	3.8	-	-	V
V_{OL}	LOW-level output voltage	V_I=V_{IH}(2)	I_O=100uA; V_{CCO}=1.2V to 4.5V	-	-	0.1	V
			I_O=6mA; V_{CCO}=1.4V	-	-	0.3	V
			I_O=8mA; V_{CCO}=1.65V	-	-	0.45	V
			I_O=12mA; V_{CCO}=2.3V	-	-	0.3	V
			I_O=24mA; V_{CCO}=3.0V	-	-	0.55	V
			I_O=32mA; V_{CCO}=4.5V	-	-	0.55	V
I_I	Input leakage current	DIR input; V_I=0V to 5.5V; V_{CCI}=1.2V to 5.5V		-	-	±2	uA
I_{BHL}	Bus hold LOW current	A or B port(1)	V_I=0.49V; V_{CCI}=1.4V	10	-	-	uA
			V_I=0.58V;V_{CCI}=1.65V	20	-	-	uA
			V_I=0.70V; V_{CCI}=2.3V	45	-	-	uA
			V_I=0.80V; V_{CCI}=3.0V	80	-	-	uA
			V_I=1.35V; V_{CCI}=4.5V	100	-	-	uA
I_{BHH}	Bus hold HIGH current	A or B port(1)	V_I=0.91V; V_{CCI}=1.4V	-10	-	-	uA
			V_I=1.07V;V_{CCI}=1.65V	-20	-	-	uA
			V_I=1.60V; V_{CCI}=2.3V	-45	-	-	uA
			V_I=2.00V; V_{CCI}=3.0V	-80	-	-	uA
			V_I=3.15V; V_{CCI}=4.5V	-100	-	-	uA
I_{BHLO}	Bus hold LOW overdrive current	A or B port(1) (3)	V_{CCI}=1.6V	125	-	-	uA
			V_{CCI}=1.95V	200	-	-	uA
			V_{CCI}=2.7V	300	-	-	uA
			V_{CCI}=3.6V	500	-	-	uA
			V_{CCI}=5.5V	900	-	-	uA
I_{BHHO}	Bus hold HIGH overdrive current	A or B port(1) (3)	V_{CCI}=1.6V	-125	-	-	uA
			V_{CCI}=1.95V	-200	-	-	uA
			V_{CCI}=2.7V	-300	-	-	uA
			V_{CCI}=3.6V	-500	-	-	uA
			V_{CCI}=5.5V	-900	-	-	uA
I_{OZ}	OFF-state output current	A or B port; V_O=0V or V_{CCO}; V_{CCO}=1.2V to 5.5V(2)		-	-	±10	uA
I_{OFF}	Power-off leakage current	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V		-	-	±10	uA
		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V		-	-	±10	uA
I_{CC}	Supply current	A port; V_I=0V or	$V_{CC(A)}$, $V_{CC(B)}$=1.2V to 5.5V	-	-	8	uA

		V_{CCI}; I_O=0A(1)	$V_{CC(A)}$, $V_{CC(B)}$=1.65V to 5.5V	-	-	3	uA
			$V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V	-	-	2	uA
			$V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V	-2	-	-	uA
		B port; V_I=0V or V_{CCI}; I_O=0A	$V_{CC(A)}$, $V_{CC(B)}$=1.2V to 5.5V	-	-	8	uA
			$V_{CC(A)}$, $V_{CC(B)}$=1.65V to 5.5V	-	-	3	uA
			$V_{CC(B)}$=0V; $V_{CC(A)}$=5.5V	-2	-	-	uA
			$V_{CC(B)}$=5.5V; $V_{CC(A)}$=0V	-	-	2	uA
		A plus B port ($I_{CC(A)}$+ $I_{CC(B)}$); I_O=0A; V_I=0V or V_{CCI}	$V_{CC(A)}$, $V_{CC(B)}$=1.2V to 5.5V		-	16	uA
			$V_{CC(A)}$, $V_{CC(B)}$=1.65V to 5.5V	-	-	4	uA
ΔI_{CC}	Additional supply current	Per input; $V_{CC(A)}$, $V_{CC(B)}$= 3.0V to 5.5V	A port; A port at $V_{CC(A)}$-0.6V; DIR at $V_{CC(A)}$; B port=open(4)	-	-	75	uA
			DIR input; DIR at $V_{CC(A)}$-0.6V; A port at $V_{CC(A)}$ or GND; B port=open	-	-	75	uA
			B port; B port at $V_{CC(B)}$-0.6V; DIR at GND; A port=open(4)	-	-	75	uA

(1) V_{CCI} is the supply voltage associated with the data input port.

(2) V_{CCO} is the supply voltage associated with the output port

(3) To guarantee the node switches, an external driver must source/sink at least I_{BHLO}/I_{BHHO} when the input is in the range V_{IL} to V_{IH}.

(4) For non bus hold parts only (CJ74LVC1T45).

7.4.4 AC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	$V_{CC(B)}$										UNIT
			1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$V_{CC(A)}$=1.4V to 1.6V													
t_{PLH}	LOW to HIGH propagation delay	A to B	-	22.0	-	18.2	-	13.7	-	12.0	-	10.7	ns
		B to A	-	22.0	-	19.5	-	16.2	-	15.9	-	15.5	ns
t_{PHL}	HIGH to LOW propagation delay	A to B	-	19.7	-	15.6	-	12.1	-	11.1	-	10.8	ns
		B to A	-	19.7	-	17.6	-	13.5	-	11.5	-	11.2	ns
t_{PHZ}	HIGH to OFF-state propagation delay	DIR to A	-	19.2	-	19.2	-	19.2	-	19.2	-	19.2	ns
		DIR to B	-	25.0	-	23.8	-	14.1	-	13.2	-	12.5	ns
t_{PLZ}	LOW to OFF-state propagation delay	DIR to A	-	11.7	-	11.7	-	11.7	-	11.7	-	11.7	ns
		DIR to B	-	18.5	-	17.5	-	13.2	-	12.4	-	11.6	ns
t_{PZH}	OFF-state to HIGH propagation delay	DIR to A[(1)]	-	39.7	-	36.7	-	24.8	-	23.0	-	21.8	ns
		DIR to B[(1)]	-	33.0	-	29.5	-	25.3	-	23.3	-	22.3	ns
t_{PZL}	OFF-state to LOW propagation delay	DIR to A[(1)]	-	44.5	-	41.2	-	24.6	-	22.9	-	21.6	ns
		DIR to B[(1)]	-	38.3	-	34.7	-	31.1	-	30.2	-	29.8	ns
$V_{CC(A)}$=1.65V to 1.95V													
t_{PLH}	LOW to HIGH propagation delay	A to B	-	19.5	-	18.1	-	9.7	-	7.7	-	7.2	ns
		B to A	-	18.3	-	18.1	-	15.2	-	12.6	-	12.2	ns
t_{PHL}	HIGH to LOW propagation delay	A to B	-	17.4	-	14.4	-	9.0	-	7.5	-	7.3	ns
		B to A	-	15.6	-	14.4	-	13.2	-	12.9	-	12.5	ns
t_{PHZ}	HIGH to OFF-state propagation delay	DIR to A	-	17.5	-	17.5	-	17.5	-	17.5	-	17.5	ns
		DIR to B	-	24.5	-	22.3	-	12.8	-	12.0	-	10.5	ns
t_{PLZ}	LOW to OFF-state propagation delay	DIR to A	-	11.1	-	11.1	-	11.1	-	11.1	-	11.1	ns
		DIR to B	-	18.4	-	16.9	-	11.3	-	10.5	-	9.5	ns
t_{PZH}	OFF-state to HIGH propagation delay	DIR to A[(1)]	-	35.6	-	33.9	-	25.6	-	24.4	-	22.3	ns
		DIR to B[(1)]	-	30.0	-	28.5	-	20.3	-	18.1	-	17.5	ns
t_{PZL}	OFF-state to LOW propagation delay	DIR to A[(1)]	-	39.8	-	36.5	-	24.8	-	23.3	-	20.6	ns
		DIR to B[(1)]	-	35.0	-	31.9	-	26.0	-	24.6	-	24.5	ns
$V_{CC(A)}$=2.3V to 2.7V													
t_{PLH}	LOW to HIGH	A to B	-	18.1	-	16.1	-	8.7	-	6.5	-	5.0	ns

	propagation delay	B to A	-	13.7	-	9.2	-	8.7	-	7.8	-	7.5	ns
t_{PHL}	HIGH to LOW propagation delay	A to B	-	15.9	-	13.2	-	7.6	-	5.9	-	4.9	ns
		B to A	-	12.3	-	8.7	-	7.6	-	7.0	-	6.2	ns
t_{PHZ}	HIGH to OFF-state propagation delay	DIR to A	-	8.2	-	8.2	-	8.2	-	8.2	-	8.2	ns
		DIR to B	-	22.5	-	21.6	-	11.2	-	9.2	-	8.3	ns
t_{PLZ}	LOW to OFF-state propagation delay	DIR to A	-	6.2	-	6.2	-	6.2	-	6.2	-	6.2	ns
		DIR to B	-	14.6	-	13.3	-	9.2	-	8.7	-	7.7	ns
t_{PZH}	OFF-state to HIGH propagation delay	DIR to A[(1)]	-	27.7	-	22.3	-	17.2	-	16.5	-	12.6	ns
		DIR to B[(1)]	-	23.5	-	21.5	-	14.1	-	11.9	-	10.5	ns
t_{PZL}	OFF-state to LOW propagation delay	DIR to A[(1)]	-	34.1	-	29.5	-	18.3	-	16.2	-	13.0	ns
		DIR to B[(1)]	-	23.7	-	20.9	-	15.5	-	13.5	-	12.5	ns
$V_{CC(A)}$=3.0V to 3.6V													
t_{PLH}	LOW to HIGH propagation delay	A to B	-	17.2	-	15.5	-	7.9	-	5.6	-	4.5	ns
		B to A	-	11.7	-	7.3	-	6.4	-	5.6	-	5.5	ns
t_{PHL}	HIGH to LOW propagation delay	A to B	-	15.5	-	12.5	-	7.0	-	5.0	-	4.4	ns
		B to A	-	11.0	-	7.2	-	5.6	-	5.0	-	4.5	ns
t_{PHZ}	HIGH to OFF-state propagation delay	DIR to A	-	7.3	-	7.3	-	7.3	-	7.3	-	7.3	ns
		DIR to B	-	18.1	-	16.6	-	10.4	-	8.7	-	6.8	ns
t_{PLZ}	LOW to OFF-state propagation delay	DIR to A	-	5.8	-	5.8	-	5.8	-	5.8	-	5.8	ns
		DIR to B	-	13.8	-	12.7	-	8.0	-	7.4	-	6.8	ns
t_{PZH}	OFF-state to HIGH propagation delay	DIR to A[(1)]	-	25.0	-	19.4	-	13.8	-	12.6	-	10.0	ns
		DIR to B[(1)]	-	22.5	-	20.7	-	13.3	-	10.9	-	9.8	ns
t_{PZL}	OFF-state to LOW propagation delay	DIR to A[(1)]	-	28.5	-	23.3	-	15.3	-	13.3	-	10.5	ns
		DIR to B[(1)]	-	22.7	-	19.7	-	14.1	-	12.1	-	11.1	ns
$V_{CC(A)}$=4.5V to 5.5V													
t_{PLH}	LOW to HIGH propagation delay	A to B	-	16.5	-	15.0	-	7.7	-	5.6	-	3.9	ns
		B to A	-	10.4	-	6.6	-	5.0	-	4.5	-	3.9	ns
t_{PHL}	HIGH to LOW propagation delay	A to B	-	15.0	-	12.1	-	6.3	-	4.5	-	3.6	ns
		B to A	-	10.4	-	6.5	-	4.6	-	4.0	-	3.6	ns
t_{PHZ}	HIGH to OFF-state propagation delay	DIR to A	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	ns
		DIR to B	-	16.9	-	15.9	-	9.5	-	8.0	-	6.5	ns

t_{PLZ}	LOW to OFF-state propagation delay	DIR to A	-	5.3	-	5.3	-	5.3	-	5.3	-	5.3	ns
		DIR to B	-	13.0	-	11.8	-	7.5	-	7.1	-	6.5	ns
t_{PZH}	OFF-state to HIGH propagation delay	DIR to A(1)	-	23.5	-	18.7	-	12.0	-	10.9	-	8.3	ns
		DIR to B(1)	-	20.0	-	18.6	-	11.0	-	9.1	-	7.4	ns
t_{PZL}	OFF-state to LOW propagation delay	DIR to A(1)	-	27.7	-	23.3	-	14.1	-	11.6	-	9.3	ns
		DIR to B(1)	-	20.5	-	17.7	-	11.3	-	9.6	-	8.9	ns

(1) t_{PZH} and t_{PZL} are calculated values using the formula shown in Section 6.4.

7.4.5 AC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	$V_{CC(B)}$										UNIT
			1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$V_{CC(A)}$=1.4V to 1.6V													
t_{PLH}	LOW to HIGH propagation delay	A to B	-	24.2	-	20.0	-	15.1	-	13.2	-	11.8	ns
		B to A	-	24.2	-	21.4	-	17.8	-	17.5	-	17.1	ns
t_{PHL}	HIGH to LOW propagation delay	A to B	-	21.7	-	17.2	-	13.3	-	12.2	-	11.9	ns
		B to A	-	21.7	-	19.4	-	14.9	-	12.7	-	12.3	ns
t_{PHZ}	HIGH to OFF-state propagation delay	DIR to A	-	21.1	-	21.1	-	21.1	-	21.1	-	21.1	ns
		DIR to B	-	27.5	-	26.2	-	15.5	-	14.5	-	13.8	ns
t_{PLZ}	LOW to OFF-state propagation delay	DIR to A	-	12.9	-	12.9	-	12.9	-	12.9	-	12.9	ns
		DIR to B	-	20.4	-	19.3	-	14.5	-	13.6	-	12.8	ns
t_{PZH}	OFF-state to HIGH propagation delay	DIR to A(1)	-	43.7	-	40.4	-	27.3	-	25.3	-	24.0	ns
		DIR to B(1)	-	36.3	-	32.4	-	27.8	-	25.6	-	24.5	ns
t_{PZL}	OFF-state to LOW propagation delay	DIR to A(1)	-	48.9	-	45.3	-	27.1	-	25.2	-	23.8	ns
		DIR to B(1)	-	42.1	-	38.2	-	34.2	-	33.2	-	32.8	ns
$V_{CC(A)}$=1.65V to 1.95V													
t_{PLH}	LOW to HIGH propagation delay	A to B	-	21.4	-	19.9	-	10.7	-	8.5	-	7.9	ns
		B to A	-	20.1	-	19.9	-	16.7	-	13.9	-	13.4	ns
t_{PHL}	HIGH to LOW propagation delay	A to B	-	19.1	-	15.8	-	9.9	-	8.3	-	8.0	ns
		B to A	-	17.2	-	15.8	-	14.5	-	14.2	-	13.7	ns
t_{PHZ}	HIGH to OFF-state propagation delay	DIR to A	-	19.2	-	19.2	-	19.2	-	19.2	-	19.2	ns
		DIR to B	-	26.9	-	24.5	-	14.1	-	13.2	-	11.5	ns

t_{PLZ}	LOW to OFF-state propagation delay	DIR to A	-	12.2	-	12.2	-	12.2	-	12.2	-	12.2	ns
		DIR to B	-	20.2	-	18.6	-	12.4	-	11.5	-	10.4	ns
t_{PZH}	OFF-state to HIGH propagation delay	DIR to A(1)	-	39.2	-	37.3	-	28.2	-	26.8	-	24.5	ns
		DIR to B(1)	-	33.0	-	31.4	-	22.3	-	19.9	-	19.3	ns
t_{PZL}	OFF-state to LOW propagation delay	DIR to A(1)	-	43.8	-	40.2	-	27.3	-	25.6	-	22.7	ns
		DIR to B(1)	-	38.5	-	35.1	-	28.6	-	27.1	-	26.9	ns
$V_{CC(A)}$=2.3V to 2.7V													
t_{PLH}	LOW to HIGH propagation delay	A to B	-	19.9	-	17.7	-	9.6	-	7.1	-	5.5	ns
		B to A	-	15.1	-	10.1	-	9.6	-	8.6	-	8.3	ns
t_{PHL}	HIGH to LOW propagation delay	A to B	-	17.5	-	14.5	-	8.4	-	6.5	-	5.4	ns
		B to A	-	13.5	-	9.6	-	8.4	-	7.7	-	6.8	ns
t_{PHZ}	HIGH to OFF-state propagation delay	DIR to A	-	9.0	-	9.0	-	9.0	-	9.0	-	9.0	ns
		DIR to B	-	24.8	-	23.8	-	12.3	-	10.1	-	9.1	ns
t_{PLZ}	LOW to OFF-state propagation delay	DIR to A	-	6.8	-	6.8	-	6.8	-	6.8	-	6.8	ns
		DIR to B	-	16.1	-	14.6	-	10.1	-	9.6	-	8.5	ns
t_{PZH}	OFF-state to HIGH propagation delay	DIR to A(1)	-	30.5	-	24.5	-	18.9	-	18.1	-	13.9	ns
		DIR to B(1)	-	25.8	-	23.7	-	15.5	-	13.1	-	11.5	ns
t_{PZL}	OFF-state to LOW propagation delay	DIR to A(1)	-	37.5	-	32.5	-	20.1	-	17.8	-	14.3	ns
		DIR to B(1)	-	26.1	-	23.0	-	17.0	-	14.8	-	13.8	ns
$V_{CC(A)}$=3.0V to 3.6V													
t_{PLH}	LOW to HIGH propagation delay	A to B	-	18.9	-	17.0	-	8.7	-	6.2	-	4.9	ns
		B to A	-	12.9	-	8.0	-	7.0	-	6.2	-	6.0	ns
t_{PHL}	HIGH to LOW propagation delay	A to B	-	17.1	-	13.8	-	7.7	-	5.5	-	4.8	ns
		B to A	-	12.1	-	7.9	-	6.2	-	5.5	-	5.0	ns
t_{PHZ}	HIGH to OFF-state propagation delay	DIR to A	-	8.0	-	8.0	-	8.0	-	8.0	-	8.0	ns
		DIR to B	-	19.9	-	18.3	-	11.4	-	9.6	-	7.5	ns
t_{PLZ}	LOW to OFF-state propagation delay	DIR to A	-	6.4	-	6.4	-	6.4	-	6.4	-	6.4	ns
		DIR to B	-	15.2	-	14.0	-	8.8	-	8.1	-	7.5	ns
t_{PZH}	OFF-state to HIGH propagation delay	DIR to A(1)	-	27.5	-	21.3	-	15.2	-	13.9	-	11.0	ns
		DIR to B(1)	-	24.8	-	22.8	-	14.6	-	12.0	-	10.8	ns
t_{PZL}	OFF-state to	DIR to A(1)	-	31.3	-	25.6	-	16.8	-	14.6	-	11.6	ns

	LOW propagation delay	DIR to B(1)	-	25.0	-	21.7	-	15.5	-	13.3	-	12.2	ns
$V_{CC(A)}$=4.5V to 5.5V													
t_{PLH}	LOW to HIGH propagation delay	A to B	-	18.1	-	16.5	-	8.5	-	6.2	-	4.3	ns
		B to A	-	11.4	-	7.3	-	5.5	-	5.0	-	4.3	ns
t_{PHL}	HIGH to LOW propagation delay	A to B	-	16.5	-	13.3	-	6.9	-	5.0	-	4.0	ns
		B to A	-	11.4	-	7.1	-	5.1	-	4.4	-	4.0	ns
t_{PHZ}	HIGH to OFF-state propagation delay	DIR to A	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	ns
		DIR to B	-	18.6	-	17.5	-	10.5	-	8.8	-	7.2	ns
t_{PLZ}	LOW to OFF-state propagation delay	DIR to A	-	5.8	-	5.8	-	5.8	-	5.8	-	5.8	ns
		DIR to B	-	14.3	-	13.0	-	8.2	-	7.8	-	7.2	ns
t_{PZH}	OFF-state to HIGH propagation delay	DIR to A(1)	-	25.8	-	20.6	-	13.2	-	12.0	-	9.1	ns
		DIR to B(1)	-	22.0	-	20.5	-	12.1	-	10.0	-	8.1	ns
t_{PZL}	OFF-state to LOW propagation delay	DIR to A(1)	-	30.5	-	25.6	-	15.5	-	12.8	-	10.2	ns
		DIR to B(1)	-	22.5	-	19.5	-	12.4	-	10.6	-	9.8	ns

(1) t_{PZH} and t_{PZL} are calculated values using the formula shown in Section 6.4.

8 Detailed Description

8.1 Overview

The CJ74LVC/LVCH1T45 are single bit, dual supply transceivers with 3-state outputs that enable bidirectional level translation. They feature two 1-bit input-output ports (A and B), a direction control input (DIR) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 1.2 V and 5.5 V making the device suitable for translating between any of the low voltage nodes (1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5.0V). Pins A and DIR are referenced to $V_{CC(A)}$ and pin B is referenced to $V_{CC(B)}$. A HIGH on DIR allows transmission from A to B and a LOW on DIR allows transmission from B to A.

The devices are fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both A port and B port are in the high-impedance OFF-state.

Active bus hold circuitry in the CJ74LVCH1T45 holds unused or floating data inputs at a valid logic level.

8.2 Functional Block Diagram

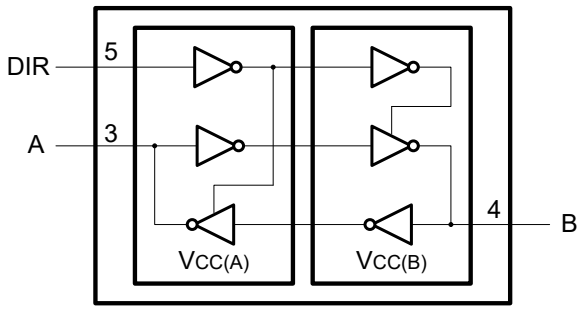


Figure 8-1 Logic symbol

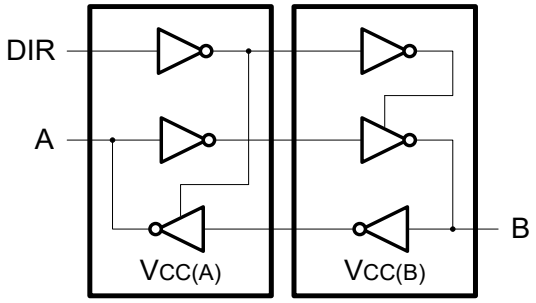


Figure 8-2 Logic diagram

8.3 Function Table

SUPPLY VOLTAGE	INPUT	INPUT/OUTPUT	
$V_{CC(A)}$, $V_{CC(B)}$	DIR	A	B
1.2V to 5.5V	L	A=B	Input
1.2V to 5.5V	H	Input	B=A
GND	X	Z	Z

Note:

(1) H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.

(2) The input circuit of the data I/O is always active.

(3) When either $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

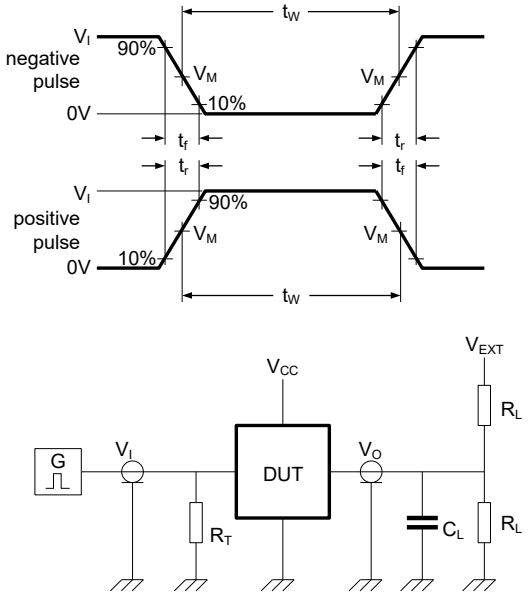


Figure 8-3 Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance.

V_{EXT}=External voltage for measuring switching times.

8.4.2 AC Testing Waveforms

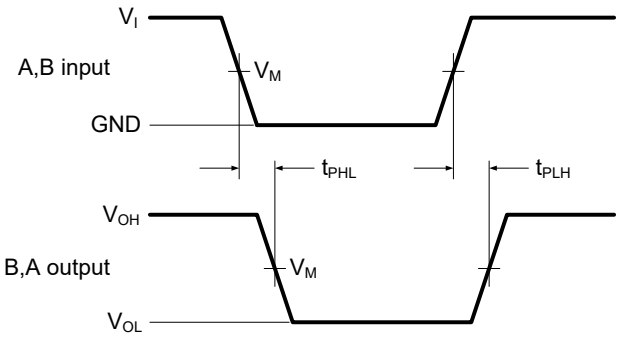


Figure 8-4 The data input (A, B) to output (B, A) propagation delay times
(V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.)

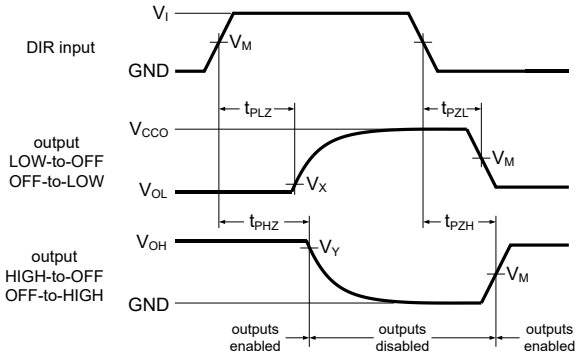


Figure 8-5 Enable and disable times
(V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.)

8.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT(1)	OUTPUT(2)		
$V_{CC(A)}$, $V_{CC(B)}$	V_M	V_M	V_X	V_Y
1.2V to 1.6V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.1V	V_{OH}-0.1V
1.65V to 2.7V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.15V	V_{OH}-0.15V
3.0V to 5.5V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.3V	V_{OH}-0.3V

(1) V_{CCI} is the supply voltage associated with the data input port.

(2) V_{CCO} is the supply voltage associated with the output port.

8.4.4 Test Data

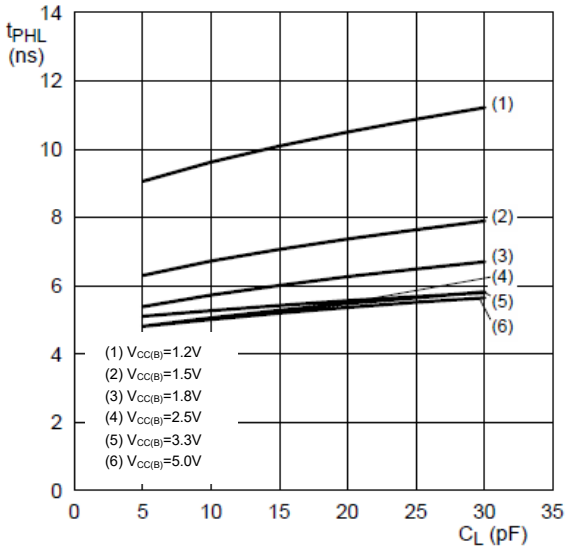
SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}		
$V_{CC(A)}$, $V_{CC(B)}$	V_I(1)	$\Delta t/\Delta V$(2)	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}(3)
1.2V to 5.5V	V_{CCI}	≤1.0ns/V	15pF	2kΩ	Open	GND	$2V_{CCO}$

(1) V_{CCI} is the supply voltage associated with the data input port.

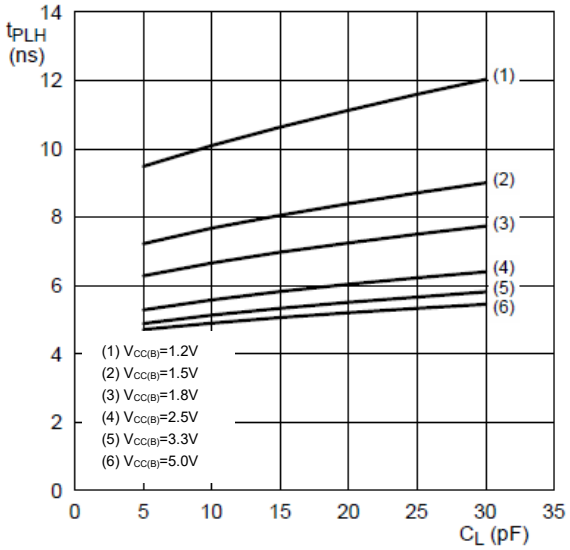
(2) dV/dt≥1.0V/ns.

(3) V_{CCO} is the supply voltage associated with the output port.

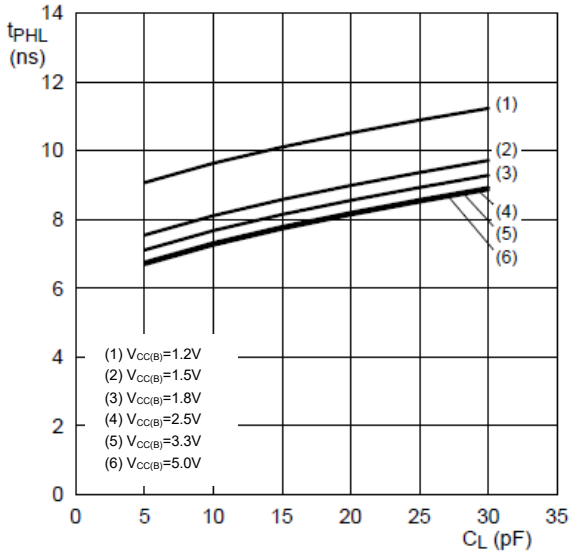
9 Characteristic Curve



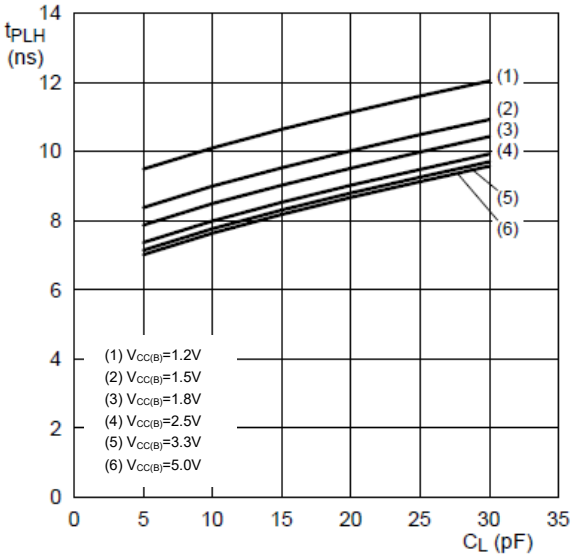
a. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$=1.2V



b. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$=1.2V

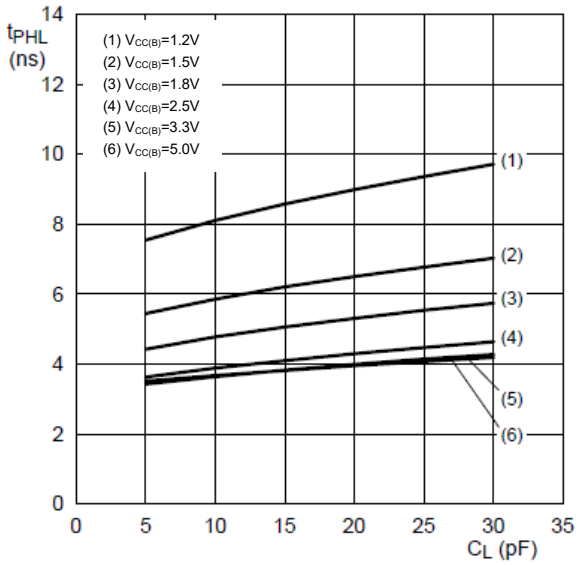


c. HIGH to LOW propagation delay (B to A); $V_{CC(A)}$=1.2V

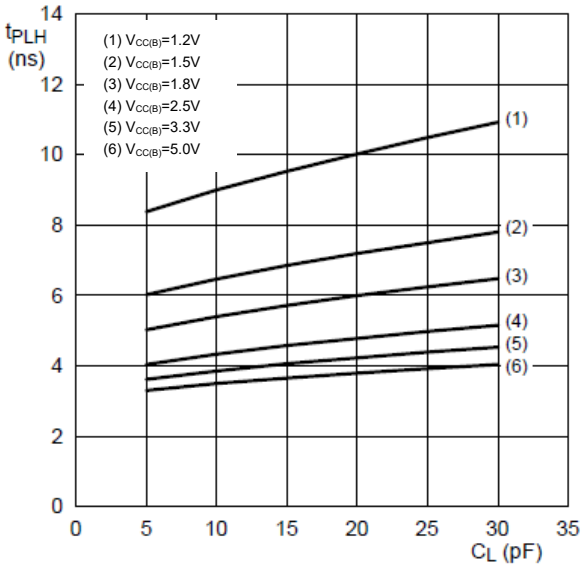


d. LOW to HIGH propagation delay (B to A); $V_{CC(A)}$=1.2V

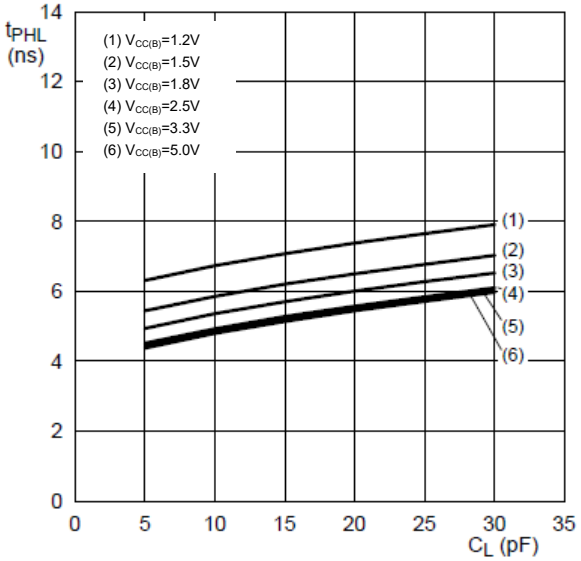
Figure 9-1 Typical propagation delay versus load capacitance; T_{amb}=25°C



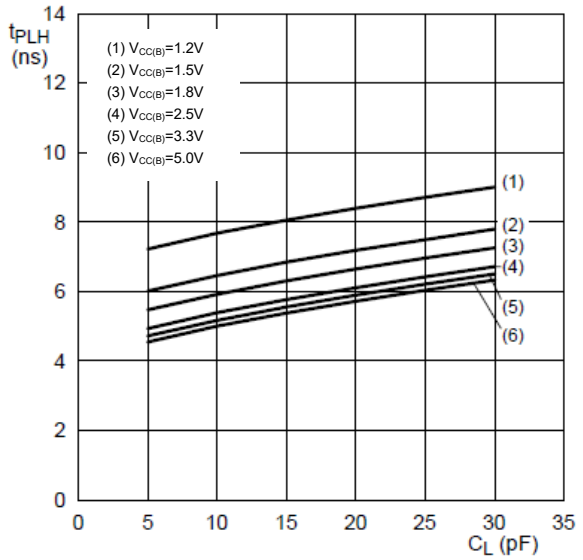
a. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$=1.5V



b. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$=1.5V

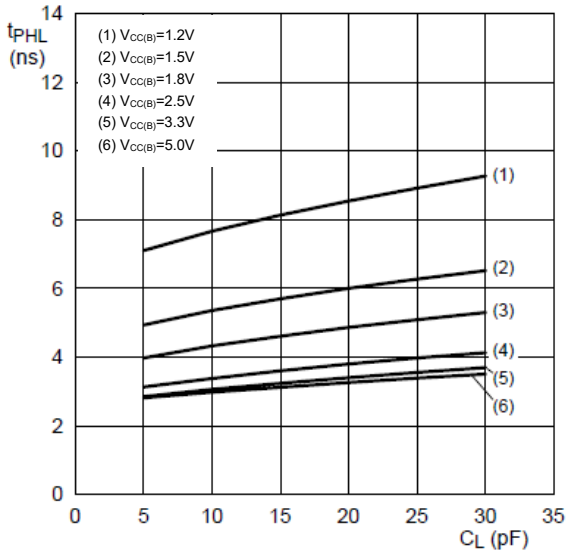


c. HIGH to LOW propagation delay (B to A); $V_{CC(A)}$=1.5V

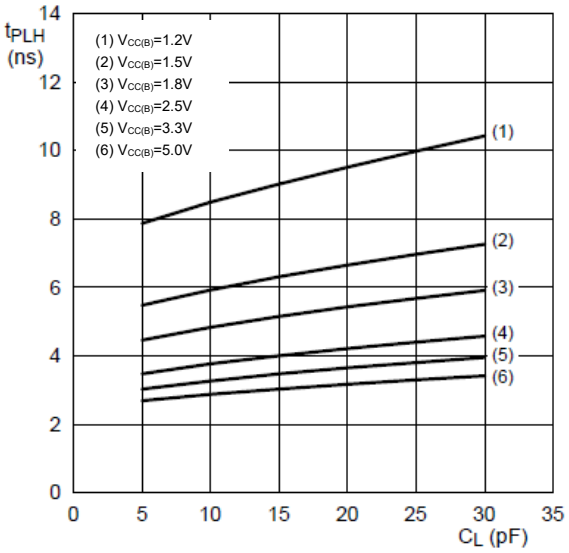


d. LOW to HIGH propagation delay (B to A); $V_{CC(A)}$=1.5V

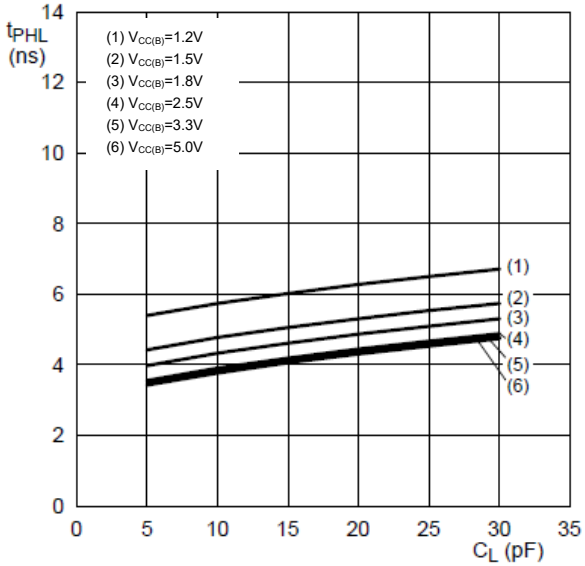
Figure 9-2 Typical propagation delay versus load capacitance; T_{amb}=25°C



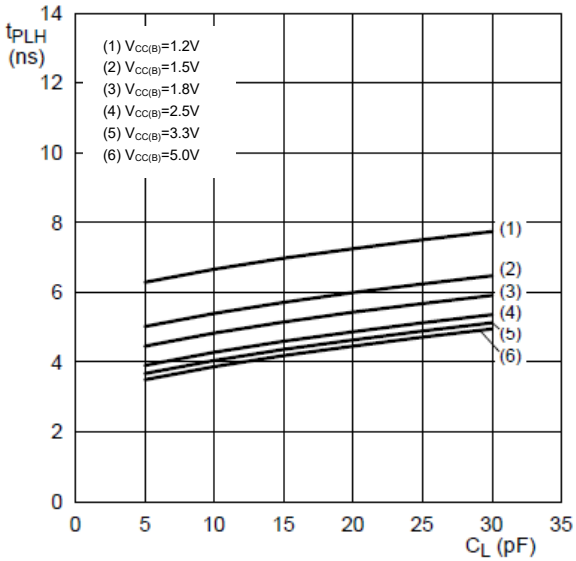
a. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$=1.8V



b. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$=1.8V

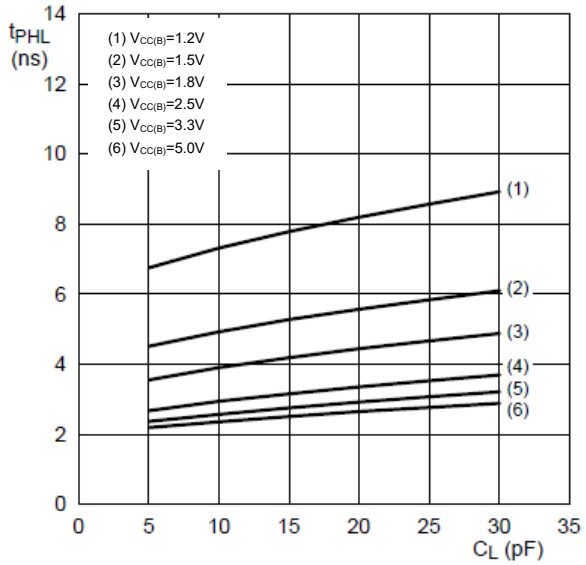


c. HIGH to LOW propagation delay (B to A); $V_{CC(A)}$=1.8V

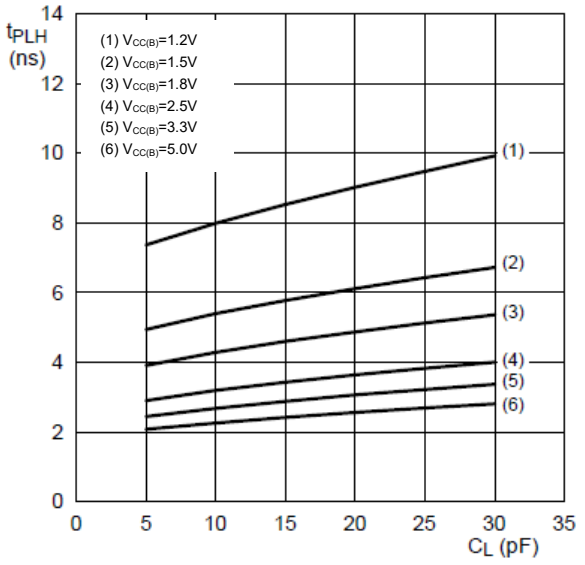


d. LOW to HIGH propagation delay (B to A); $V_{CC(A)}$=1.8V

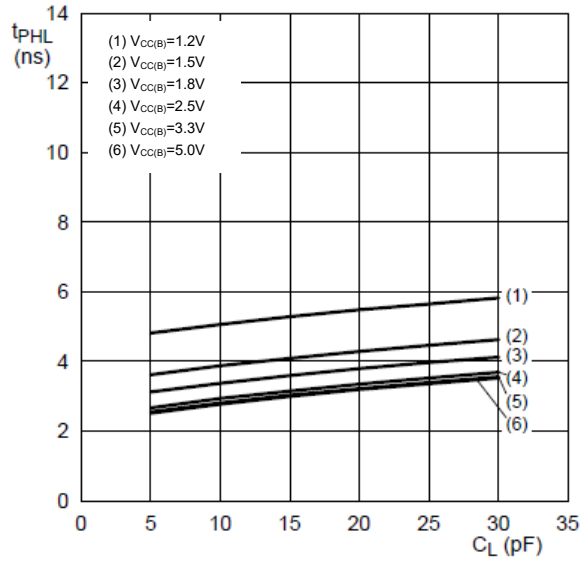
Figure 9-3 Typical propagation delay versus load capacitance; T_{amb}=25°C



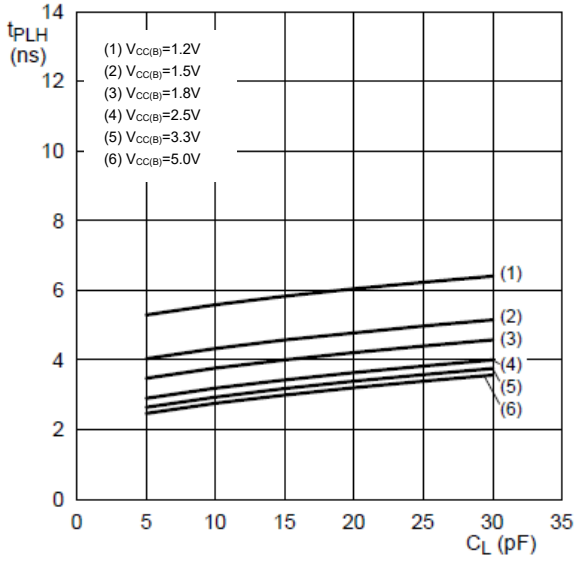
a. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$=2.5V



b. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$= 2.5V

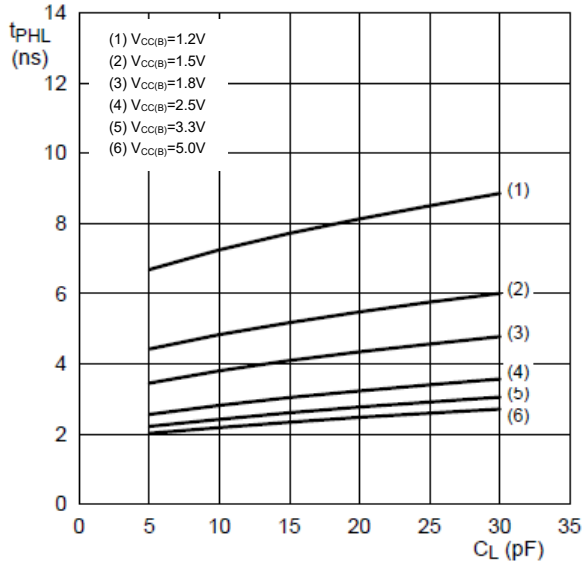


c. HIGH to LOW propagation delay (B to A); $V_{CC(A)}$= 2.5V

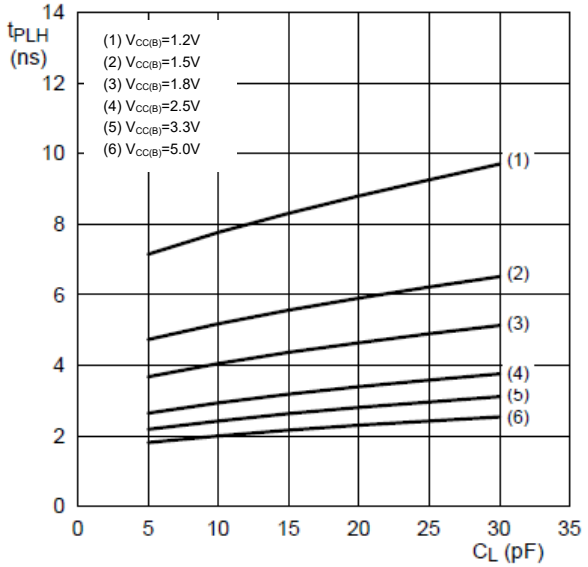


d. LOW to HIGH propagation delay (B to A); $V_{CC(A)}$= 2.5V

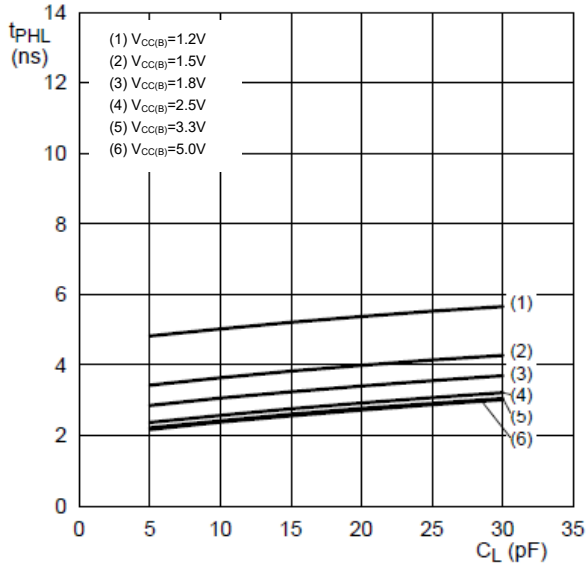
Figure 9-4 Typical propagation delay versus load capacitance; T_{amb}=25°C



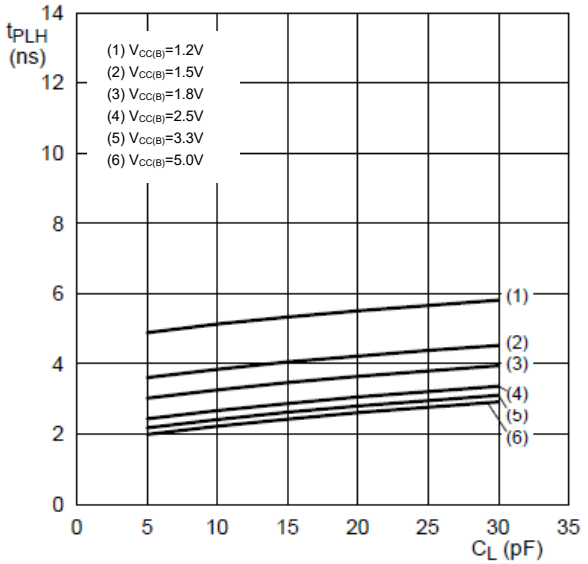
a. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$=3.3V



b. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$= 3.3V

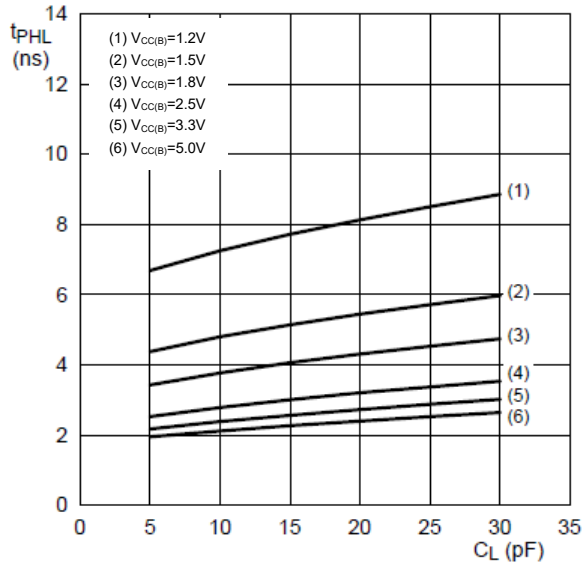


c. HIGH to LOW propagation delay (B to A); $V_{CC(A)}$= 3.3V

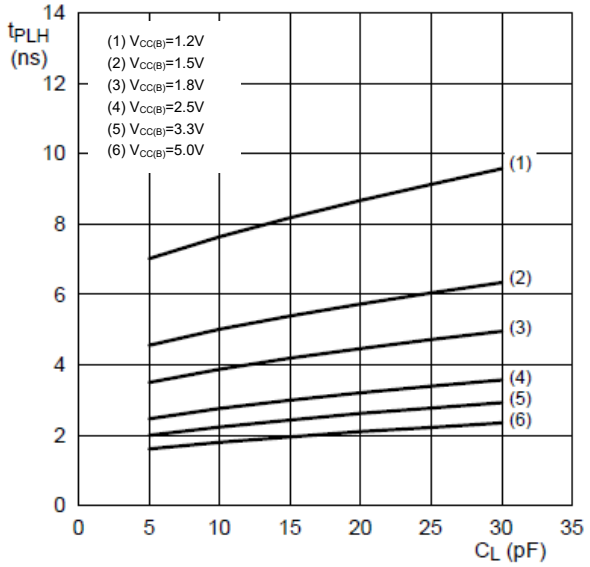


d. LOW to HIGH propagation delay (B to A); $V_{CC(A)}$= 3.3V

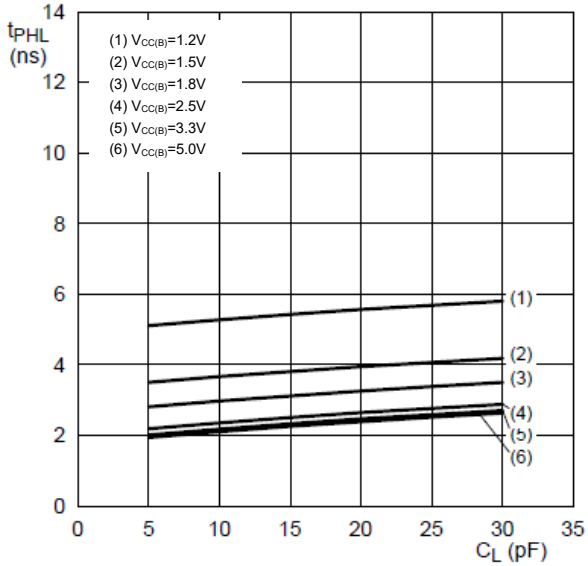
Figure 9-5 Typical propagation delay versus load capacitance; T_{amb}=25°C



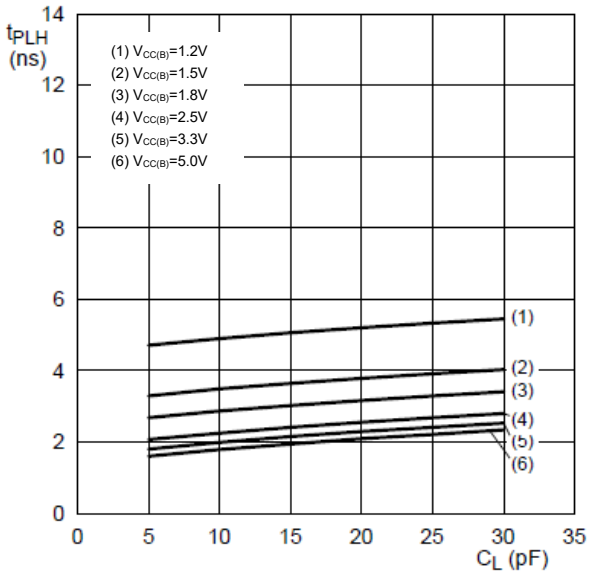
a. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$=5.0V



b. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$= 5.0V



c. HIGH to LOW propagation delay (B to A); $V_{CC(A)}$= 5.0V



d. LOW to HIGH propagation delay (B to A); $V_{CC(A)}$= 5.0V

Figure 9-6 Typical propagation delay versus load capacitance; T_{amb}=25°C

10 Typical Application Circuit and Application Note

10.1 Unidirectional Logic Level-shifting Application

The circuit given in Figure 10-1 is an example of the CJ74LVC1T45; CJ74LVCH1T45 being used in a unidirectional logic level-shifting application.

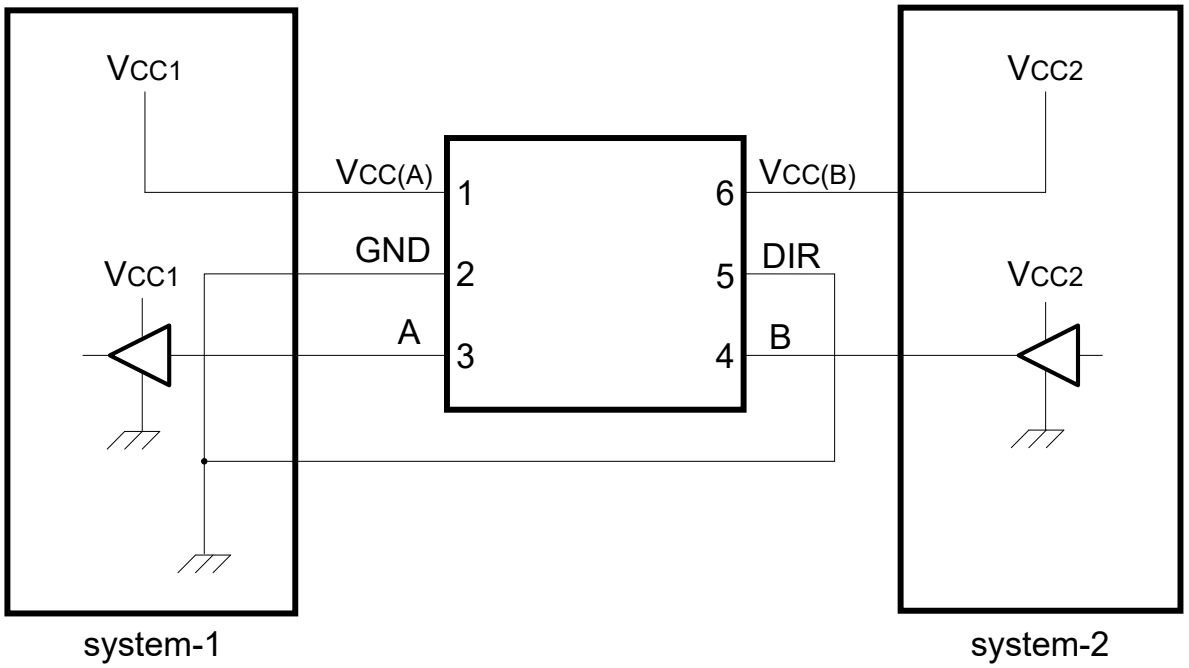


Figure 10-1 Unidirectional logic level-shifting application

Table 1. Description of unidirectional logic level-shifting application

PIN	NAME	FUNCTION	DESCRIPTION
1	$V_{CC(A)}$	V_{CC1}	Supply voltage of system-1 (1.2V to 5.5V)
2	GND	GND	Device GND
3	A	OUT	Output level depends on V_{CC1} voltage
4	B	IN	Input threshold value depends on V_{CC2} voltage
5	DIR	DIR	The GND (LOW level) determines B port to A port direction
6	$V_{CC(B)}$	V_{CC2}	Supply voltage of system-2 (1.2V to 5.5V)

10.2 Bidirectional Logic Level-shifting Application

Figure 10-2 shows the CJ74LVC1T45; CJ74LVCH1T45 being used in a bidirectional logic level-shifting application. Since the device does not have an output enable pin, the system designer should take precautions to avoid bus contention between system-1 and system-2 when changing directions.

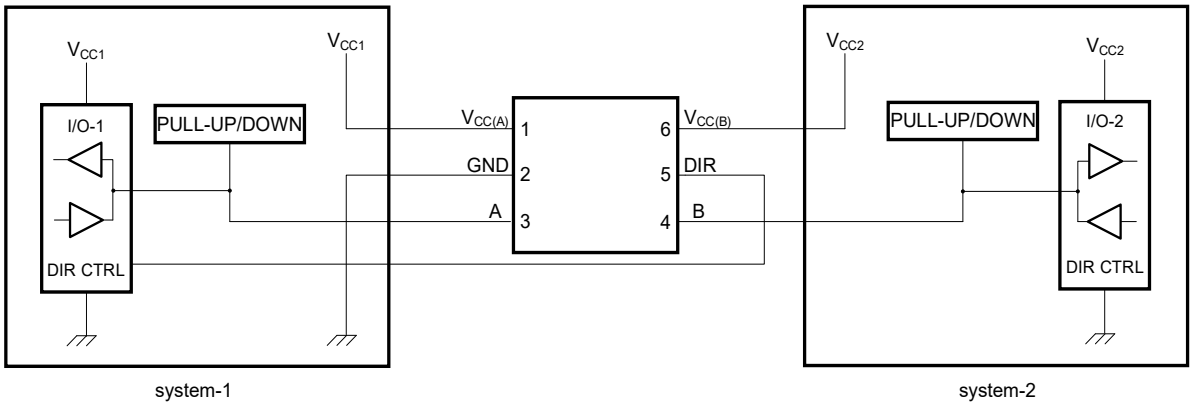


Figure 10-2 Bidirectional logic level-shifting application

Note: Pull-up or pull-down only needed for CJ74LVC1T45.

Table 2 gives a sequence that will illustrate data transmission from system-1 to system-2 and then from system-2 to system-1.

Table 2. Description of bidirectional logic level-shifting application

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Output	Input	System-1 data to system-2
2	H	Z	Z	System-2 is getting ready to send data to system-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on bus hold.
3	L	Z	Z	DIR bit is set LOW. I/O-1 and I/O-2 still are disabled. The bus-line state depends on bus hold.
4	L	Input	Output	System-2 data to system-1

Note: H=HIGH voltage level;L=LOW voltage level;Z=high-impedance OFF-state.

10.3 Power-up Considerations

The device is designed such that no special power-up sequence is required other than GND being applied first.

Table 3. Typical total supply current ($I_{CC(A)}$+$I_{CC(B)}$)

$V_{CC(A)}$	$V_{CC(B)}$					UNIT
	0V	0.8V	2.5V	3.3V	5.0V	
0V	0	<1	<1	<1	<1	uA
1.8V	<1	<2	<2	<2	2	uA
2.5V	<1	<2	<2	<2	<2	uA
3.3V	<1	<2	<2	<2	<2	uA
5.0V	<1	2	<2	<2	<2	uA

10.4 Enable Times

Calculate the enable times for the CJ74LVC1T45; CJ74LVCH1T45 using the following formulas:

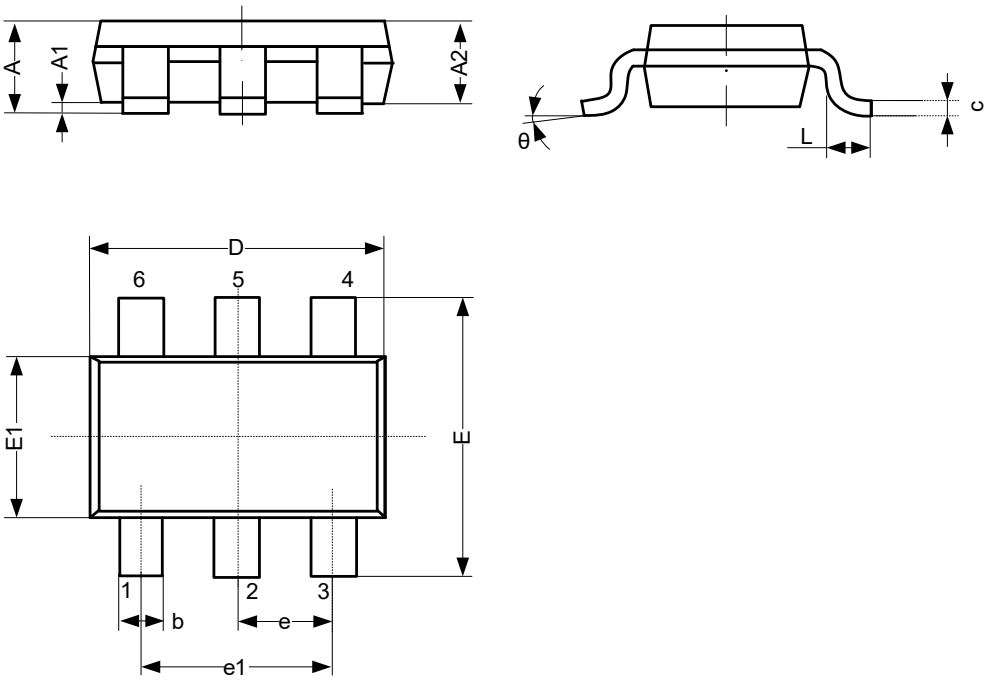
- t_{PZH}(DIR to A)=t_{PLZ}(DIR to B)+t_{PLH}(B to A)
- t_{PZL}(DIR to A)=t_{PHZ}(DIR to B)+t_{PHL}(B to A)
- t_{PZH}(DIR to B)=t_{PLZ}(DIR to A)+t_{PLH}(A to B)
- t_{PZL}(DIR to B)=t_{PHZ}(DIR to A)+t_{PHL}(A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the CJ74LVC1T45; CJ74LVCH1T45 initially is transmitting from A to B, then the DIR bit is switched, the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

11 Mechanical Information

11.1 SOT-23-6L Mechanical Information

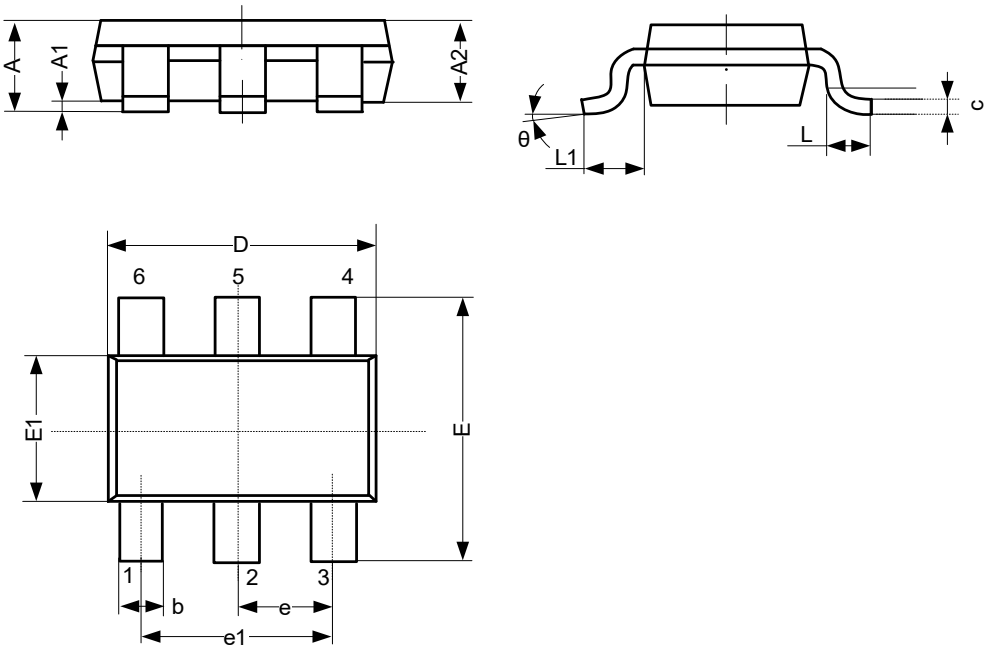
11.1.1 SOT-23-6L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.25
A1	0.00	-	0.12
A2	1.00	-	1.20
b	0.30	-	0.50
c	0.10	-	0.20
D	2.82	-	3.02
E	2.60	-	3.00
E1	1.50	-	1.70
e	0.95 BSC		
e1	1.80	-	2.00
L	0.30	-	0.60
Θ	0°	-	8°
Unit: mm			

11.2 SOT-363 Mechanical Information

11.2.1 SOT-363 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.90	-	1.10
A1	0.00	-	0.10
A2	0.90	-	1.00
b	0.15	-	0.35
c	0.11	-	0.175
D	2.00	-	2.20
E	2.15	-	2.45
E1	1.15	-	1.35
e	0.65 BSC		
e1	1.20	-	1.40
L	0.26	-	0.46
L1	-	0.525	-
Θ	0°	-	8°
Unit: mm			

12 Notes and Revision History

12.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

12.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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