Octal Bus Transceiver; 3-state

CJ74LVC245 Logic

1 Introduction

The CJ74LVC245 is a 8-bit transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features an output enable(/OE) input for easy cascading and a send/receive (DIR) input for direction control. /OE controls the outputs so that the buses are effectively isolated.

Inputs can be driven from either 3.3V or 5V devices. When disabled, up to 5.5V can be applied to the outputs. These features allow the use of these devices in mixed 3.3V and 5V applications.

2 Available Packages

PART NUMBER	PACKAGE
CJ74LVC245	SOP20
	TSSOP20
	QFN4.5x2.5-20L

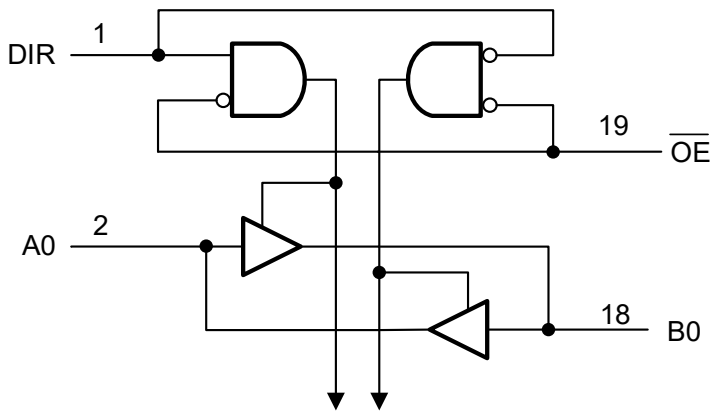
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- 5V tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range from 1.2V to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5V
- High-impedance when V_{CC}=0V

4 Applications

- Cable Modem Termination Systems
- Servers
- LED Displays
- Network Switches
- Telecom Infrastructure
- Motor Drivers
- I/O Expanders



Simplified schematic

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74LVC245AGN	SOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 2000 Units / Reel	Active
CJ74LVC245BGN	TSSOP20	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74LVC245QDN	QFN4.5x2.5-20L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

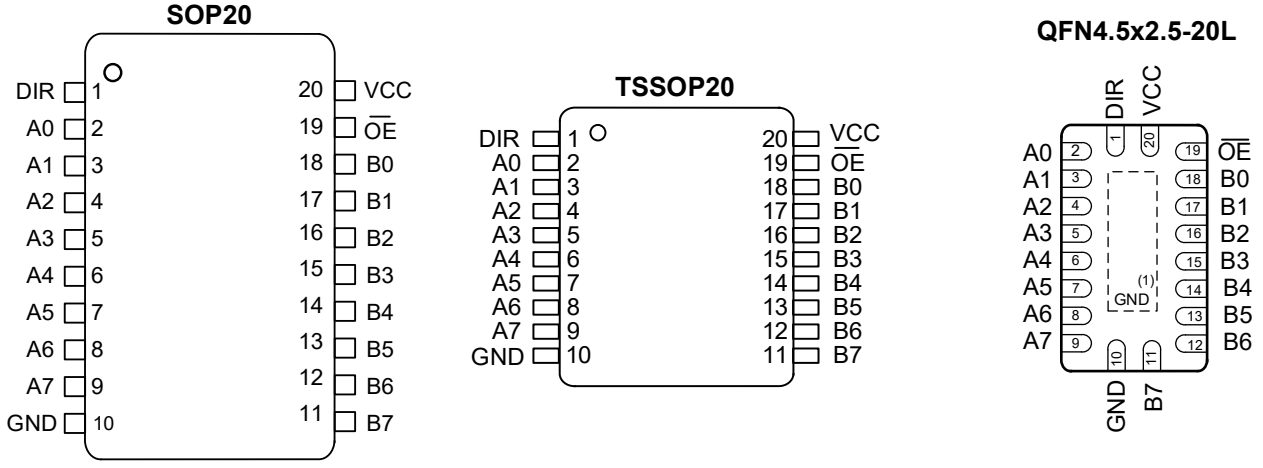


Figure 6-1 Pin configuration

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

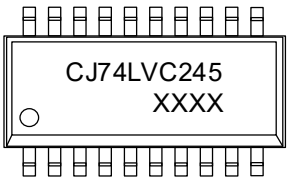
6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	DIR	-	Direction control
2	A0	I/O	Data input/output
3	A1	I/O	Data input/output
4	A2	I/O	Data input/output
5	A3	I/O	Data input/output
6	A4	I/O	Data input/output
7	A5	I/O	Data input/output
8	A6	I/O	Data input/output
9	A7	I/O	Data input/output
10	GND	G	Ground (0 V)
11	B7	I/O	Data input/output
12	B6	I/O	Data input/output
13	B5	I/O	Data input/output
14	B4	I/O	Data input/output
15	B3	I/O	Data input/output
16	B2	I/O	Data input/output
17	B1	I/O	Data input/output
18	B0	I/O	Data input/output
19	$\overline{OE}$	I	Output enable input (active LOW)
20	VCC	P	Supply voltage

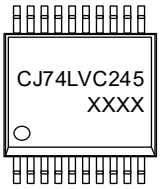
(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information

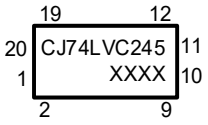
SOP20



TSSOP20



QFN4.5x2.5-20L



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-	-0.5	6.5	V
I_{IK}	Input clamping current	V_I < 0V	-50	-	mA
V_I	Input voltage	-	-0.5	6.5	V
I_{OK}	Output clamping current	V_O > V_{CC} or V_O < 0V	-	±50	mA
V_O	Output voltage	Output HIGH or LOW	-0.5	V_{CC}+0.5	V
		Output 3-state	-0.5	6.5	V
I_O	Output current	V_O=0V to V_{CC}	-	±50	mA
I_{CC}	Supply current	-	-	100	mA
I_{GND}	Ground current	-	-100	-	mA
T_{stg}	Storage temperature	-	-65	150	°C
P_{tot}	Total power dissipation	-	-	500	mW
T_L	Soldering Temperature	10s	-	260	°C

Note:

(1) The minimum input voltage ratings may be exceeded if the input current ratings are observed.

(2) The output voltage ratings may be exceeded if the output current ratings are observed.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage	-	1.65	-	5.5	V
		Functional	1.2	-	5.5	V
V_I	Input voltage	-	0	-	5.5	V
V_O	Output voltage	Output HIGH or LOW	0	-	V_{CC}	V
		Output 3-state	0	-	5.5	V
T_{amb}	Ambient temperature	In free air	-40	-	+125	°C
Δt/ΔV	Input transition rise and fall rate	V_{CC}=1.2V to 2.7V	0	-	20	ns/V
		V_{CC}=2.7V to 3.6V	0	-	10	ns/V

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM)(1)	±4000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	V_{CC}=1.2V		1.08	-	-	V
		V_{CC}=1.65V to 1.95V		0.65xV_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=1.2V		-	-	0.12	V
		V_{CC}=1.65V to 1.95V		-	-	0.35xV_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 3.6V	V_{CC}-0.2	-	-	V
			I_O=-4mA;V_{CC}=1.65V	1.2	-	-	V
			I_O=-8mA;V_{CC}=2.3V	1.8	-	-	V
			I_O=-12mA;V_{CC}= 2.7V	2.2	-	-	V
			I_O=-18mA;V_{CC}= 3.0V	2.4	-	-	V
			I_O=-24mA;V_{CC}= 3.0V	2.2	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.65V to 3.6V	-	-	0.2	V
			I_O=4mA;V_{CC}=1.65V	-	-	0.45	V
			I_O=8mA;V_{CC}=2.3V	-	-	0.6	V
			I_O=12mA;V_{CC}=2.7V	-	-	0.4	V
			I_O=24mA;V_{CC}=3.0V	-	-	0.55	V
I_I	Input leakage current	V_{CC}=3.6V; V_I=5.5V or GND		-	-	±5	uA
I_{OZ}	OFF-state output current	V_{CC}=3.6V; V_I=V_{IH} or V_{IL}; V_O=5.5V or GND		-	-	±5	uA
I_{OFF}	Power-off leakage current	V_{CC}=0V; V_I or V_O=5.5V		-	-	±10	uA
I_{CC}	Supply current	V_{CC}=3.6V; V_I=V_{CC} or GND; I_O=0A		-	-	10	uA
ΔI_{CC}	Additional supply current	Per input pin; V_{CC}=2.7V to 3.6V; V_I=V_{CC}-0.6V; I_O=0A		-	-	500	uA
C_I	Input capacitance	V_{CC}=0V to 3.6V; V_I=GND to V_{CC}		-	4	-	pF
$C_{I/O}$	Input/output capacitance	V_{CC}=0V to 3.6V; V_I=GND to V_{CC}		-	10	-	pF

Note:

(1) All typical values are measured at V_{CC}=3.3V (unless stated otherwise) and T_{amb}=25°C.

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	V_{CC}=1.2V		1.08	-	-	V
		V_{CC}=1.65V to 1.95V		0.65xV_{CC}	-	-	V
		V_{CC}=2.3V to 2.7V		1.7	-	-	V
		V_{CC}=2.7V to 3.6V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=1.2V		-	-	0.12	V
		V_{CC}=1.65V to 1.95V		-	-	0.35xV_{CC}	V
		V_{CC}=2.3V to 2.7V		-	-	0.7	V
		V_{CC}=2.7V to 3.6V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-100uA; V_{CC}=1.65V to 3.6V	V_{CC}-0.3	-	-	V
			I_O=-4mA;V_{CC}=1.65V	1.05	-	-	V
			I_O=-8mA;V_{CC}=2.3V	1.65	-	-	V
			I_O=-12mA;V_{CC}= 2.7V	2.05	-	-	V
			I_O=-18mA;V_{CC}= 3.0V	2.25	-	-	V
			I_O=-24mA;V_{CC}= 3.0V	2.0	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=100uA; V_{CC}=1.65V to 3.6V	-	-	0.3	V
			I_O=4mA;V_{CC}=1.65V	-	-	0.65	V
			I_O=8mA;V_{CC}=2.3V	-	-	0.8	V
			I_O=12mA;V_{CC}=2.7V	-	-	0.6	V
			I_O=24mA;V_{CC}=3.0V	-	-	0.8	V
I_I	Input leakage current	V_{CC}=3.6V; V_I=5.5V or GND		-	-	±20	uA
I_{OZ}	OFF-state output current	V_{CC}=3.6V; V_I=V_{IH} or V_{IL}; V_O=5.5V or GND		-	-	±20	uA
I_{OFF}	Power-off leakage current	V_{CC}=0V; V_I or V_O=5.5V		-	-	±20	uA
I_{CC}	Supply current	V_{CC}=3.6V; V_I=V_{CC} or GND; I_O=0A		-	-	40	uA
ΔI_{CC}	Additional supply current	Per input pin; V_{CC}=2.7V to 3.6V; V_I=V_{CC}-0.6V; I_O=0A		-	-	5000	uA

Note:

(1) All typical values are measured at V_{CC}=3.3V (unless stated otherwise) and T_{amb}=25°C.

7.4.3 AC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{pd}	nAn to nBn nBn to nAn propagation delay	See Figure 8-4	V_{CC}=1.2V	-	17.0	-	ns
			V_{CC}=1.65V to 1.95V	1.5	6.5	14.6	ns
			V_{CC}=2.3V to 2.7V	1.0	3.4	7.6	ns
			V_{CC}=2.7V	1.5	3.4	7.3	ns
			V_{CC}=3.0V to 3.6V	1.5	2.9	6.3	ns
t_{en}	$\overline{nOE}$ to nAn/nBn enable time	See Figure 8-5	V_{CC}=1.2V	-	22.0	-	ns
			V_{CC}=1.65V to 1.95V	1.9	8.3	19.5	ns
			V_{CC}=2.3V to 2.7V	1.5	4.6	10.7	ns
			V_{CC}=2.7V	1.5	4.8	9.5	ns
			V_{CC}=3.0V to 3.6V	1.5	3.7	8.5	ns
t_{dis}	$\overline{nOE}$ to nAn/nBn disable time	See Figure 8-5	V_{CC}=1.2V	-	12.0	-	ns
			V_{CC}=1.65V to 1.95V	2.9	5.5	12.3	ns
			V_{CC}=2.3V to 2.7V	1.0	3.1	7.1	ns
			V_{CC}=2.7V	1.5	3.9	8.0	ns
			V_{CC}=3.0V to 3.6V	1.7	3.6	7.0	ns
$t_{sk(o)}$	Output skew time	-		-	-	1.0	ns
C_{PD}	Power dissipation capacitance	Per input; V_I=GND to V_{CC}	V_{CC}=1.65V to 1.95V	-	7.7	-	pF
			V_{CC}=2.3V to 2.7V	-	11.3	-	pF
			V_{CC}=3.0V to 3.6V	-	14.4	-	pF

Note:

(1) Typical values are measured at T_{amb}=25°C and V_{CC}=1.8V, 2.5V, 2.7V, and 3.3V respectively.

(2) t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZH} and t_{PZL}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

(3) Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

(4) C_{PD} is used to determine the dynamic power dissipation (P_D in uW).
$P_D=(C_{PD}xV_{CC}^2xf_ixN)+\sum(C_LxV_{CC}^2xf_o)$ where:
f_i=input frequency in MHz.
f_o=output frequency in MHz.
C_L=output load capacitance in pF.
V_{CC}=supply voltage in V_{olt}.
N=number of inputs switching.
$\sum(C_LxV_{CC}^2xf_o)$=sum of the outputs.

7.4.4 AC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{pd}	nAn to nBn nBn to nAn propagation delay	See Figure 8-4	V_{CC}=1.65V to 1.95V	1.5	-	16.9	ns
			V_{CC}=2.3V to 2.7V	1.0	-	8.7	ns
			V_{CC}=2.7V	1.5	-	9.5	ns
			V_{CC}=3.0V to 3.6V	1.5	-	8.0	ns
t_{en}	$\overline{nOE}$ to nAn/nBn enable time	See Figure 8-5	V_{CC}=1.65V to 1.95V	1.9	-	22.5	ns
			V_{CC}=2.3V to 2.7V	1.5	-	12.4	ns
			V_{CC}=2.7V	1.5	-	12.0	ns
			V_{CC}=3.0V to 3.6V	1.5	-	11.0	ns
t_{dis}	$\overline{nOE}$ to nAn/nBn disable time	See Figure 8-5	V_{CC}=1.65V to 1.95V	2.9	-	14.2	ns
			V_{CC}=2.3V to 2.7V	1.0	-	8.2	ns
			V_{CC}=2.7V	1.5	-	10.0	ns
			V_{CC}=3.0V to 3.6V	1.7	-	9.0	ns
$t_{sk(o)}$	Output skew time	-		-	-	1.5	ns

Note:

(1) Typical values are measured at T_{amb}=25°C and V_{CC}=1.8V, 2.5V, 2.7V, and 3.3V respectively.

(2) t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZH} and t_{PZL}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

(3) Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

8 Detailed Description

8.1 Overview

The CJ74LVC245 is a 8-bit transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features an output enable(/OE) input for easy cascading and a send/receive (DIR) input for direction control. /OEcontrols the outputs so that the buses are effectively isolated.

Inputs can be driven from either 3.3V or 5V devices. When disabled, up to 5.5V can be applied to the outputs. These features allow the use of these devices in mixed 3.3V and 5V applications.

8.2 Functional Block Diagram

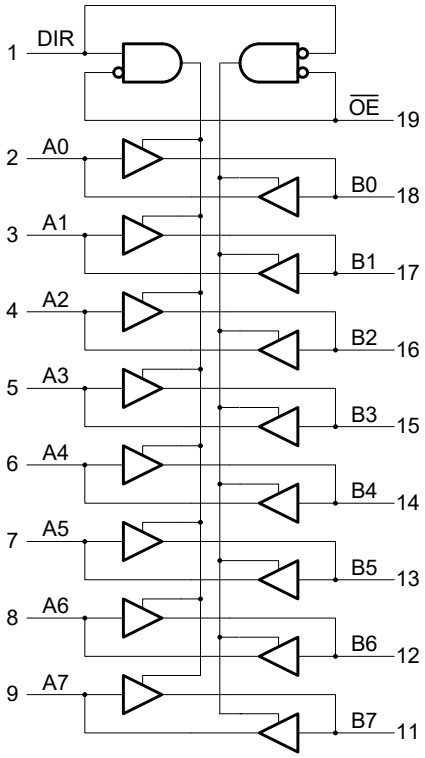


Figure 8-1 Logic diagram

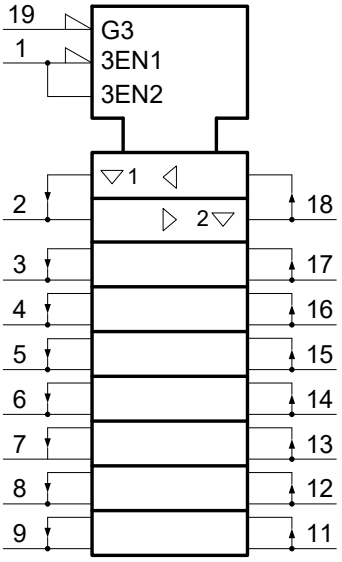


Figure 8-2 IEC Logic symbol

8.3 Function Table

INPUT		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	An	Bn
L	L	An=Bn	Inputs
L	H	Inputs	Bn=An
H	X	Z	Z

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

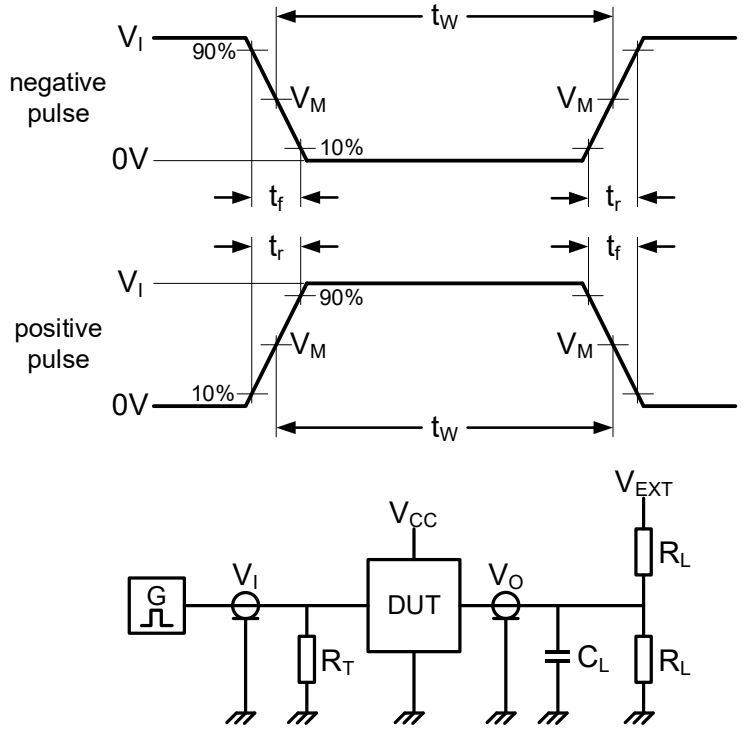


Figure 8-3 Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT}=External voltage for measuring switching times.

8.4.2 AC Testing Waveforms

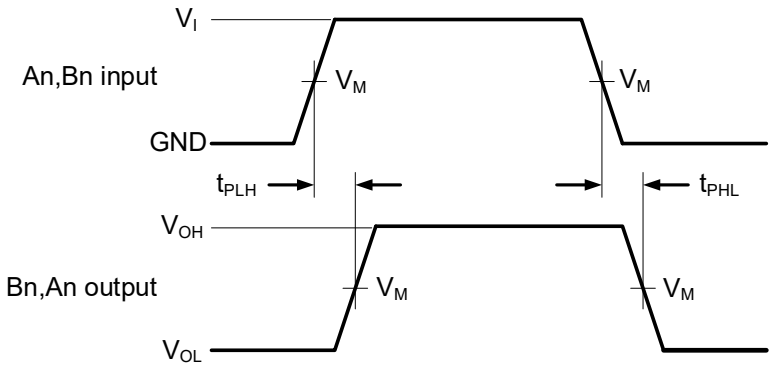


Figure 8-4 The input (An,Bn) to output (Bn,An) propagation delays

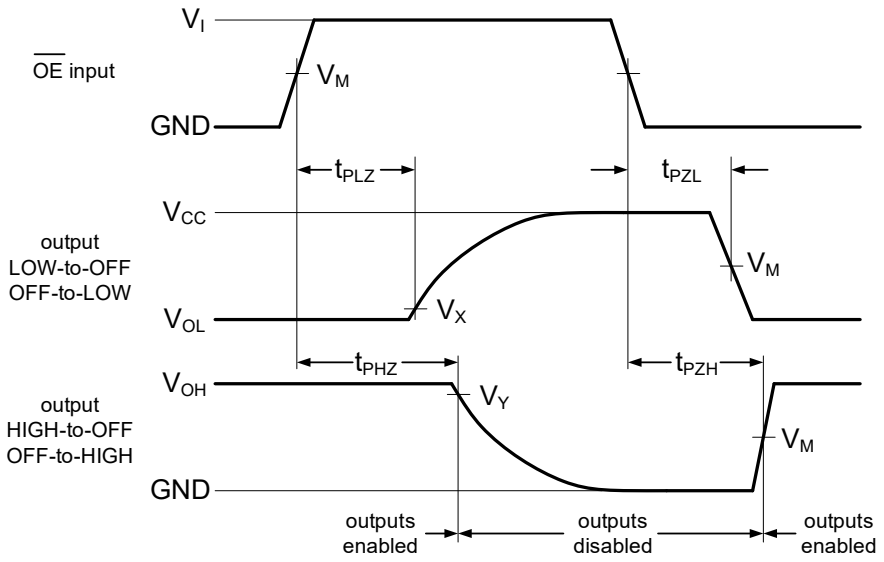


Figure 8-5 3-state enable and disable times

8.4.3 Measurement Points

SUPPLY VOLTAGE	V_M	INPUT		
V_{CC}		V_I	V_X	V_Y
1.2V	0.5xV_{CC}	V_{CC}	V_{OL}+0.15V	V_{OH}-0.15V
1.65V to 1.95V	0.5xV_{CC}	V_{CC}	V_{OL}+0.15V	V_{OH}-0.15V
2.3V to 2.7V	0.5xV_{CC}	V_{CC}	V_{OL}+0.15V	V_{OH}-0.15V
2.7V	1.5V	2.7V	V_{OL}+0.3V	V_{OH}-0.3V
3.0V to 3.6V	1.5V	2.7V	V_{OL}+0.3V	V_{OH}-0.3V

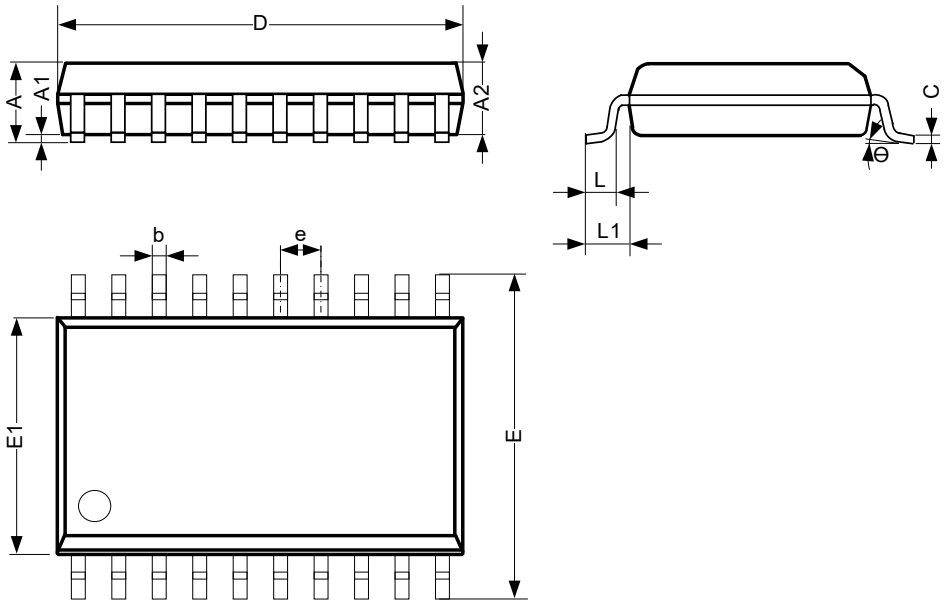
8.4.4 Test Data

SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}		
V_{CC}	V_I	t_r,t_f	C_L	R_L	t_{PLH},t_{PHL}	t_{PLZ},t_{PZL}	t_{PHZ},t_{PZH}
1.2V	V_{CC}	≤2ns	30pF	1kΩ	Open	2xV_{CC}	GND
1.65V to 1.95V	V_{CC}	≤2ns	30pF	1kΩ	Open	2xV_{CC}	GND
2.3V to 2.7V	V_{CC}	≤2ns	30pF	500Ω	Open	2xV_{CC}	GND
2.7V	2.7V	≤2.5ns	50pF	500Ω	Open	2xV_{CC}	GND
3.0V to 3.6V	2.7V	≤2.5ns	50pF	500Ω	Open	2xV_{CC}	GND

9 Mechanical Information

9.1 SOP20 Mechanical Information

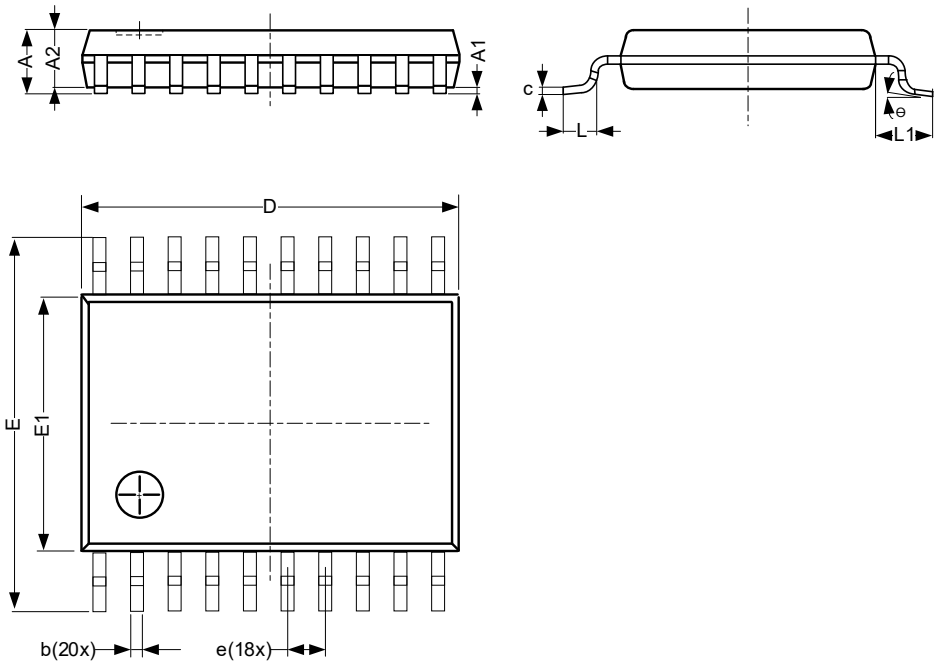
9.1.1 SOP20 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	2.47	-	2.65
A1	0.05	-	0.30
A2	2.20	-	2.44
b	0.35	-	0.50
c	0.15	-	0.30
D	12.54	-	12.94
E	10.00	-	10.60
E1	7.30	-	7.70
e	1.27 BSC		
L	0.40	-	1.05
L1	1.30	-	1.50
Θ	0°	-	8°
Unit: mm			

9.2 TSSOP20 Mechanical Information

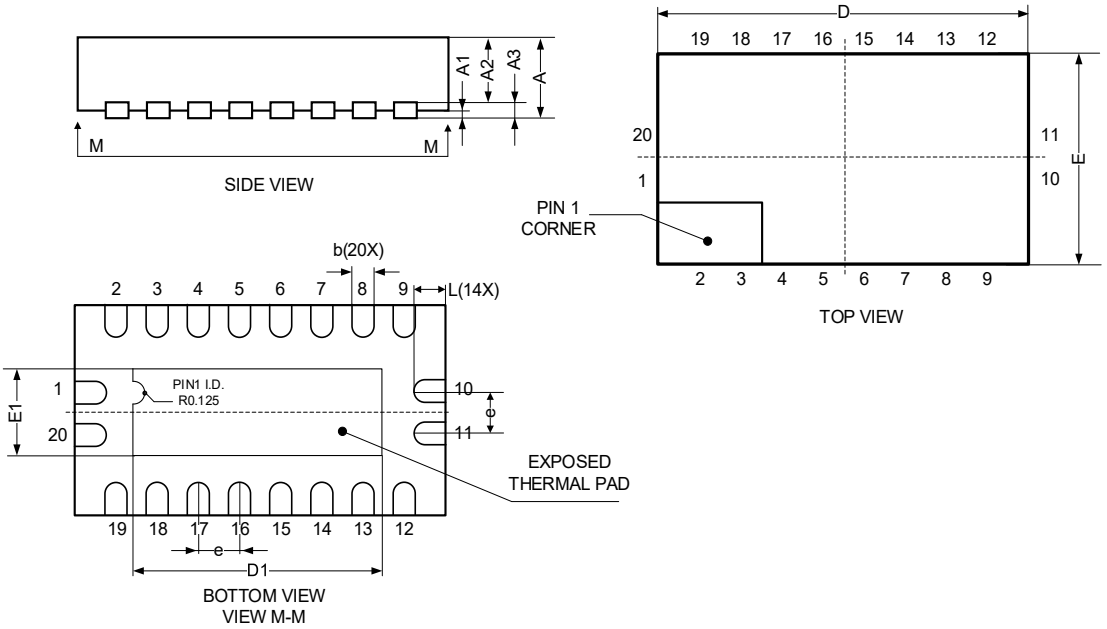
9.2.1 TSSOP20 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	6.40	-	6.60
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
θ	0°	-	8°
Unit: mm			

9.3 QFN4.5x2.5-20L Mechanical Information

9.3.1 QFN4.5x2.5-20L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.80	-	1.00
A1	0.00	-	0.05
A2	0.60	-	0.70
A3	-	0.20	-
D	4.40	-	4.60
E	2.40	-	2.60
e	0.50 BSC		
b	0.18	-	0.30
L	0.30	-	0.50
D1	2.70	-	3.15
E1	0.70	-	1.15
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of JSCJ, this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. JSCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

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