

Dual Buffer (Open-drain)

CJ74LVC2G07 Logic

1 Introduction

The CJ74LVC2G07 provides two non-inverting buffers.

The output of this device is an open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device in a mixed 3.3V and 5V environment.

2 Available Packages

PART NUMBER	PACKAGE
CJ74LVC2G07	SOT-23-6L
	SOT-363
	DFN1.45x1-6L
	DFN1x1-6L

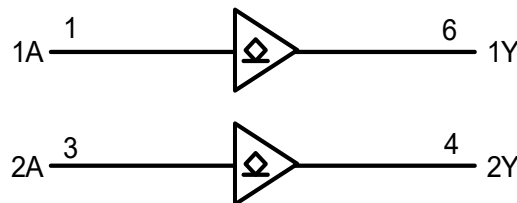
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range from 1.65V to 5.5V
- 5V tolerant inputs for interfacing with 5V logic
- -24mA output drive ($V_{CC}=3.0V$)
- CMOS low power consumption
- Specified from -40°C to +125°C

4 Applications

- Blu-ray Players and Home Theaters
- DVD Recorders and Players
- Desktops or Notebook PCs
- Digital Video Cameras (DVC)
- Embedded PCs
- GPS: Personal Navigation Devices
- Mobile Phones
- Network Projector Front Ends
- Portable Media Players
- Solid State Drive (SSD): Enterprise
- High-Definition (HDTV)
- Tablet: Enterprise
- Audio Dock: Portable
- DLP Front Projection System



Functional block diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74LVC2G07M6N	SOT-23-6L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units / Reel	Active
CJ74LVC2G07R6N	SOT-363	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units / Reel	Active
CJ74LVC2G07DNN	DFN1.45x1-6L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active
CJ74LVC2G07DKN	DFN1x1-6L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

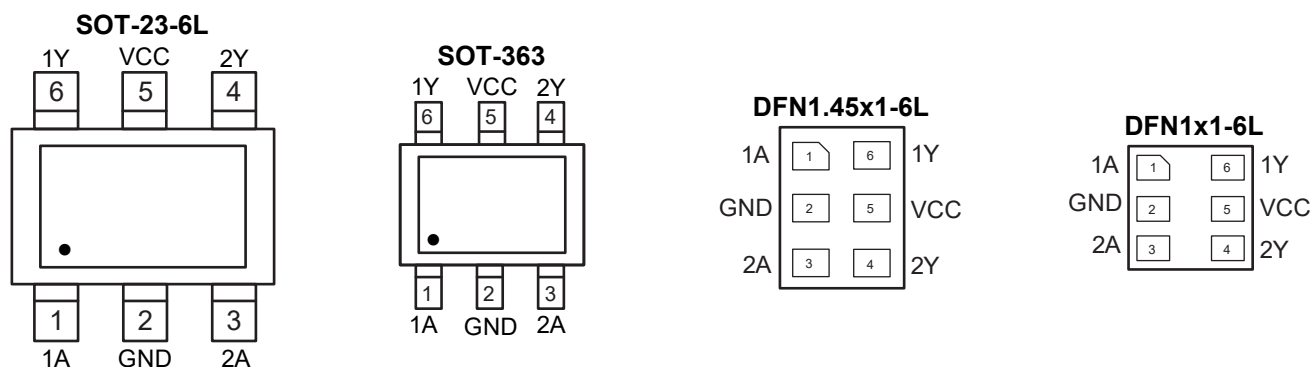


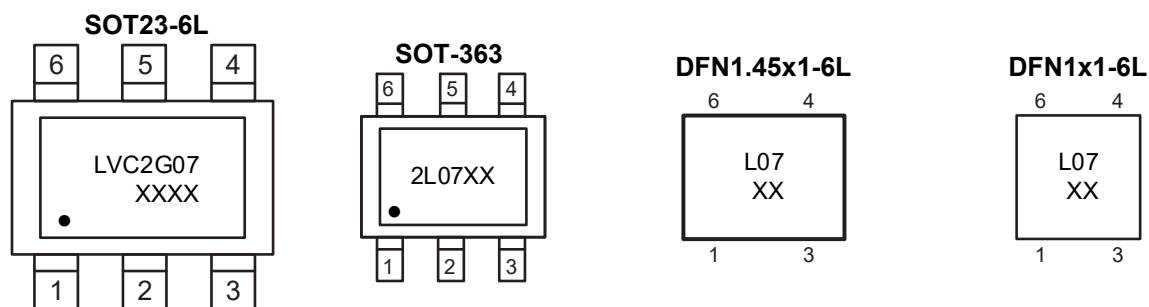
Figure 6-1 Pin configuration

6.2 Pin Function

PIN		I/O ⁽¹⁾	DESCRIPTION
No.	NAME		
1	1A	I	Data input
2	GND	G	Ground (0V)
3	2A	I	Data input
4	2Y	O	Data output
5	VCC	P	Supply voltage
6	1Y	O	Data output

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



XXXX or XX : Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-	-0.5	+6.5	V
I_{IK}	Input clamping current	$V_I < 0V$	-	-50	mA
V_I	Input voltage	-	-0.5	+6.5	V
I_{OK}	Output clamping current	$V_O < 0V$	-	-50	mA
V_O	Output voltage	Active mode	-0.5	+6.5	V
		Power-down mode	-0.5	+6.5	V
I_O	Output current	$V_O=0V$ to 6.5V	-	50	mA
I_{CC}	Supply current	-	-	100	mA
I_{GND}	Ground current	-	-	-100	mA
T_{stg}	Storage temperature	-	-65	+150	°C
P_{tot}	Total power dissipation	-	-	250	mW
T_L	Soldering temperature	10s	-	260	°C

Note: When $V_{CC}=0V$ (Power-down mode), the output voltage can be 5.5V in normal operation.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage	-	1.65	-	5.5	V
V_I	Input voltage	-	0	-	5.5	V
V_O	Output voltage	Active mode	0	-	5.5	V
		Power-down mode; $V_{CC}=0V$	0	-	5.5	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) ⁽¹⁾	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	$V_{CC}=1.65\text{V}$ to 1.95V		$0.65 \times V_{CC}$	-	-	V
		$V_{CC}=2.3\text{V}$ to 2.7V		1.7	-	-	V
		$V_{CC}=2.7\text{V}$ to 3.6V		2.0	-	-	V
		$V_{CC}=4.5\text{V}$ to 5.5V		$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC}=1.65\text{V}$ to 1.95V		-	-	$0.35 \times V_{CC}$	V
		$V_{CC}=2.3\text{V}$ to 2.7V		-	-	0.7	V
		$V_{CC}=2.7\text{V}$ to 3.6V		-	-	0.8	V
		$V_{CC}=4.5\text{V}$ to 5.5V		-	-	$0.3 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_O=100\mu\text{A}$; $V_{CC}=1.65\text{V}$ to 5.5V	-	-	0.10	V
			$I_O=4\text{mA}$; $V_{CC}=1.65\text{V}$	-	-	0.45	V
			$I_O=8\text{mA}$; $V_{CC}=2.3\text{V}$	-	-	0.30	V
			$I_O=12\text{mA}$; $V_{CC}=2.7\text{V}$	-	-	0.40	V
			$I_O=24\text{mA}$; $V_{CC}=3.0\text{V}$	-	-	0.55	V
			$I_O=32\text{mA}$; $V_{CC}=4.5\text{V}$	-	-	0.55	V
I_I	Input leakage current	$V_I=5.5\text{V}$ or GND; $V_{CC}=0\text{V}$ to 5.5V		-	-	± 1	μA
I_{OZ}	OFF-state output current	$V_I=V_{IH}$ or V_{IL} ; $V_O=V_{CC}$ or GND; $V_{CC}=5.5\text{V}$		-	-	± 2	μA
I_{OFF}	Power-off leakage current	V_I or $V_O=5.5\text{V}$; $V_{CC}=0\text{V}$		-	-	± 2	μA
I_{CC}	Supply current	$V_I=5.5\text{V}$ or GND; $I_O=0\text{A}$; $V_{CC}=1.65\text{V}$ to 5.5V		-	-	4	μA
ΔI_{CC}	Additional supply current	Per pin; $V_I=V_{CC}-0.6\text{V}$; $I_O=0\text{A}$; $V_{CC}=2.3\text{V}$ to 5.5V		-	-	500	μA
C_i	Input capacitance	-		-	2.5	-	pF

Note: All typical values are measured at $V_{CC}=3.3\text{V}$ and $T_{amb}=25^{\circ}\text{C}$.

7.4.2 DC Characteristics 2

T_{amb}=−40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V _{IH}	HIGH-level input voltage	V _{CC} =1.65V to 1.95V		0.65xV _{CC}	-	-	V
		V _{CC} =2.3V to 2.7V		1.7	-	-	V
		V _{CC} =2.7V to 3.6V		2.0	-	-	V
		V _{CC} =4.5V to 5.5V		0.7xV _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} =1.65V to 1.95V		-	-	0.35xV _{CC}	V
		V _{CC} =2.3V to 2.7V		-	-	0.7	V
		V _{CC} =2.7V to 3.6V		-	-	0.8	V
		V _{CC} =4.5V to 5.5V		-	-	0.3xV _{CC}	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}	I _O =100uA; V _{CC} =1.65V to 5.5V	-	-	0.10	V
			I _O =4mA; V _{CC} =1.65V	-	-	0.70	V
			I _O =8mA; V _{CC} =2.3V	-	-	0.45	V
			I _O =12mA; V _{CC} =2.7V	-	-	0.60	V
			I _O =24mA; V _{CC} =3.0V	-	-	0.80	V
			I _O =32mA; V _{CC} =4.5V	-	-	0.80	V
I _I	Input leakage current	V _I =5.5V or GND; V _{CC} =0V to 5.5V		-	-	±1	uA
I _{OZ}	OFF-state output current	V _I =V _{IH} or V _{IL} ; V _O =V _{CC} or GND; V _{CC} =5.5V		-	-	±2	uA
I _{OFF}	Power-off leakage current	V _I or V _O =5.5V; V _{CC} =0V		-	-	±2	uA
I _{CC}	Supply current	V _I =5.5V or GND; I _O =0A; V _{CC} =1.65V to 5.5V		-	-	4	uA
ΔI _{CC}	Additional supply current	Per pin; V _I =V _{CC} -0.6V; I _O =0A; V _{CC} =2.3V to 5.5V		-	-	500	uA

7.4.3 AC Characteristics 1

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
t _{PLZ} , t _{PZL}	nA to nY propagation delay	See Figure 8-5	V _{CC} =1.65V to 1.95V	-	12.3	18.4	ns
			V _{CC} =2.3V to 2.7V	-	8.4	12.6	ns
			V _{CC} =2.7V	-	8.1	12.1	ns
			V _{CC} =3.0V to 3.6V	-	9.1	13.7	ns
			V _{CC} =4.5V to 5.5V	-	5.3	7.9	ns

(1) Typical values are measured at $T_{amb}=25^{\circ}\text{C}$ and $V_{CC}=1.8\text{V}$, 2.5V , 2.7V , 3.3V and 5.0V respectively.

7.4.4 AC Characteristics 2

$T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t _{PLZ} , t _{PZL}	nA to nY propagation delay	See Figure 8-5	V _{CC} =1.65V to 1.95V	-	-	23.0	ns
			V _{CC} =2.3V to 2.7V	-	-	16.1	ns
			V _{CC} =2.7V	-	-	15.2	ns
			V _{CC} =3.0V to 3.6V	-	-	17.3	ns
			V _{CC} =4.5V to 5.5V	-	-	10.0	ns

8 Detailed Description

8.1 Overview

The CJ74LVC2G07 provides two non-inverting buffers.

The output of this device is an open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device in a mixed 3.3V and 5V environment.

8.2 Functional Block Diagram

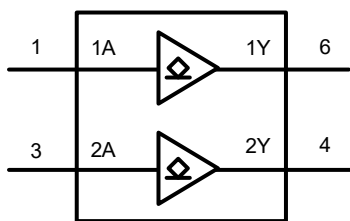


Figure 8-1 Logic symbol

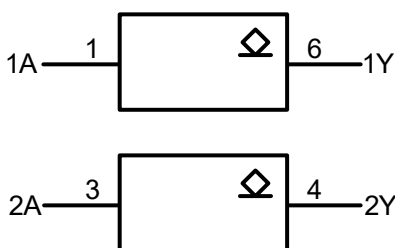


Figure 8-2 IEC logic symbol

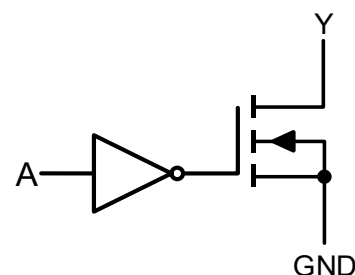


Figure 8-3 Logic diagram

8.3 Function Table⁽¹⁾

INPUT	OUTPUT
nA	nY
L	L
H	Z

(1) H=HIGH voltage level; L=LOW voltage level; Z=high-impedance OFF-state.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

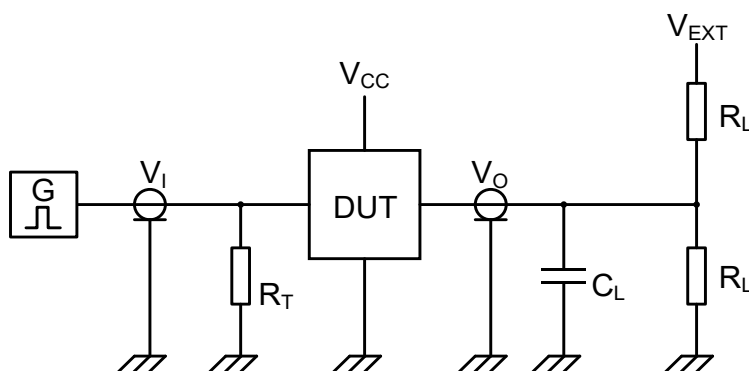


Figure 8-4 Test circuit for measuring switching times

Definitions for test circuit:

R_L =Load resistance.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance; should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} =External voltage for measuring switching times.

8.4.2 AC Testing Waveforms

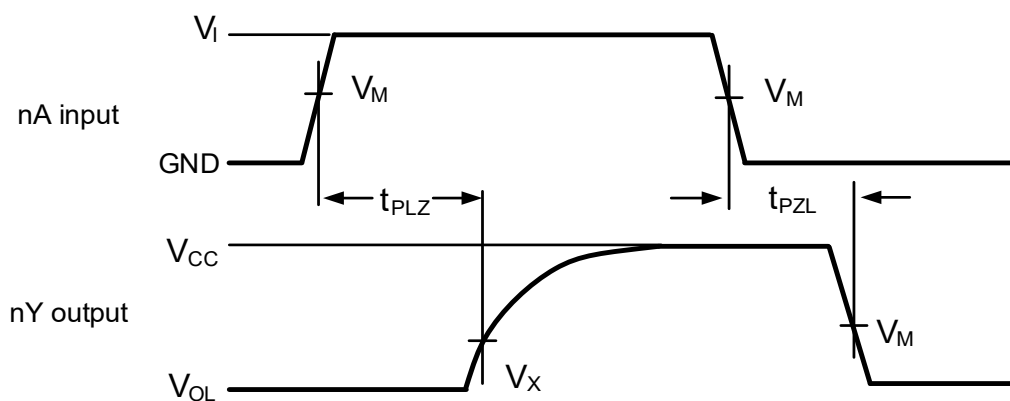


Figure 8-5 The input nA to output nY propagation delays

8.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT	
V_{CC}	V_M	V_M	V_X
1.65V to 1.95V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15V$
2.3V to 2.7V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15V$
2.7V	1.5V	1.5V	$V_{OL} + 0.3V$
3.0V to 3.6V	1.5V	1.5V	$V_{OL} + 0.3V$
4.5V to 5.5V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3V$

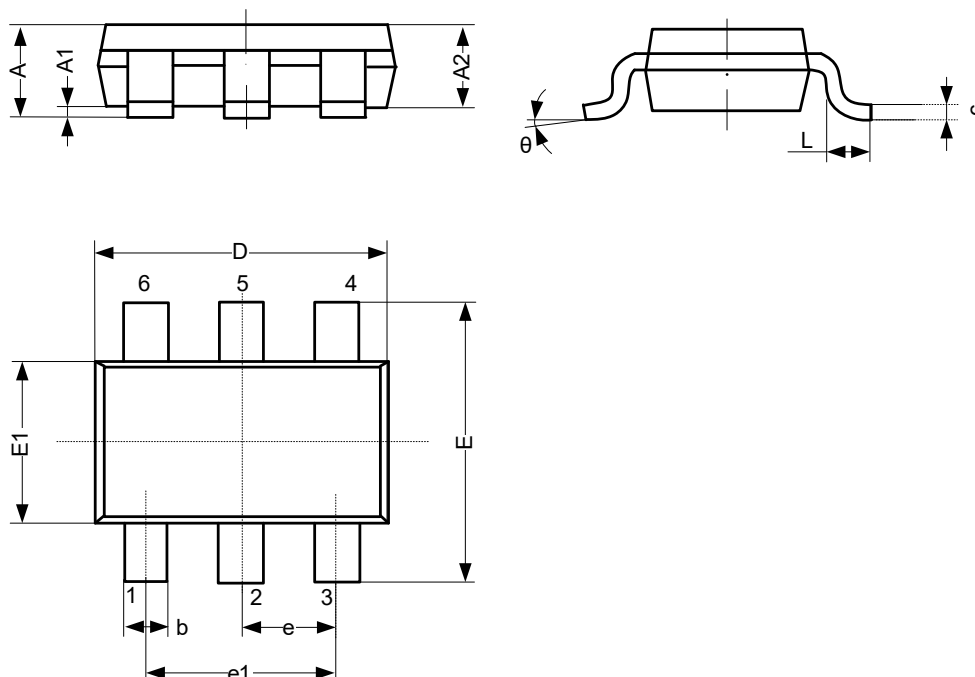
8.4.4 Test Data

SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PZL}, t_{PLZ}
1.65V to 1.95V	V_{CC}	$\leq 3ns$	30pF	1k Ω	$2 \times V_{CC}$
2.3V to 2.7V	V_{CC}	$\leq 3ns$	30pF	500 Ω	$2 \times V_{CC}$
2.7V	2.7V	$\leq 3ns$	50pF	500 Ω	6V
3.0V to 3.6V	2.7V	$\leq 3ns$	50pF	500 Ω	6V
4.5V to 5.5V	V_{CC}	$\leq 3ns$	50pF	500 Ω	$2 \times V_{CC}$

9 Mechanical Information

9.1 SOT-23-6L Mechanical Information

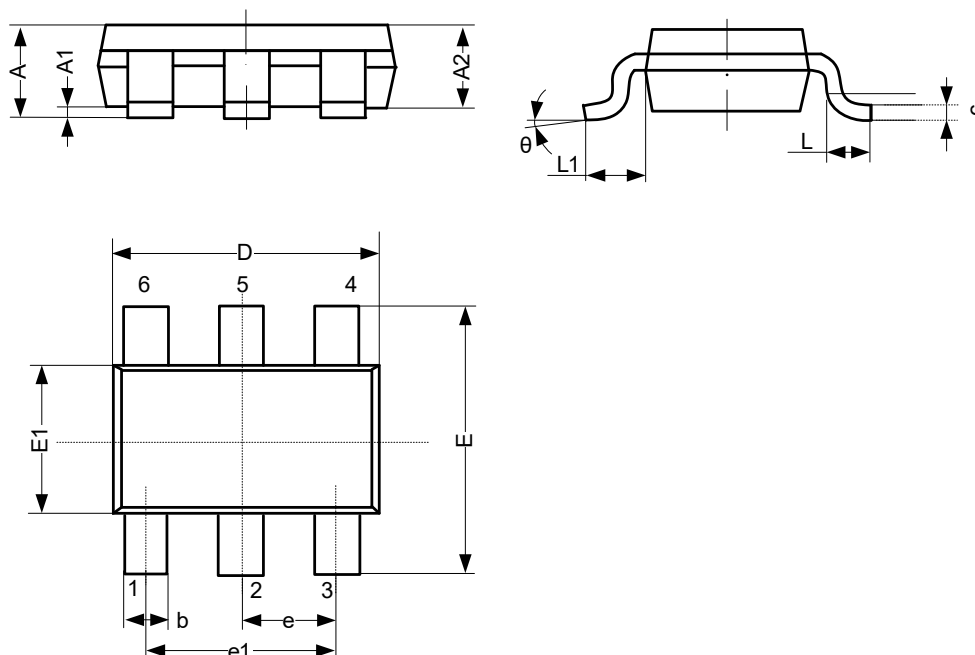
9.1.1 SOT-23-6L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.25
A1	0.00	-	0.12
A2	1.00	-	1.20
b	0.30	-	0.50
c	0.10	-	0.20
D	2.82	-	3.02
E	2.60	-	3.00
E1	1.50	-	1.70
e	0.95 BSC		
e1	1.80	-	2.00
L	0.30	-	0.60
θ	0°	-	8°
Unit: mm			

9.2 SOT-363 Mechanical Information

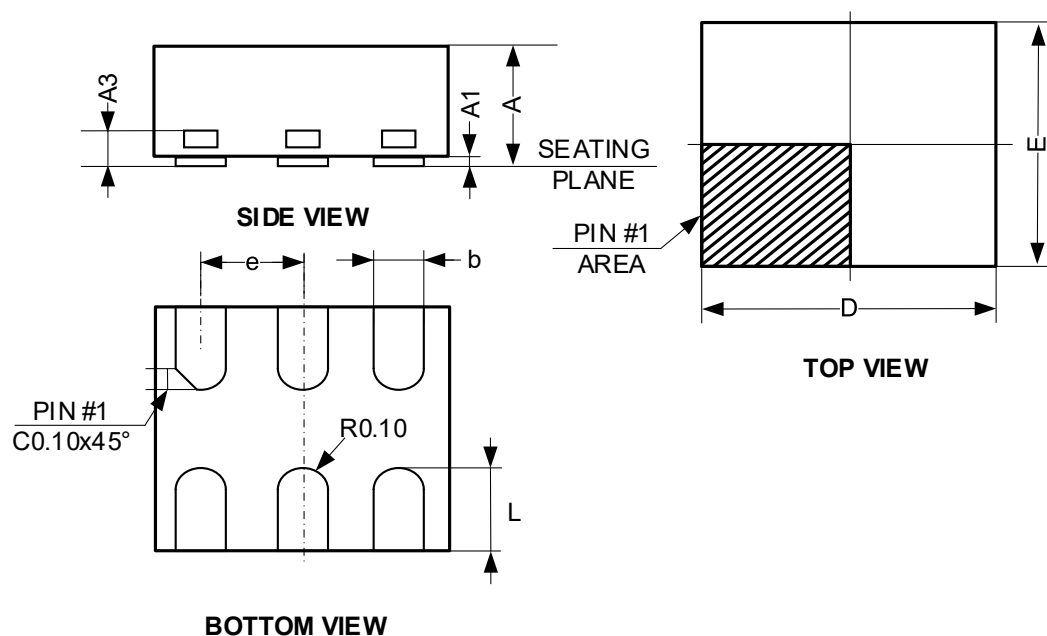
9.2.1 SOT-363 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.90	-	1.10
A1	0.00	-	0.10
A2	0.90	-	1.00
b	0.15	-	0.35
c	0.11	-	0.175
D	2.00	-	2.20
E	2.15	-	2.45
E1	1.15	-	1.35
e	0.65 BSC		
e1	1.20	-	1.40
L	0.26	-	0.46
L1	-	0.525	-
θ	0°	-	8°
Unit: mm			

9.3 DFN1.45x1-6L Mechanical Information

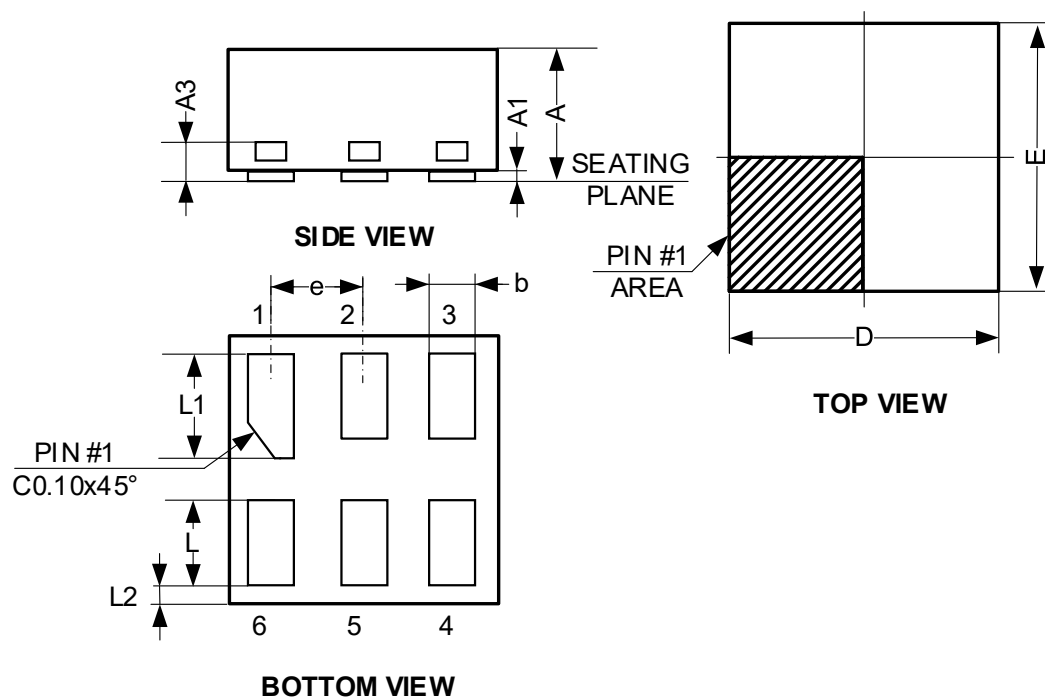
9.3.1 DFN1.45x1-6L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.51	-	0.60
A1	0.00	-	0.05
A3	-	0.15	-
b	0.15	-	0.25
D	-	1.45	-
E	-	1.00	-
e	0.50 BSC		
L	0.25	-	0.45
Unit: mm			

9.4 DFN1x1-6L Mechanical Information

9.4.1 DFN1x1-6L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.41	-	0.50
A1	0.00	-	0.05
A3	-	0.127	-
b	0.11	-	0.21
D	-	1.00	-
E	-	1.00	-
e	0.35 BSC		
L	0.26	-	0.36
L1	0.31	-	0.41
L2	0.02	-	0.12
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- <https://www.jscj-elec.com> for more details.

10.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

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