

**Quad 2-input AND Gate****CJ74LVC08** Logic**1 Introduction**

The CJ74LVC08 provides four 2-input AND gates.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in mixed 3.3V and 5V applications.

2 Available Packages

PART NUMBER	PACKAGE
CJ74LVC08	SOP14
	TSSOP14
	QFN3.5x3.5-14L

Note: For all available packages, please refer to the part Orderable Information.

3 Features

- 5V tolerant inputs for interfacing with 5V logic
- Wide supply voltage range from 1.2V to 3.6V
- CMOS low power consumption
- Direct interface with TTL levels
- Specified from -40°C to +125°C

4 Applications

- Servers
- LED Displays
- Network Switches
- I/O Expanders
- Base Station Processor Board



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74LVC08ADN	SOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74LVC08BDN	TSSOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active
CJ74LVC08QIN	QFN3.5x3.5-14L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

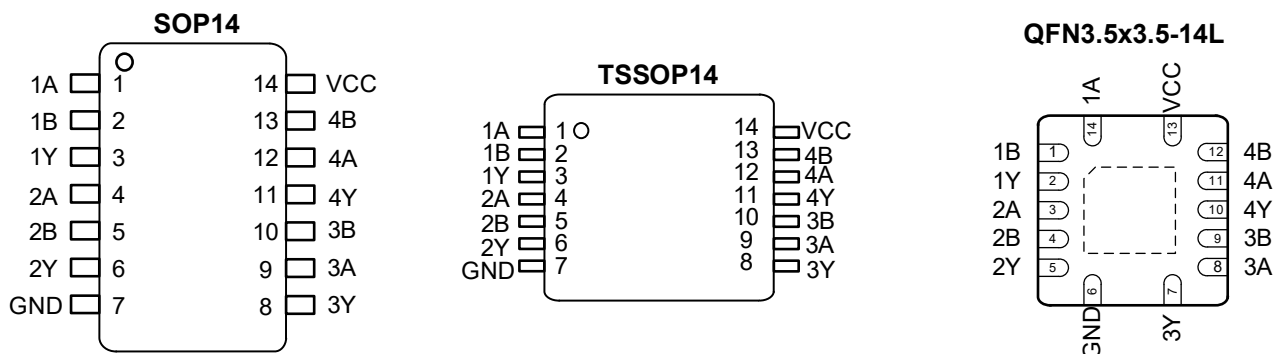


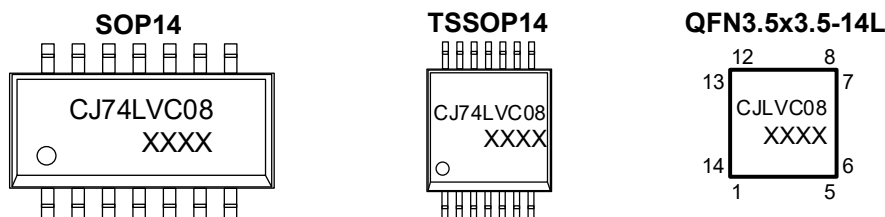
Figure 6-1 Pin configuration

6.2 Pin Function

PIN		NAME	I/O ⁽¹⁾	DESCRIPTION
No.				
SOP14/TSSOP14	QFN3.5x3.5-14L			
1	14	1A	I	Data input
2	1	1B	I	Data input
3	2	1Y	O	Data output
4	3	2A	I	Data input
5	4	2B	I	Data input
6	5	2Y	O	Data output
7	6	GND	G	Ground (0V)
8	7	3Y	O	Data output
9	8	3A	I	Data input
10	9	3B	I	Data input
11	10	4Y	O	Data output
12	11	4A	I	Data input
13	12	4B	I	Data input
14	13	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-	-0.5	+6.5	V
I_{IK}	Input clamping current	$V_I < 0V$	-50	-	mA
V_I	Input voltage	-	-0.5	+6.5	V
I_{OK}	Output clamping current	$V_O > V_{CC}$ or $V_O < 0V$	-	± 50	mA
V_O	Output voltage	Output in HIGH or LOW-state	-0.5	$V_{CC}+0.5$	V
I_O	Output current	$V_O=0V$ to V_{CC}	-	± 50	mA
I_{CC}	Supply current	-	-	100	mA
I_{GND}	Ground current	-	-100	-	mA
P_{tot}	Total power dissipation	-	-	500	mW
T_{stg}	Storage temperature	-	-65	+150	°C
T_L	Soldering Temperature	10s	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage	-	1.65	-	3.6	V
		Functional	1.2	-	-	V
V_I	Input voltage	-	0	-	5.5	V
V_O	Output voltage	Output HIGH or LOW state	0	-	V_{CC}	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C
$\Delta t/\Delta V$	Input transition rise and fall rate	$V_{CC}=1.65V$ to $2.7V$	0	-	20	ns/V
		$V_{CC}=2.7V$ to $3.6V$	0	-	10	ns/V

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) ⁽¹⁾	± 4000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V _{IH}	HIGH-level input voltage	V _{CC} =1.2V		1.08	-	-	V
		V _{CC} =1.65V to 1.95V		0.65xV _{CC}	-	-	V
		V _{CC} =2.3V to 2.7V		1.7	-	-	V
		V _{CC} =2.7V to 3.6V		2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} =1.2V		-	-	0.12	V
		V _{CC} =1.65V to 1.95V		-	-	0.35xV _{CC}	V
		V _{CC} =2.3V to 2.7V		-	-	0.7	V
		V _{CC} =2.7V to 3.6V		-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}	I _O =-100uA; V _{CC} =1.65V to 3.6V	V _{CC} -0.2	-	-	V
			I _O =-4mA; V _{CC} =1.65V	1.2	-	-	V
			I _O =-8mA; V _{CC} =2.3V	1.8	-	-	V
			I _O =-12mA; V _{CC} =2.7V	2.2	-	-	V
			I _O =-18mA; V _{CC} =3.0V	2.4	-	-	V
			I _O =-24mA; V _{CC} =3.0V	2.2	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}	I _O =100uA; V _{CC} =1.65V to 3.6V	-	-	0.2	V
			I _O =4mA; V _{CC} =1.65V	-	-	0.45	V
			I _O =8mA; V _{CC} =2.3V	-	-	0.6	V
			I _O =12mA; V _{CC} =2.7V	-	-	0.4	V
			I _O =24mA; V _{CC} =3.0V	-	-	0.55	V
I _I	Input leakage current	V _I =5.5V or GND; V _{CC} =3.6V		-	-	±5	uA
I _{CC}	Supply current	V _I =V _{CC} or GND; I _O =0A; V _{CC} =3.6V		-	-	15	uA
ΔI _{CC}	Additional supply current	Per input pin; V _I =V _{CC} -0.6V; I _O =0A; V _{CC} =2.7V to 3.6V		-	-	500	uA
C _I	Input capacitance	V _{CC} =0V to 3.6V; V _I = GND to V _{CC}		-	4.0	-	pF

Note: All typical values are measured at $V_{CC}=3.3\text{V}$ (unless stated otherwise) and $T_{amb}=25^{\circ}\text{C}$.

7.4.2 DC Characteristics 2

$T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	$V_{CC}=1.2\text{V}$		1.08	-	-	V
		$V_{CC}=1.65\text{V}$ to 1.95V		$0.65 \times V_{CC}$	-	-	V
		$V_{CC}=2.3\text{V}$ to 2.7V		1.7	-	-	V
		$V_{CC}=2.7\text{V}$ to 3.6V		2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC}=1.2\text{V}$		-	-	0.12	V
		$V_{CC}=1.65\text{V}$ to 1.95V		-	-	$0.35 \times V_{CC}$	V
		$V_{CC}=2.3\text{V}$ to 2.7V		-	-	0.7	V
		$V_{CC}=2.7\text{V}$ to 3.6V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_O = -100\mu\text{A}; V_{CC}=1.65\text{V}$ to 3.6V	$V_{CC}-0.3$	-	-	V
			$I_O = -4\text{mA}; V_{CC}=1.65\text{V}$	1.05	-	-	V
			$I_O = -8\text{mA}; V_{CC}=2.3\text{V}$	1.65	-	-	V
			$I_O = -12\text{mA}; V_{CC}=2.7\text{V}$	2.05	-	-	V
			$I_O = -18\text{mA}; V_{CC}=3.0\text{V}$	2.25	-	-	V
			$I_O = -24\text{mA}; V_{CC}=3.0\text{V}$	2.0	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_O = 100\mu\text{A}; V_{CC}=1.65\text{V}$ to 3.6V	-	-	0.3	V
			$I_O = 4\text{mA}; V_{CC}=1.65\text{V}$	-	-	0.65	V
			$I_O = 8\text{mA}; V_{CC}=2.3\text{V}$	-	-	0.8	V
			$I_O = 12\text{mA}; V_{CC}=2.7\text{V}$	-	-	0.6	V
			$I_O = 24\text{mA}; V_{CC}=3.0\text{V}$	-	-	0.8	V
I_I	Input leakage current	$V_I = 5.5\text{V}$ or GND; $V_{CC}=3.6\text{V}$		-	-	± 20	μA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{A}; V_{CC}=3.6\text{V}$		-	-	200	μA
ΔI_{CC}	Additional supply current	Per input pin; $V_I = V_{CC}-0.6\text{V}; I_O = 0\text{A}; V_{CC}=2.7\text{V}$ to 3.6V		-	-	5000	μA

Note: All typical values are measured at $V_{CC}=3.3\text{V}$ (unless stated otherwise) and $T_{amb}=25^{\circ}\text{C}$.

7.4.3 AC Characteristics 1

T_{amb}=−40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t _{pd}	nA, nB to nY propagation delay	See Figure 8-5	V _{CC} =1.2V	-	11.0	-	ns
			V _{CC} =1.65V to 1.95V	0.5	4.2	9.0	ns
			V _{CC} =2.3V to 2.7V	1.0	2.5	6.9	ns
			V _{CC} =2.7V	1.5	2.5	4.8	ns
			V _{CC} =3.0V to 3.6V	1.0	2.3	4.1	ns
t _{sk(o)}	Output skew time	V _{CC} =3.0V to 3.6V		-	-	1.0	ns
C _{PD}	Power dissipation capacitance	Per gate; V _I = GND to V _{CC}	V _{CC} =1.65V to 1.95V	-	4.4	-	pF
			V _{CC} =2.3V to 2.7V	-	7.7	-	pF
			V _{CC} =3.0V to 3.6V	-	10.5	-	pF

Note:

- (1) Typical values are measured at T_{amb}=25°C and V_{CC}=1.2V, 1.8V, 2.5V, 2.7V and 3.3V respectively.
- (2) t_{pd} is the same as t_{PLH} and t_{PHL}.
- (3) Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- (4) C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$$P_D = (C_{PD} \times V_{CC}^2 \times f_i \times N) + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

∑(C_L×V_{CC}²×f_o)=sum of outputs.

7.4.4 AC Characteristics 2

T_{amb}=−40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t _{pd}	nA, nB to nY propagation delay	See Figure 8-5	V _{CC} =1.65V to 1.95V	0.5	-	10.4	ns
			V _{CC} =2.3V to 2.7V	1.0	-	8.0	ns
			V _{CC} =2.7V	1.5	-	5.6	ns
			V _{CC} =3.0V to 3.6V	1.0	-	4.8	ns
t _{sk(o)}	Output skew time	V _{CC} =3.0V to 3.6V		-	-	1.5	ns

Note:

- (1) Typical values are measured at T_{amb}=25°C and V_{CC}=1.2V, 1.8V, 2.5V, 2.7V and 3.3V respectively.
- (2) t_{pd} is the same as t_{PLH} and t_{PHL}.
- (3) Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

8 Detailed Description

8.1 Overview

The CJ74LVC08 provides four 2-input AND gates.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in mixed 3.3V and 5V applications.

8.2 Functional Block Diagram

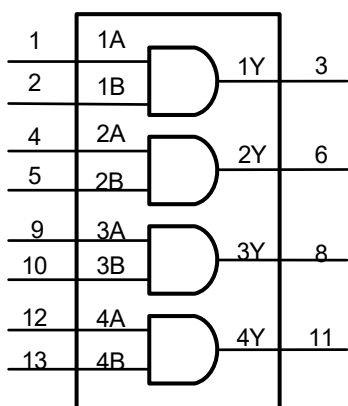


Figure 8-1 Logic symbol

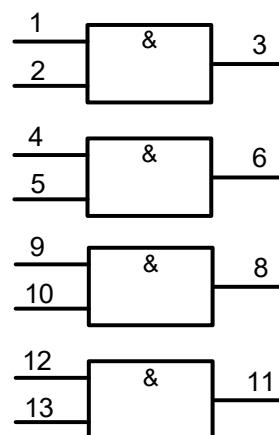


Figure 8-2 IEC Logic symbol

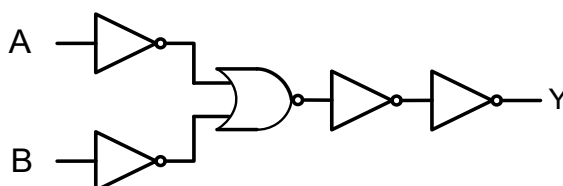


Figure 8-3 Logic diagram for one gate

8.3 Function Table

INPUT		OUTPUT
nA	nB	nY
L	X	L
X	L	L
H	H	H

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

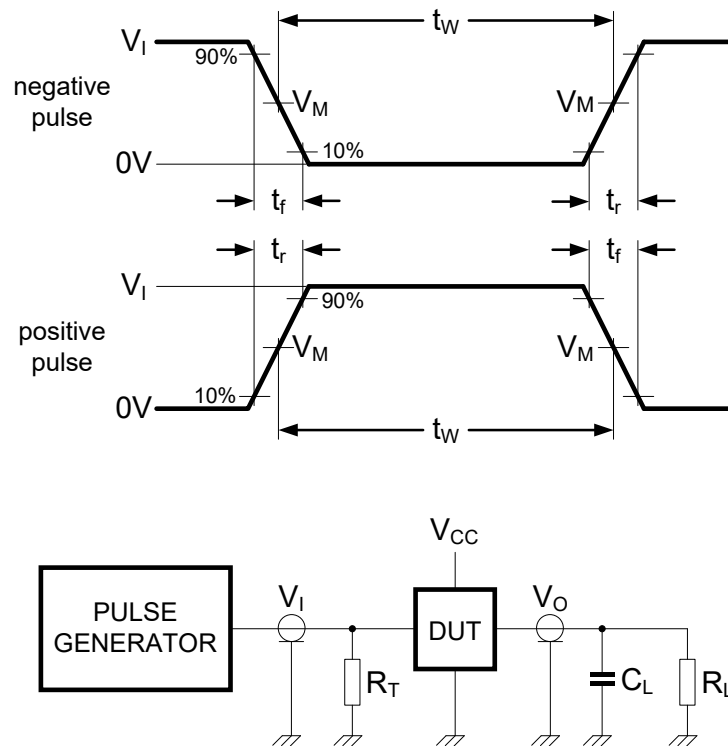


Figure 8-4 Test circuit for measuring switching times

Definitions for test circuit:

R_L =Load resistance.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

8.4.2 AC Testing Waveforms

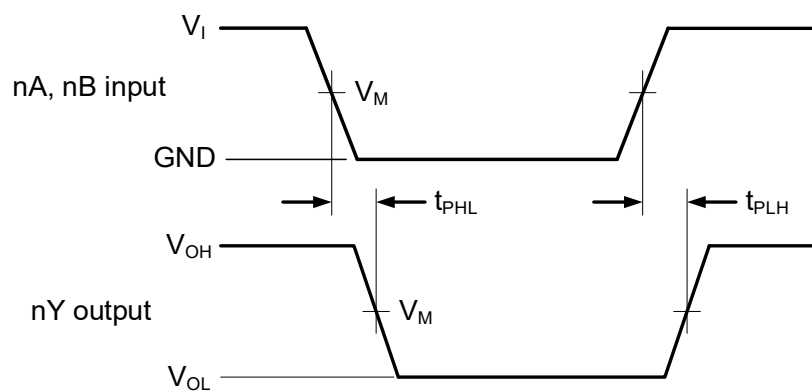


Figure 8-5. The input (nA, nB) to output (nY) propagation delays

8.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{CC}	V_M	V_M
$< 2.7V$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
$\geq 2.7V$	$1.5V$	$1.5V$

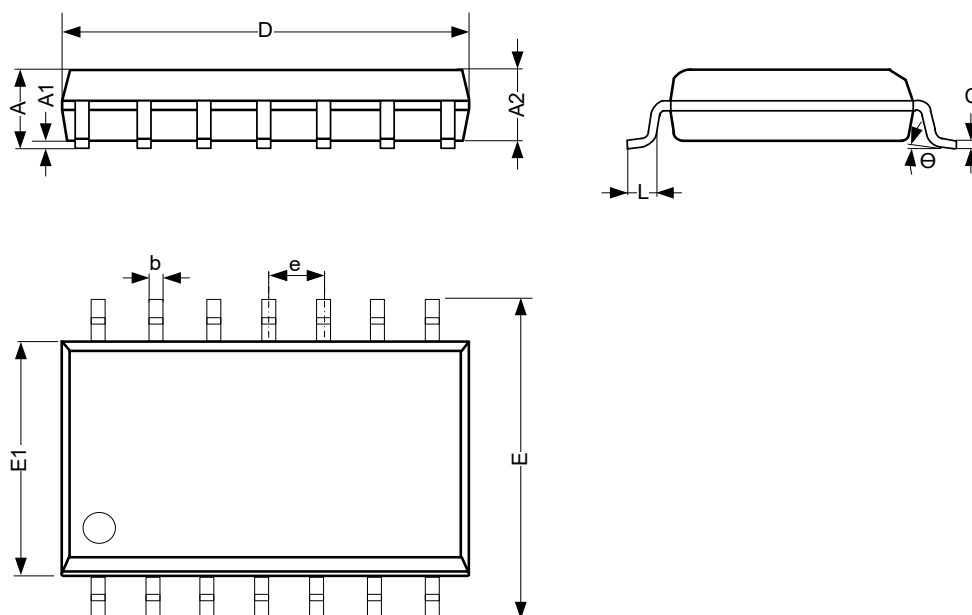
8.4.4 Test Data

SUPPLY VOLTAGE	INPUT		LOAD	
V_{CC}	V_I	t_r, t_f	C_L	R_L
1.2V	V_{CC}	$\leq 2.0ns$	30pF	1k Ω
1.65V to 1.95V	V_{CC}	$\leq 2.0ns$	30pF	1k Ω
2.3V to 2.7V	V_{CC}	$\leq 2.0ns$	30pF	500 Ω
2.7V	2.7V	$\leq 2.5ns$	50pF	500 Ω
3.0V to 3.6V	2.7V	$\leq 2.5ns$	50pF	500 Ω

9 Mechanical Information

9.1 SOP14 Mechanical Information

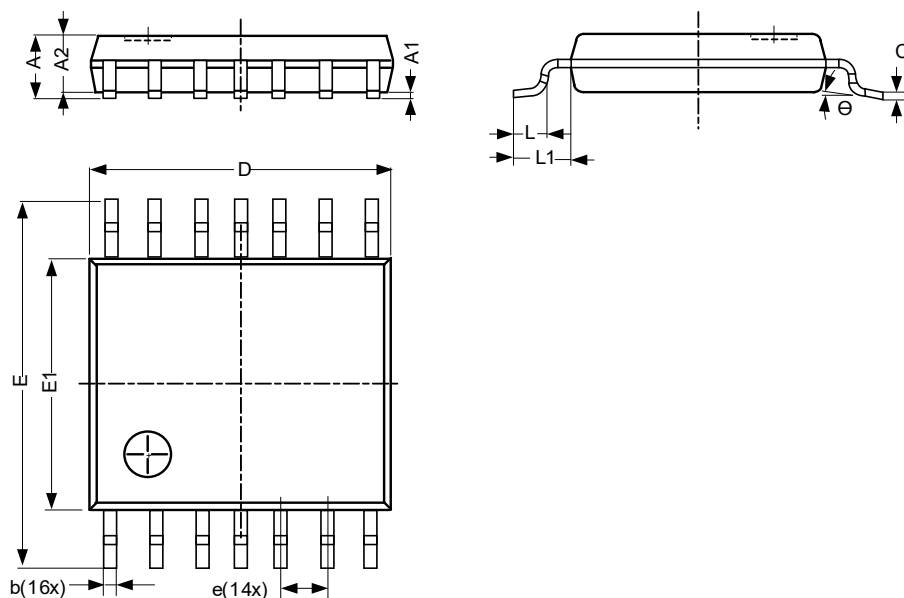
9.1.1 SOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.50	-	1.75
A1	0.05	-	0.25
A2	1.30	-	-
b	0.33	-	0.50
c	0.19	-	0.25
D	8.43	-	8.76
E	5.80	-	6.25
E1	3.75	-	4.00
e	1.27 BSC		
L	0.40	-	0.89
θ	0°	-	8°
Unit: mm			

9.2 TSSOP14 Mechanical Information

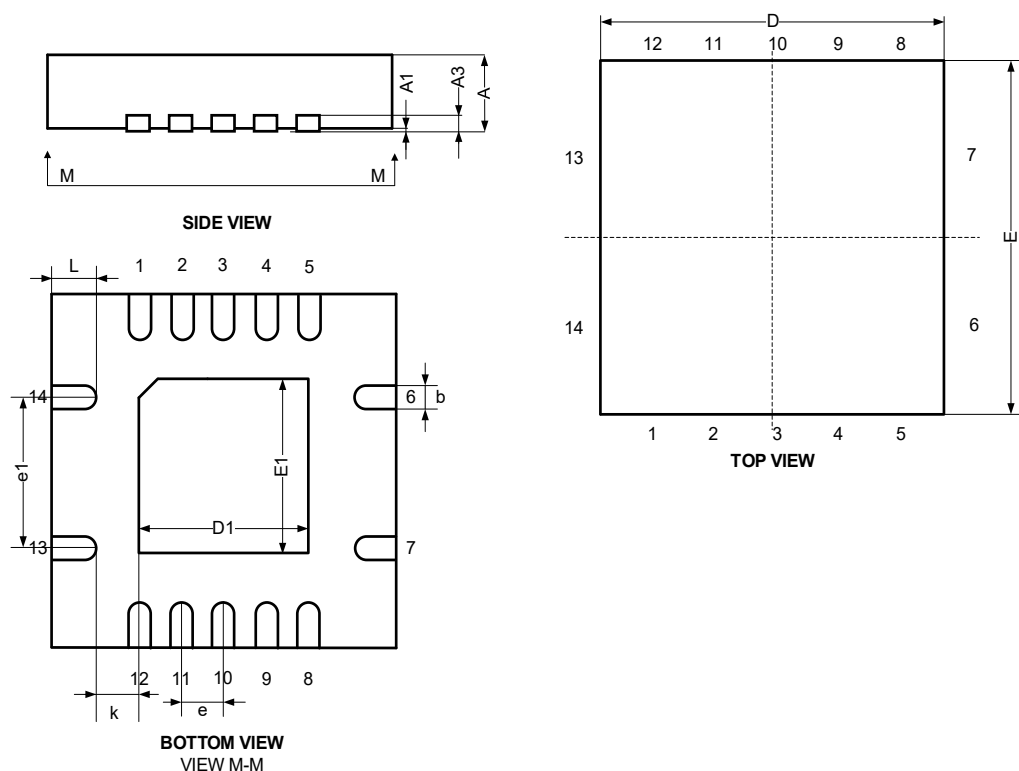
9.2.1 TSSOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
θ	0°	-	8°
Unit: mm			

9.3 QFN3.5x3.5-14L Mechanical Information

9.3.1 QFN3.5x3.5-14L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.70	-	0.90
A1	0	-	0.05
A3	0.203 REF		
D	3.424	-	3.576
E	3.424	-	3.576
D1	1.95	-	2.15
E1	1.95	-	2.15
k	0.20	-	-
b	0.20	-	0.30
e	0.50 BSC		
e1	1.50 BSC		
L	0.324	-	0.476
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- <https://www.jscj-elec.com> for more details.

10.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

August, 2025: rev - 1.1, Correct symbol from V_{OL} to I_I in 7.4.2.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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