NuMicro® Family

1T 8051-based Microcontroller

CM1003 Series

CM1003BF2AE

CM1003BF3AE

CM1003CF2AE

CM1003CF3AE

Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 GENERAL DESCRIPTION

The NuMicro CM1003 series is an embedded Flash type 1T 8051-based microcontroller. The instruction set is fully compatible with the standard 80C51 and performance enhanced. It supports 16/24 MHz core speed and features up to 32 Kbytes Flash memory, 256 Bytes of RAM and 1 Kbyte of auxiliary RAM (XRAM), 4 Kbytes of Flash loader memory (LDROM), 2.4V to 5.5V operating voltage, and -40°C to +105°C operating temperature.

The CM1003 series also provides plenty of peripherals including two 16-bit Timers, one 16-bit Timer with three-channel input capture mode, one Watchdog Timer, one Self Wake-up Timer, one 16-bit auto-reload Timer3 for general purpose or baud rate generator, two UARTs with frame error detection and automatic address recognition, one set of SPI, one set of I^2C, six enhanced PWM output channels, eight-channel shared pin interrupt for all I/O, and eight-channel of 12-bit 500 kSPS ADC.

Supported small form factor packages include two types, TSSOP 20-pin and QFN 20-pin.

For the development, Nuvoton provides the NuMaker evaluation board and Nuvoton Nu-Link debugger. The 3rd Party IDE such as Keil C51, IAR EW8051, and NuEclipse SDCC compilers are also supported.

Product Line	UART	I^2C	SPI	Timer	PWM	ADC
CM1003BF2AE CM1003BF3AE CM1003CF2AE CM1003CF3AE	2	1	1	4	6	8

Table 1-1 NuMicro CM1003 Series Key Features Support Table

The CM1003 series is suitable for a wide range of applications such as:

- Home appliances
- LED lighting controls
- Motor controls
- Industrial automation

2 FEATURES

Core and System	
8051	• Fully static design 8-bit high performance 1T 8051-based CMOS microcontroller. • Instruction set fully compatible with MCS-51. • 4-priority-level interrupts capability. • Dual Data Pointers (DPTRs).
Power On Reset (POR)	• POR with 1.15V threshold voltage level
Brown-out Detector (BOD)	• 4-level selection, with brown-out interrupt and reset option. (4.4V / 3.7V / 2.7V / 2.2V)
Low Voltage Reset (LVR)	• LVR with 2.0V threshold voltage level
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID) • 128-bytes security protection memory SPROM (only for 32KB/16KB APROM)
Memories	
Flash	• 16/32 KBytes of APROM for User Code. • 4/3/2/1 Kbytes of Flash for loader (LDROM) configure from APROM for In-System-Programmable (ISP) • Flash Memory accumulated with pages of 128 Bytes from APROM by In-Application-Programmable (IAP) means whole APROM can be use as Data Flash • An additional 128 bytes security protection memory SPROM • Code lock for security by CONFIG
SRAM	• 256 Bytes on-chip RAM. • Additional 1 KBytes on-chip auxiliary RAM (XRAM) accessed by MOVX instruction.
Clocks	
Internal Clock Source	• Default 16 MHz high-speed internal oscillator (HIRC) trimmed to ±1% (accuracy at 25 °C, 3.3 V), ±2% in -20~+105°C, ±4% in -40~+105°C • Selectable 24 MHz high-speed internal oscillator (HIRC) trimmed to ±1% (accuracy at 25 °C, 3.3 V) switch by software • 10 kHz low-speed internal oscillator (LIRC) calibrating to ±10% typically.

Timers	
16-bit Timer	• Two 16-bit Timers/Counters 0 and 1 compatible with standard 8051. • One 16-bit Timer2 with three-channel input capture module and 9 input pin can be selected. • One 16-bit auto-reload Timer3, which can be the baud rate clock source of UART0 and UART1.
Watchdog	• 6-bit free running up counter for WDT time-out interval. • Selectable time-out interval is 6.40 ms ~ 1.638s since WDT_CLK = 10 kHz (LIRC). • Able to wake up from Power-down or Idle mode • Interrupt or reset selectable on watchdog time-out
Wake-up Timer	• 16-bit free running up counter for time-out interval. • Clock sources from LIRC • Able self Wake-up wake up from Power-down or Idle mode, and auto reload count value. • Supports Interrupt
PWM	• Up To 6 output pins can be selected • Supports maximum clock source frequency up to 24 MHz • Supports independent mode for PWM output • Supports complementary mode for 3 complementary paired PWM output channels • Supports 16-bit resolution PWM counter • Supports mask function and tri-state enable for each PWM pin • PWM0 module support Dead-time insertion with 8-bit resolution • PWM0 module Supports brake function • PWM0 module Supports trigger ADC on the following events
Analog Interfaces	
Analog-to-Digital Converter (ADC)	• Analog input voltage range: 0 ~ AV_{DD}. • 12-bit resolution and 10-bit accuracy is guaranteed. • Up to 8 single-end analog input channels • 1 internal channel, it is band-gap voltage (VBG). • Up to 500 KSPS sampling rate. • Software trigger 1 to ADCS bit. • External pin (STADC) trigger • PWM trigger.

Communication Interfaces	
UART	• Supports up to 2 UARTs: UART0 & UART1 • Full-duplex asynchronous communications • Supports programmable 9th bit. • Supports TXD and RXD of UART0 pins exchangeable via software.
I²C	• 1 set of I²C device • Supports Master/Slave mode • Bidirectional data transfer between masters and slaves • 7-bit addressing mode • Supports standard mode (100 kbps) and Fast mode (400 kbps). • Supports 8-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows • Supports hold time programmable
SPI	• 1 set of SPI device • Supports Master or Slave mode operation • Supports MSB first or LSB first transfer sequence • Slave mode up to 12 MHz
GPIO	• Four I/O modes: – Quasi-bidirectional mode – Push-Pull output mode – Open-Drain output mode – Input only with high impendence mode • Schmitt trigger input / TTL mode selectable. • Each I/O pin configured as interrupt source with edge/level trigger setting • Standard interrupt pins INT0 and INT1. • Supports high drive and high sink current I/O • Maximum I/O Speed is 12 MHz • Supports wake-up function
ESD & EFT	
ESD	• HBM ± 7 kV
EFT	• ± 4.4 kV
Latch-up	• ± 200 mA

3 PARTS INFORMATION

3.1 CM1003 Series Package Type

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

	TSSOP20	QFN20
Part No.	CM1003BF2AE CM1003CF2AE	CM1003BF3AE CM1003CF3AE

3.2 CM1003 Series Naming Rule

C	M	1	003	B	F2	A	E
NTNJ	**Product**	**Core**	**Series**	**Flash**	**Package**	**Reserve**	**Temperature**
C	MCU	1:1T 8051	003	B: 16 KB C: 32 KB	F2: TSSOP20 (4.4x6.5 mm) F3: QFN20 (3x3 mm)		E:-40°C to +105°C

3.3 CM1003 Series Selection Gude

Part Number	Flash (KB)	SRAM (B)	LDROM (KB) [1]	I/O	Timer	PWM	Connectivity				ADC(12-Bit)	Package
							ISO 7816-3 [2]	UART	SPI	I2C		
CM1003BF3AE	16	1K+256	4	18	4	6	-	2	1	1	8-ch	QFN20
CM1003BF2AE	16	1K+256	4	18	4	6	-	2	1	1	8-ch	TSSOP20
CM1003CF3AE	32	1K+256	4	18	4	6	-	2	1	1	8-ch	QFN20
CM1003CF2AE	32	1K+256	4	18	4	6	-	2	1	1	8-ch	TSSOP20

Note:

1. ISP ROM programmable 1K/2K/3K/4KB Flash for user program loader (LDROM) share from ARPOM.
2. Detailed package information please refer to chapter 9 PACKAGE DIMENSIONS
3. This document is only for 16/32 KB Flash size part number product.

Table 3.3-1 Selection Guide

4 PIN CONFIGURATION

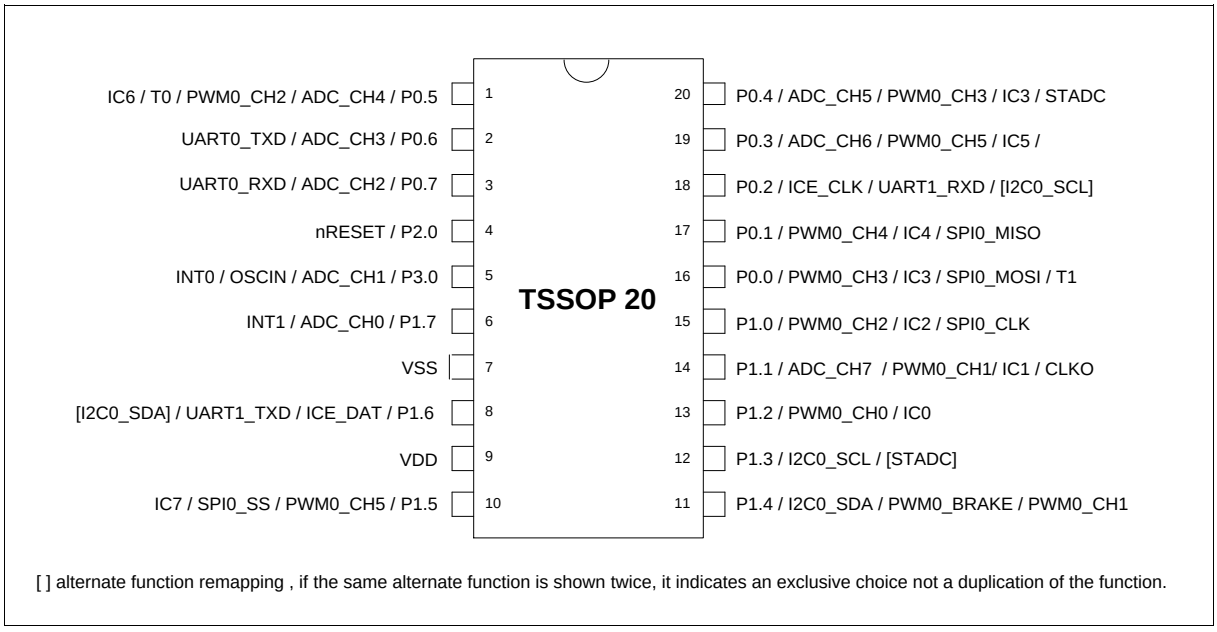
Users can find pin configuaration informations by using NuTool - PinConfigure. The NuTool - PinConfigure contains all Nuvoton NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1 CM1003 Series Pin Diagram

4.1.1 TSSOP 20-pin Package

Corresponding Part Number:

CM1003BF2AE, CM1003CF2AE



[ ] alternate function remapping , if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function.

Figure 4.1-1 Pin Assignment of TSSOP-20 Package

4.1.2 QFN 20-pin Package

Corresponding Part Number:

CM1003BF3AE, CM1003CF3AE

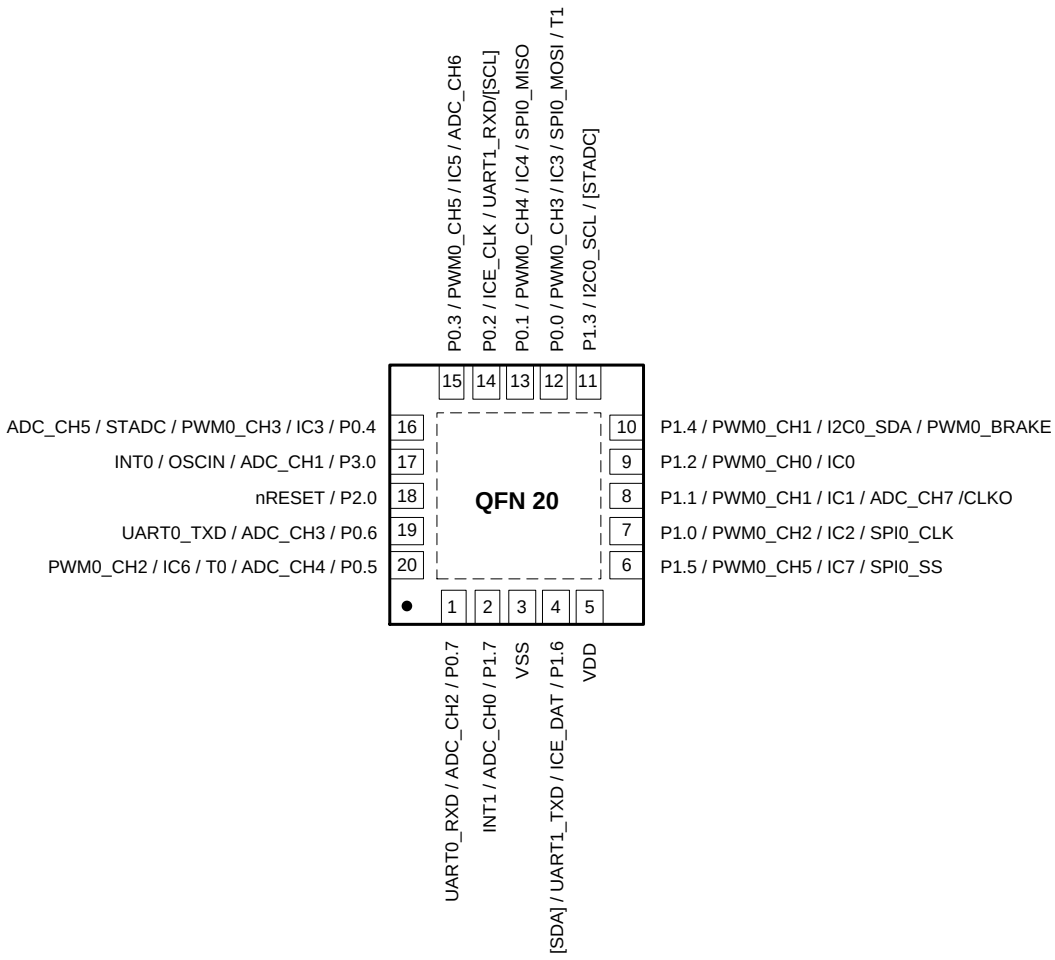


Figure 4.1-2 Pin Assignment of QFN-20 Package

4.2 CM1003 Pin Description

Pin Number		Symbol	Multi-Function Description[1]
CM1003BF2AE CM1003CF2AE	CM1003BF3AE CM1003CF3AE		
9	5	VDD	POWER SUPPLY: Supply voltage V_{DD} for operation.
7	3	VSS	GROUND: Ground potential.
16	12	P0.0	Port 0 bit 0.
		PWM0_CH3	PWM0 output channel 3.
		SPI0_MOSI	SPI master output/slave input.
		IC3	Input capture channel 3.
		T1	External count input to Timer/Counter 1 or its toggle output.
17	13	P0.1	Port 0 bit 1.
		PWM0_CH4	PWM0 output channel 4.
		IC4	Input capture channel 4.
		SPI0_MISO	SPI master input/slave output.
18	14	P0.2	Port 0 bit 2.
		ICE_CLK	ICP / OCD clock input.
		UART1_RXD	Serial port 1 receive input.
		[I2C0_SCL] [3]	I^2C clock.
19	15	P0.3	Port 0 bit 3.
		ADC_CH6	ADC input channel 6.
		PWM0_CH5	PWM0 output channel
		IC5	Input capture channel 5.
20	16	P0.4	Port 0 bit 4.
		PWM0_CH3	PWM0 output channel 3.
		IC3	Input capture channel 3.
		ADC_CH5	ADC input channel 5.
		STADC	External start ADC trigger
1	20	P0.5	Port 0 bit 5.
		PWM0_CH2	PWM0 output channel 2.
		IC6	Input capture channel 6.
		T0	External count input to Timer/Counter 0 or its toggle output.
		ADC_CH4	ADC input channel 5.
2	19	P0.6	Port 0 bit 6.
		UART0_TXD [2]	Serial port 0 transmit data output.

Pin Number		Symbol	Multi-Function Description[1]
CM1003BF2AE CM1003CF2AE	CM1003BF3AE CM1003CF3AE		
		ADC_CH3	ADC input channel 3.
3	1	P0.7	Port 0 bit 7.
		UART0_RXD	Serial port 0 receive input.
		ADC_CH2	ADC input channel 2.
15	7	P1.0	Port 1 bit 0.
		PWM0_CH2	PWM0 output channel 2.
		IC2	Input capture channel 2.
		SPI0_CLK	SPI clock.
14	8	P1.1	Port 1 bit 1
		PWM0_CH1	PWM0_CH1: PWM0 output channel 1.
		IC1	Input capture channel 1.
		ADC_CH7	ADC input channel 7.
		CLKO	System clock output.
13	9	P1.2	Port 1 bit 2.
		PWM0_CH0	PWM0 output channel 0.
		IC0	Input capture channel 0.
12	11	P1.3	Port 1 bit 3.
		I2C0_SCL	I^2C clock.
		[STADC] [4]	External start ADC trigger
11	10	P1.4	Port 1 bit 4.
		PWM0_CH1	PWM0 output channel 1.
		I2C0_SDA	I^2C data.
		PWM0_BRAKE	Fault Brake input.
10	6	P1.5	Port 1 bit 5.
		PWM0_CH5	PWM0 output channel 5.
		IC7	Input capture channel 7.
		SPI0_SS	SPI slave select input.
8	4	P1.6	P1.6: Port 1 bit 6.
		ICE_DAT	ICP / OCD data input or output.
		UART1_TXD/	Serial port 1 transmit data output.
		[I2C0_SDA] [3]	I^2C data.
6	2	P1.7	Port 1 bit 7.

Pin Number		Symbol	Multi-Function Description[1]
CM1003BF2AE CM1003CF2AE	CM1003BF3AE CM1003CF3AE		
		$\overline{INT1}$	External interrupt 1 input.
		ADC_CH0	ADC input channel 0.
4	18	P2.0/	Port 2 bit 0 input pin available when RPD (CONFIG0.2) is programmed as 0.
		nRESET	nRESET pin is a Schmitt trigger input pin for hardware device reset. A low on this pin resets the device. nRESETpin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
5	17	P3.0	Port 3 bit 0 available when the internal oscillator is used as the system clock.
		ADC_CH1	ADC input channel 1.
		$\overline{INT0}$	External interrupt 0 input.
		OSCIN	If the ECLK mode is enabled, Xin is the external clock input pin.

Note:

1. All I/O pins can be configured as a interrupt pin. This feature is not listed in multi-function description.
2. UART0_TXD and UART0_RXD pins are software exchangeable by UART0PX (AUXR1.2).
3. [I2C] alternate function remapping option. I^2C pins is software switched by I2CPX (I2CON.0).
4. [STADC] alternate function remapping option. STADC pin is software switched by STADCPX(ADCCON1.6).
5. PIOx register decides which pins are PWM or GPIO.

Table 4.2-1 Pin Description

5 BLOCK DIAGRAM

5.1 CM1003 Sereis Block Diagram

Figure 5.1-1 CM1003 Series Functional Block Diagram shows the CM1003 functional block diagram and gives the outline of the device. User can find all the peripheral functions of the device in the diagram.

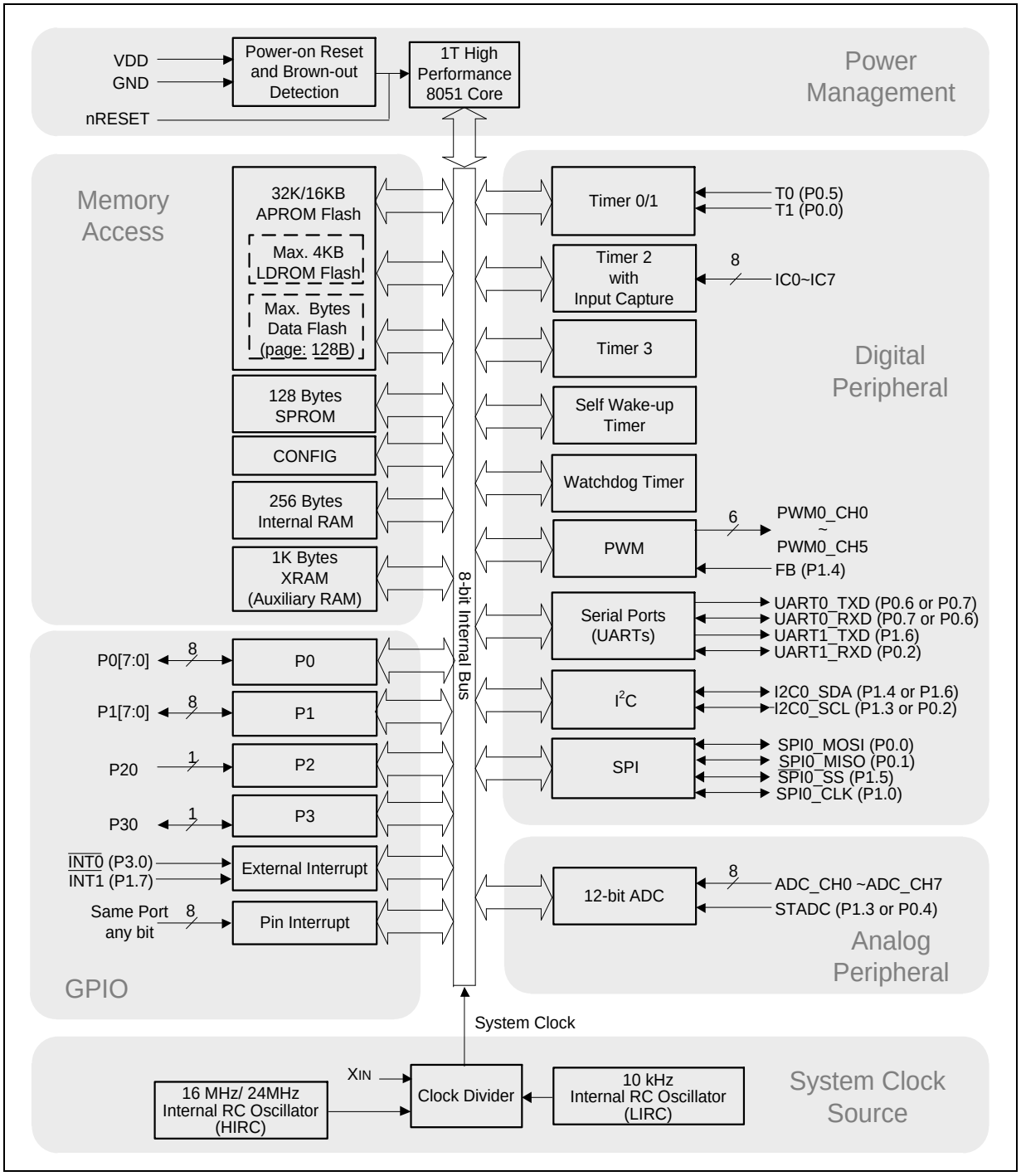


Figure 5.1-1 CM1003 Series Functional Block Diagram

6 FUNCTION DESCRIPTION

6.1 Memory Organization

A standard 80C51 based microcontroller divides the memory into two different sections, Program Memory and Data Memory. The Program Memory is used to store the instruction codes, whereas the Data Memory is used to store data or variations during the program execution.

The Data Memory occupies a separate address space from Program Memory. In CM1003, there are 256 Bytes of internal scratch-pad RAM. For many applications those need more internal RAM, the CM1003 provides another on-chip 1K Bytes of RAM, which is called XRAM, accessed by MOVX instruction.

The whole embedded flash, functioning as Program Memory, is divided into four blocks: Application ROM (APROM) normally for User Code, Loader ROM (LDROM) normally for Boot Code, Security protection ROM (SPROM) normally for Security Application, and CONFIG bytes for hardware initialization. Actually, APROM and LDROM function in the same way but have different size. Each block is accumulated page by page and the page size is 128 Bytes. The flash control unit supports Erase, Program, and Read modes. The external writer tools though specific I/O pins, In-Application-Programming (IAP), or In-System-Programming (ISP) can both perform these modes. The SPROM includes 128 bytes at location address FF80H ~ FFFFH and doesn't support "whole chip erase command". The last byte of SPROM (address: FFFFH) is used to identify the SPROM code is non-secured or secured mode.

6.2 System Manager

6.2.1 Clock System

The CM1003 has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. The CM1003 provides three options of the system clock sources including internal oscillator, or external clock from XIN pin via software. The CM1003 is embedded with two internal oscillators: one 10 kHz low-speed and one 16 MHz high-speed, which is factory trimmed to ±2% under all conditions. A clock divider CKDIV is also available on CM1003 for adjustment of the flexibility between power consumption and operating performance.

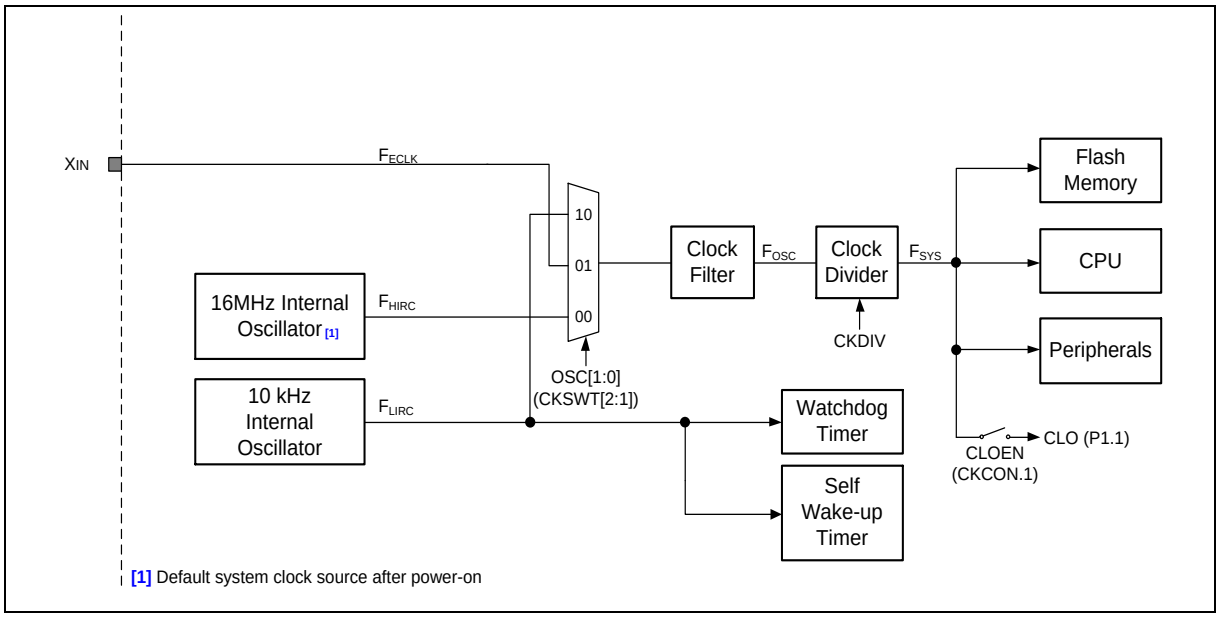


Figure 6.2-1 Clock System Block Diagram

6.3 Flash Memory Contorl

6.3.1 In-Application-Programming (IAP)

Unlike RAM's real-time operation, to update flash data often takes long time. Furthermore, it is a quite complex timing procedure to erase, program, or read flash data. The CM1003 carried out the flash operation with convenient mechanism to help user re-programming the flash content by In-Application-Programming (IAP). IAP is an in-circuit electrical erasure and programming method through software.

After IAP enabling by setting IAPEN (CHPCON.0 with TA protected) and setting the enable bit in IAPUEN that allows the target block to be updated, user can easily fill the 16-bit target address in IAPAH and IAPAL, data in IAPFD, and command in IAPCN. Then the IAP is ready to begin by setting a triggering bit IAPGO (IAPTRG.0). Note that IAPTRG is also TA protected. At this moment, the CPU holds the Program Counter and the built-in IAP automation takes over to control the internal charge-pump for high voltage and the detail signal timing. The erase and program time is internally controlled disregard of the operating voltage and frequency. Nominally, a page-erase time is 5 ms and a byte-program time is 23.5 μs. After IAP action completed, the Program Counter continues to run the following instructions. The IAPGO bit will be automatically cleared. An IAP failure flag, IAPFF (CHPCON.6), can be check whether the previous IAP operation was successful or not. Through this progress, user can easily erase, program, and verify the Flash Memory by just taking care of pure software.

6.4 General Purpose IO (GPIO)

6.4.1 GPIO Mode

The CM1003 has a maximum of 43 general purpose I/O pins which 40 bit-addressable general I/O pins grouped as 5 ports, P0 to P4, and 7 general I/O pins grouped as P5. Each port has its port control register (Px register). The writing and reading of a port control register have different meanings. A write to port control register sets the port output latch logic value, whereas a read gets the port pin logic state. These four modes are quasi-bidirectional (standard 8051 port structure), push-pull, input-only, and open-drain modes. Each port spends two special function registers PxM1 and PxM2 to select the I/O mode of port Px. The list below illustrates how to select the I/O mode of Px.n. Note that the default configuration of is input-only (high-impedance) after any reset.

PnM1.X[1]	PnM2.X[1]	I/O Type
0	0	Quasi-bidirectional
0	1	Push-pull
1	0	Input-only (high-impedance)
1	1	Open-drain
NOTE1: N = 0~5, x = 0~7		

Table 6.4-1 Configuration for Different I/O Modes

6.5 Timer

6.5.1 Timer/Counter 0 And 1

Timer/Counter 0 and 1 on CM1003 are two 16-bit Timers/Counters. Each of them has two 8-bit registers those form the 16-bit counting register. For Timer/Counter 0 they are TH0, the upper 8-bit register, and TL0, the lower 8-bit register. Similarly Timer/Counter 1 has two 8-bit registers, TH1 and TL1. TCON and TMOD can configure modes of Timer/Counter 0 and 1.

The Timer or Counter function is selected by the C/$\overline{T}$ bit in TMOD. Each Timer/Counter has its own selection bit. TMOD.2 selects the function for Timer/Counter 0 and TMOD.6 selects the function for Timer/Counter 1

When configured as a “Timer”, the timer counts the system clock cycles. The timer clock is 1/12 of the system clock (F_{SYS}) for standard 8051 capability or direct the system clock for enhancement, which is selected by T0M (CKCON.3) bit for Timer 0 and T1M (CKCON.4) bit for Timer 1. In the “Counter” mode, the countering register increases on the falling edge of the external input pin T0. If the sampled value is high in one clock cycle and low in the next, a valid 1-to-0 transition is recognized on T0 or T1 pin.

The Timers 0 and 1 can be configured to automatically to toggle output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. This function is enabled by control bits T0OE and T1OE in the CKCON register, and apply to Timer 0 and Timer 1 respectively. The port outputs will be logic 1 prior to the first timer overflow when this mode is turned on. In order for this mode to function, the C/$\overline{T}$ bit should be cleared selecting the system clock as the clock source for the timer.

Note that the TH0 (TH1) and TL0 (TL1) are accessed separately. It is strongly recommended that in mode 0 or 1, user should stop Timer temporally by clearing TR0 (TR1) bit before reading from or writing to TH0 (TH1) and TL0 (TL1). The free-running reading or writing may cause unpredictable result.

6.5.2 Timer2 And Input Capture

Timer 2 is a 16-bit up counter cascaded with TH2, the upper 8 bits register, and TL2, the lower 8 bit register. Equipped with RCMP2H and RCMP2L, Timer 2 can operate under compare mode and auto-reload mode selected by CM/$\overline{RL2}$ (T2CON.0). An 3-channel input capture module makes Timer 2 detect and measure the width or period of input pulses. The results of 3 input captures are stores in C0H and C0L, C1H and C1L, C2H and C2L individually. The clock source of Timer 2 is from the system clock pre-scaled by a clock divider with 8 different scales for wide field application. The clock is enabled when TR2 (T2CON.2) is 1, and disabled when TR2 is 0. The following registers are related to Timer 2 function.

6.5.3 Timer3

Timer 3 is implemented simply as a 16-bit auto-reload, up-counting timer. The user can select the pre-scale with T3PS[2:0] (T3CON[2:0]) and fill the reload value into RH3 and RL3 registers to determine its overflow rate. User then can set TR3 (T3CON.3) to start counting. When the counter rolls over FFFFH, TF3 (T3CON.4) is set as 1 and a reload is generated and causes the contents of the RH3 and RL3 registers to be reloaded into the internal 16-bit counter. If ET3 (EIE1.1) is set as 1, Timer 3 interrupt service routine will be served. TF3 is auto-cleared by hardware after entering its interrupt service routine.

6.6 Watchdog Timer (WDT)

6.6.1 Overview

The CM1003 provides one Watchdog Timer (WDT). It can be configured as a time-out reset timer to reset whole device. Once the device runs in an abnormal status or hangs up by outward interference, a WDT reset recover the system. It provides a system monitor, which improves the reliability of the system. Therefore, WDT is especially useful for system that is susceptible to noise, power glitches, or electrostatic discharge. The WDT also can be configured as a general purpose timer, of which the periodic interrupt serves as an event timer or a durational system supervisor in a monitoring system, which is able to operate during Idle or Power-down mode. WDTEN[3:0] (CONFIG4[7:4]) initialize the WDT to operate as a time-out reset timer or a general purpose timer.

6.7 Self Wake-Up Timer (WKT)

6.7.1 Overview

The CM1003 has a dedicated Self Wake-up Timer (WKT), which serves for a periodic wake-up timer in low power mode or for general purpose timer. WKT remains counting in Idle or Power-down mode. When WKT is being used as a wake-up timer, a start of WKT can occur just prior to entering a power management mode. WKT has one clock source, internal 10 kHz. Note that the system clock frequency must be twice over WKT clock. If WKT starts counting, the selected clock source will remain active once the device enters Idle or Power-down mode. Note that the selected clock source of WKT will not automatically enabled along with WKT configuration. User should manually enable the selected clock source and waiting for stability to ensure a proper operation.

The WKT is implemented simply as a 8-bit auto-reload, up-counting timer with pre-scale 1/1 to 1/2048 selected by WKPS[2:0] (WKCON[2:0]). User fills the reload value into RWK register to determine its overflow rate. The WKTR (WKCON.3) can be set to start counting. When the counter rolls over FFH, WKTF (WKCON.4) is set as 1 and a reload is generated and causes the contents of the RWK register to be reloaded into the internal 8-bit counter. If EWKT (EIE1.2) is set as 1, WKT interrupt service routine will be served.

6.8 Serial Port (UART0 & UART1)

6.8.1 Overview

The CM1003 includes two enhanced full duplex serial ports enhanced with automatic address recognition and framing error detection. As control bits of these two serial ports are implemented the same. Generally speaking, in the following contents, there will not be any reference to serial port 1, but only to serial port 0.

Each serial port supports one synchronous communication mode, Mode 0, and three modes of full duplex UART (Universal Asynchronous Receiver and Transmitter), Mode 1, 2, and 3. This means it can transmit and receive simultaneously. The serial port is also receiving-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. The receiving and transmitting registers are both accessed at SBUF. Writing to SBUF loads the transmitting register, and reading SBUF accesses a physically separate receiving register. There are four operation modes in serial port. In all four modes, transmission initiates by any instruction that uses SBUF as a destination register.

6.9 Serial Peripheral Interface (SPI)

6.9.1 Overview

The CM1003 provides two Serial Peripheral Interface (SPI) block to support high-speed serial communication. SPI is a full-duplex, high-speed, synchronous communication bus between microcontrollers or other peripheral devices such as serial EEPROM, LCD driver, or D/A converter. It provides either Master or Slave mode, high-speed rate up to $F_{SYS}/4$, transfer complete and write collision flag. For a multi-master system, SPI supports Master Mode Fault to protect a multi-master conflict.

6.10 Inter-Integrated Circuit (I^2C)

6.10.1 Overview

The CM1003 provides two Inter-Integrated Circuit (I^2C) bus to serves as an serial interface between the microcontrollers and the I^2C devices such as EEPROM, LCD module, temperature sensor, and so on. The I^2C bus used two wires design (a serial data line I2C0_SDA and a serial clock line I2C0_SCL) to transfer information between devices.

The I^2C bus uses bi-directional data transfer between masters and slaves. There is no central master and the multi-master system is allowed by arbitration between simultaneously transmitting masters. The serial clock synchronization allows devices with different bit rates to communicate via one serial bus. The I^2C bus supports four transfer modes including master transmitter, master receiver, slave receiver, and slave transmitter. The I^2C interface only supports 7-bit addressing mode. A special mode General Call is also available. The I^2C can meet both standard (up to 100kbps) and fast (up to 400k bps) speeds.

6.11 Pulse Width Modulated (PWM)

6.11.1 Overview

The PWM (Pulse Width Modulation) signal is a useful control solution in wide application field. It can used on motor driving, fan control, backlight brightness tuning, LED light dimming, or simulating as a simple digital to analog converter output through a low pass filter circuit.

The CM1003 PWM is especially designed for motor control by providing three pairs, maximum 16-bit resolution of PWM output with programmable period and duty. The architecture makes user easy to drive the one-phase or three-phase brushless DC motor (BLDC), or three-phase AC induction motor. Each of six PWM can be configured as one of independent mode, complementary mode, or synchronous mode. If the complementary mode is used, a programmable dead-time insertion is available to protect MOS turn-on simultaneously. The PWM waveform can be edge-aligned or center-aligned with variable interrupt points.

6.12 12-Bit Analog-To-Digital Converter (ADC)

6.12.1 Overview

The CM1003 is embedded with a 12-bit SAR ADC. The ADC (analog-to-digital converter) allows conversion of an analog input signal to a 12-bit binary representation of that signal. The CM1003 is selected as 8-channel inputs in single end mode. The internal band-gap voltage 0.814 V also can be the internal ADC input. The analog input, multiplexed into one sample and hold circuit, charges a sample and hold capacitor. The output of the sample and hold capacitor is the input into the converter. The converter then generates a digital result of this analog level via successive approximation and stores the result in the result registers.

7 APPLICATION CIRCUIT

7.1 Power Supply Scheme

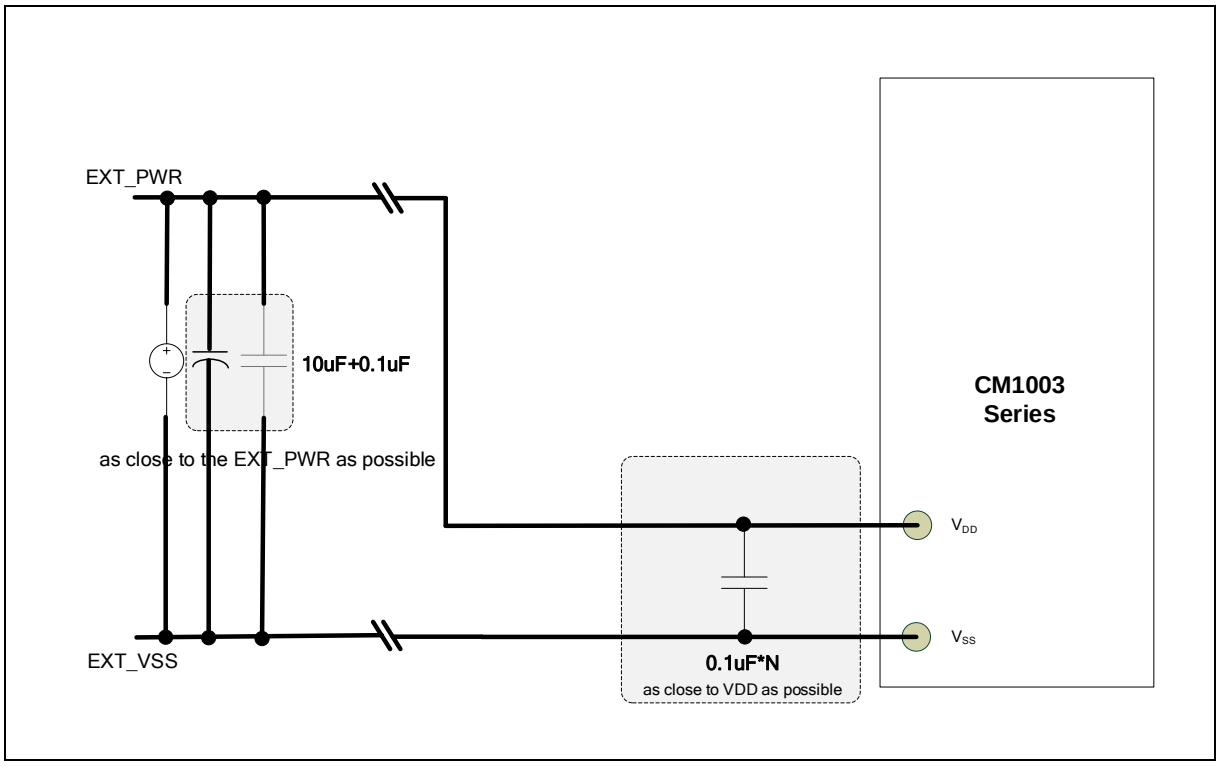
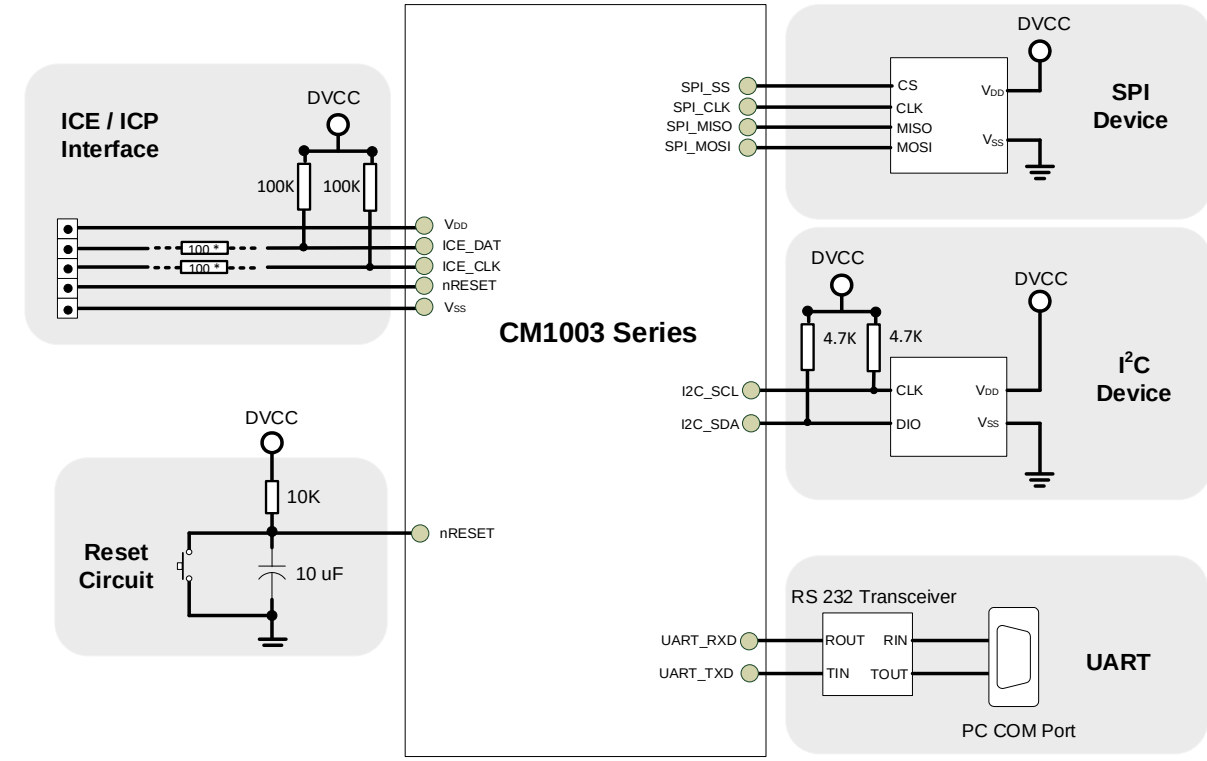


Figure 7.1-1 NuMicro® CM1003 Power Supply Circuit

7.2 Peripheral Application Scheme



Note 1: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 2: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

Note 3: It is optional add 100ohm series resistor between ICE_DAT/ICE_CLK and writer pin for filtering noise interference.

Figure 7.2-1 NuMicro® CM1003 Peripheral Interface Circuit

8 ELECTRICAL CHARACTERISTICS

8.1 General Operating Conditions

(V_{DD}-V_{SS} = 2.4 ~ 5.5V, T_A = 25°C, Fsys = 16 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{DD}	Operation voltage	2.4	-	5.5	V	
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{BG}[2]	Band-gap voltage[2]	1.17	1.22	1.30		T_A = 25 °C
		1.14		1.33		T_A = -40°C ~105 °C,
I_{RUSH}	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	150	200	mA	
E_{RUSH}	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	3.56	-	µC	V_{DD} = 2.4 V, T_A = 105 °C,

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. Based on characterization, tested in production.
3. The data presented in this table based on characterization, not tested in production unless otherwise specified.

Table 8.1-1 General Operating Conditions

8.2 DC Electrical Characteristics

8.2.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 2.4V ~ 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals clock base is the system clock Fsys.
- Program run “while (1);” in Flash.

Symbol	Conditions	Fsys	Typ [4]	Max[4]			Unit
			T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, all peripherals disable	24 MHz(HIRC)[1] @5.5V	2.6	2.8	2.7	2.9	mA
		24 MHz(HIRC)[1] @3.3V	2.5				
		24 MHz(HIRC)[1] @2.4V	2.3				
		16 MHz (HIRC) [1] @5.5V	2.0	2.4	2.3	2.6	
		16 MHz (HIRC) [1] @3.3V	1.9				
		16 MHz (HIRC) [1] @2.4V	1.7				
		10 kHz (LIRC)[2]	0.30	0.50	0.46	2.33	

Notes:

1. This value base on HIRC enable, LIRC enable
2. This value base on HIRC disable, LIRC enable
3. LVR17 enabled, POR enable and BOD enable.
4. Based on characterization, not tested in production unless otherwise specified.

Table 8.2-1 Current Consumption In Normal Run Mode

Symbol	Conditions	Fsys	Typ [3]	Max[3][4]			Unit
			T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode, executed from Flash, all peripherals disable	24 MHz(HIRC)[1] @5.5V	1.8	2.1	2.0	2.2	mA
		24 MHz(HIRC)[1] @3.3V	1.7				
		24 MHz(HIRC)[1] @2.4V	1.5				
		16 MHz (HIRC)[1] @5.5V	1.4	1.7	1.6	1.8	
		16 MHz (HIRC)[1] @3.3V	1.2				
		16 MHz (HIRC)[1] @2.4V	1.0				
		10 kHz (LIRC)[2]	0.2	0.2	0.24	0.27	

Notes:
1. This value base on HIRC enable, LIRC enable
2. This value base on HIRC disable, LIRC enable
3. LVR17 enabled, POR enable and BOD enable.
4. Based on characterization, not tested in production unless otherwise specified.

Table 8.2-2 Current Consumption In Idle Mode

Symbol	Test Conditions	Typ[1]	Max[2]			Unit
		T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_PD}	Power down mode, all peripherals disable@5.5V	8.2	8	10[3]	20	µA
	Power down mode, all peripherals disable@3.3V	7.9				
	Power down mode, all peripherals disable@2.4V	7.5				
	Power down mode, LVR enable BOD enable all other peripherals disable	210	220	240	292	

Notes:
1. AV_{DD} = V_{DD} = 3.3V unless otherwise specified, LVR17 enable, POR disabled and BOD disabled.
2. Based on characterization, not tested in production unless otherwise specified.
3. Based on characterization, tested in production.

Table 8.2-3 Chip Current Consumption In Power Down Mode

8.2.2 Wakeup Time from Low-Power Modes

Symbol	Parameter		Typ	Max	Unit
t_{WU_IDLE}[1]	Wakeup from IDLE mode		5	6	cycles
t_{WU_NPD}[2][3]	Wakeup from Power down mode	Fsys = HIRC @16MHz	-	40	µs
		Fsys = HIRC @ 24MHz	-	40	µs

Notes:

1. Measured on a wakeup phase with a 16 MHz HIRC oscillator.
2. Based on test during characterization, not tested in production.
3. The wakeup times are measured from the wakeup event to the point in which the application code reads the first.

Table 8.2-4 Low-Power Mode Wakeup Timings

8.2.3 I/O DC Characteristics

8.2.3.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage (I/O with TTL input)	V_{SS}-0.3	-	0.2V_{DD}-0.1	V	
V_{IL1}	Input low voltage (I/O with Schmitt trigger input and Xin)	0	-	0.3*V_{DD}	V	
V_{IH}	Input high voltage (I/O with TTL input)	0.2V_{DD}+0.9	-	V_{DD}+0.3	V	
V_{IH1}	Input high voltage (I/O with Schmitt trigger input and Xin)	0.7*V_{DD}	-	V_{DD}	V	
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	0.2*V_{DD}	-	V	
I_{LK}[*2]	Input leakage current	-1		1	µA	V_{SS} < V_{IN} < V_{DD}, Open-drain or input only mode
		-1		1		V_{DD} < V_{IN} < 5.5 V, Open-drain or input only mode

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.
3. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up resistors must be disabled. Leakage could be higher than the maximum value, if positive current is injected on adjacent pins

Table 8.2-5 I/O Input Characteristics

8.2.3.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[1] [2]	Source current for quasi-bidirectional mode and high level	-7.4	-	-7.5	µA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-7.3	-	-7.5	µA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-7.3	-	-7.5	µA	V_{DD} = 2.4 V V_{IN} =(V_{DD}-0.4) V
		-57.2	-	-58.3	µA	V_{DD} = 5.5 V V_{IN} = 2.4 V
	Source current for push-pull mode and high level	-9	-	-9.6	mA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-6	-	-6.6	mA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-4.2	-	-4.9	mA	V_{DD} = 2.7 V V_{IN} =(V_{DD}-0.4) V
		-18	-	-20	mA	V_{DD} = 5.5 V V_{IN} = 2.4 V
I_{SK}[1] [2]	Sink current for push-pull mode and low level	18	-	20	mA	V_{DD} = 5.5 V V_{IN} = 0.4 V
		16	-	18	mA	V_{DD} = 3.3 V V_{IN} = 0.4 V
		9.7	-	11	mA	V_{DD} = 2.4 V V_{IN} = 0.4 V
C_{IO}[1]	I/O pin capacitance	-	5	-	pF	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.2-6 I/O Output Characteristics

8.2.3.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}[1]	Internal nRESET pull up resistor	45	-	60	KΩ	V_{DD} = 5.5 V
		45	-	65		V_{DD} = 2.4 V
t_{FR}[1]	nRESET input response time	-	1.5	-	µs	Normal run and Idle mode
		10	-	25		Power down mode

Notes:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.2-7 nRESET Input Characteristics

8.3 AC Electrical Characteristics

8.3.1 Internal High Speed RC Oscillator (HIRC)

8.3.1.1 Internal High Speed 16MHz RC Oscillator

The 16 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{HRC}	Oscillator frequnecy	-	16[1]	-	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1[3]	-	1[3]	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[4]	-	2[4]	%	T_A = -20°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
		-4[4]		4[4]	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
I_{HRC}[2]	Operating current	-	490	550	µA	
T_S[3]	Stable time	-	3	5	µs	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V

Notes:

1. Default setting value for the product
2. Based on reload value.
3. Based on characterization, tested in production.
4. Guaranteed by characterization result, not tested in production.
5. Guaranteed by design.

Table 8.3-1 16 MHz Internal High Speed RC Oscillator(HIRC) Characteristics

8.3.1.2 Internal High Speed 24MHz RC Oscillator

The 24 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{HRC}	Oscillator frequnecy	-	24[1]	-	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1[3]	-	1[3]	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[4]	-	2[4]	%	T_A = -20°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
		-4[4]		4[4]	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
I_{HRC}[2]	Operating current	-	490	550	µA	
T_S[3]	Stable time	-	3	5	µs	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V

Notes:

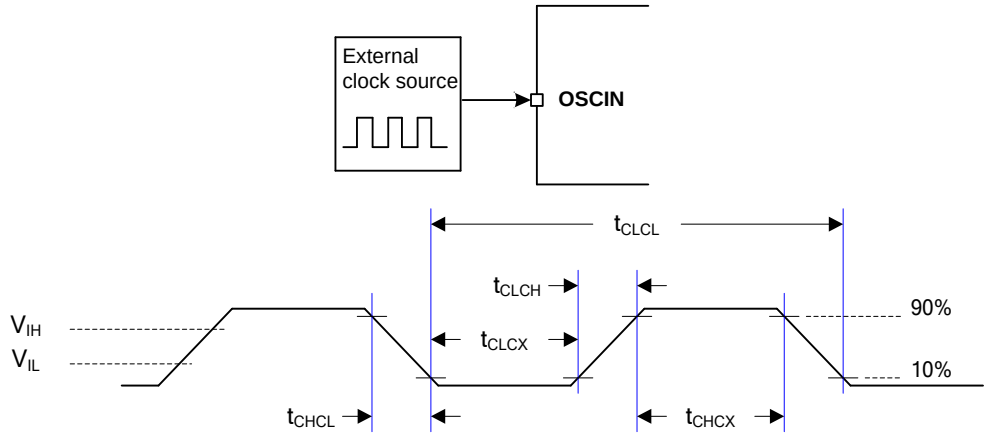
1. Default setting value for the product
2. Based on reload value.
3. Based on characterization, tested in production.
4. Guaranteed by characterization result, not tested in production.
5. Guaranteed by design.

Table 8.3-2 24 MHz Internal High Speed RC Oscillator(HIRC) characteristics

8.3.2 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the ECLK mode is enabled, OSCIN is the external clock input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	4	-	24	MHz	
t_{CHCX}	Clock high time	8	-	-	ns	
t_{CLCX}	Clock low time	8	-	-	ns	
t_{CLCH}	Clock rise time	-	-	10	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	ns	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Notes:

1. Guaranteed by characterization, not tested in production.

Table 8.3-3 External 4~24 MHz High Speed Clock Input Signal

8.3.3 Internal 10 kHz Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{LRC}	Oscillator frequnecy	-	10	-	kHz	
	Frequency drift over temperarure and volatge	-10[1]	-	10[1]	%	T_A = 25 °C, V_{DD} = 5V
		-35[2]	-	35[2]	%	T_A=-40~105°C Without software calibration
I_{LRC}[3]	Operating current	-	0.85	1	μA	V_{DD} = 3.3V
T_S	Stable time	-	500	-	μs	T_A=-40~105°C

Notes:

1. Guaranteed by characterization, tested in production.
2. Guaranteed by characterization, not tested in production.
3. Guaranteed by design.

Table 8.3-4 10 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

8.3.4 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Normal mode [4] output high (90%) to low level (10%) falling time	4.6	5.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.9	3.3		C_L = 10 pF, V_{DD} >= 5.5 V
		6.6	8		C_L = 30 pF, V_{DD} >= 3.3 V
		4.3	5		C_L = 10 pF, V_{DD} >= 3.3 V
		8.5	12.5		C_L = 30 pF, V_{DD} >= 2.4 V
		8.0	10.7		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{f(IO)out}$	High slew rate mode [5] output high (90%) to low level (10%) falling time	4.0	4.3	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		4.9	5.8		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		9.5	13.8		C_L = 30 pF, V_{DD} >= 2.4 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{r(IO)out}$	Normal mode [4] output low (10%) to high level (90%) rising time	5.6	6.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		3.4	3.7		C_L = 10 pF, V_{DD} >= 5.5 V
		8.1	9.4		C_L = 30 pF, V_{DD} >= 3.3 V
		5.1	5.8		C_L = 10 pF, V_{DD} >= 3.3 V
		15.1	20.3		C_L = 30 pF, V_{DD} >= 2.4 V
		9.6	12.4		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{r(IO)out}$	High slew rate mode [5] output low (10%) to high level (90%) rising time	4.8	5.2	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		6.4	7.4		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		12.7	16.9		C_L = 30 pF, V_{DD} >= 2.4 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 2.4 V
$f_{max(IO)out}$[*3]	I/O maximum frequency	24	24	MHz	C_L = 30 pF, V_{DD} >= 2.4 V
					C_L = 10 pF, V_{DD} >= 2.4 V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. PxSR.n bit value = 0, Normal output slew rate
5. PxSR.n bit value = 1, high speed output slew rate

Table 8.3-5 I/O AC Characteristics

8.4 Analog Characteristics

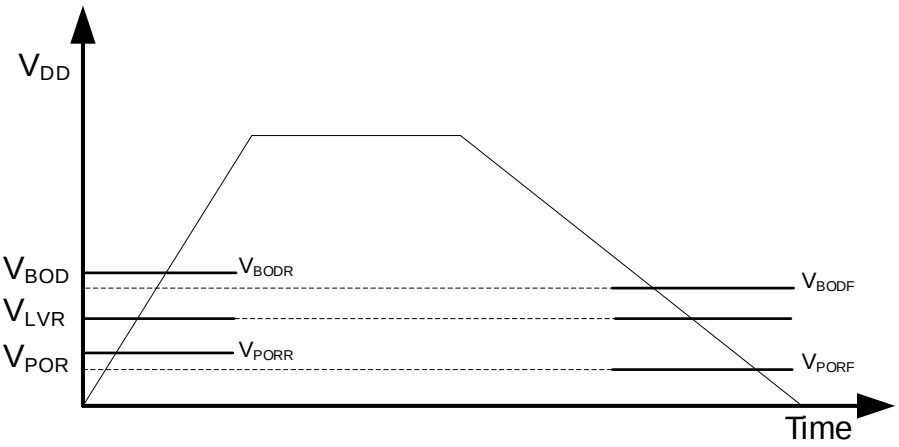
8.4.1 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}	POR operating current	10		20	μA	AV_{DD} = 5.5V
I_{LVR}	LVR operating current	0.5	-	1		AV_{DD} = 5.5V
I_{BOD}	BOD operating current	-	200	230		AV_{DD} = 5.5V
V_{PORR}	POR reset voltage (Power on rising threshold level)	1	1.15	1.3	V	-
V_{PORF}	POR reset voltage (Power off falling threshold level)	0.9	1.05	1.15		-
V_{LVR}	LVR reset threshold voltage	1.7	2.0	2.4		-
V_{BODR}	BOD brown-out detect voltage (Power on rising threshold level)	4.2	4.5	4.8		BOV[1:0] = [0,0]
		3.6	3.8	4.0		BOV[1:0] = [0,1]
		2.6	2.8	3		BOV[1:0] = [1,0]
		2.1	2.3	2.5		BOV[1:0] = [1,1]
V_{BODF}	BOD brown-out detect voltage (Power off falling threshold level)	4.1	4.4	4.7		BOV[1:0] = [0,0]
		3.5	3.7	3.9		BOV[1:0] = [0,1]
		2.5	2.7	2.9		BOV[1:0] = [1,0]
		2.0	2.2	2.4		BOV[1:0] = [1,1]
T_{LVR_SU}	LVR startup time	48	61	80	μs	-
T_{LVR_RE}	LVR respond time	-	-	30		Fsys = HIRC@16MHz
		-	-	30		Fsys = LIRC
T_{BOD_SU}	BOD startup time	180	-	320		Fsys = HIRC@16MHz
T_{BOD_RE}	BOD respond time	2.5	-	5		Fsys = HIRC@16MHz
R_{VDDR}	V_{DD} rise time rate	160	-	-	μS/V	POR Enabled
R_{VDDF}	V_{DD} fall time rate	160	-	-		POR Enabled, BOD Enabled, LVR Enabled

Notes:
1.All data except as otherwise noted is guaranteed by characterization results, not tested in production.

Table 8.4-1 Reset and Power Control Unit



Note: V_{POR} detect internal LDO voltage.

Figure 8.4-1 Power Ramp Up/Down Condition

BODFLT (BODCON1.1)	BOD Operation Mode	System Clock Source	Minimum Brown-out Detect Pulse Width
0	Normal mode (LPBOD[1:0] = [0,0])	Any clock source	Typ. 1μs
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	16 ($1/F_{LIRC}$)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	64 ($1/F_{LIRC}$)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	256 ($1/F_{LIRC}$)
1	Normal mode (LPBOD[1:0] = [0,0])	HIRC/ECLK	Normal operation: 32 ($1/F_{SYS}$) Idle mode: 32 ($1/F_{SYS}$) Power-down mode: 2 ($1/F_{LIRC}$)
		LIRC	2 ($1/F_{LIRC}$)
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	18 ($1/F_{LIRC}$)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	66 ($1/F_{LIRC}$)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	258 ($1/F_{LIRC}$)

Table 8.4-2 Minimum Brown-Out Detect Pulse Width

8.4.2 12-bit SAR ADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog Operating Voltage	2.4	-	5.5	V	$AV_{DD} = V_{DD}$
V_{REF}	Reference Voltage	2.4	-	AV_{DD}	V	$V_{REF} = AV_{DD}$
V_{IN}	ADC Channel Input Voltage	0	-	V_{REF}	V	
I_{ADC}[1]	Operating current (AV_{DD} + V_{REF} current)	-	-	418	μA	$AV_{DD} = V_{DD} = V_{REF}$ = 5.5 V F_{ADCCOV} = 500 kHz
N_R	Resolution	12			Bit	
T_{ADCEC}	Encoding Time[2]	1.6			μs	This value is fixed by ADC module
F_{ADCLK}	ADC Sampling Clock Frequency	F_{SYS}/8		F_{SYS}		
T_{ADCSMP}	ADC Sampling Time[2]	0.4	-	17	μs	F_{SYS} = 16MHz
		0.417	-	11.3	μs	F_{SYS} = 24MHz
F_{ADCCOV}	Conversion Rate $F_{ADCCOV} = 1/T_{ADCCOV}$	53.7	-	500	kHz	F_{SYS} = 16MHz
		77.6	-	495	kHz	F_{SYS} = 24MHz
T_{ADCCOV}	Conversion Time[2] $T_{ADCCOV} = T_{ADCSMP} + T_{ADCEC}$	2	-	18.6	μs	F_{SYS} = 16MHz
		2.017	-	12.9	μs	F_{SYS} = 24MHz
T_{EN}	Enable To Ready Time	20	-	-	μs	
INL[1]	Integral Non-Linearity Error	-1	-	+4	LSB	$V_{REF} = AV_{DD} = V_{DD}$
DNL[1]	Differential Non-Linearity Error	-2	-	+4	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_G[1]	Gain Error	+2	-	+4.6	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_{OT}[1]	Offset Error	-2	-	+2.8	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_A[1]	Absolute Error	-7	-	+7	LSB	$V_{REF} = AV_{DD} = V_{DD}$
R_S	Input Channel Equivalent Resistance	-	0.5	2.5	kΩ	
C_{IN}	Input Equivalent Capacitance	-	2.5	-	pF	
R_{IN}[1]	Internal Switch Resistance	-	0.5	-	kΩ	
R_{EX}[1]	External input impedance	-	-	33	kΩ	

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions

1. All data except as otherwise noted is guaranteed by characterization results, not tested in production.
2. ADC conversion time $T_{ADCCOV} = T_{ADCSMP} + T_{ADCEC}$. Encoding time is fixed, the fastest conversion rate is limited to 500k, so the sampling time has a minimum time constraint and must be greater than 400 μs.

   ADC Sampling Time $T_{ADCSMP} = \frac{4*ADCAQT+6}{F_{ADCCLK}}$, where ADCAQT is defined in ADCCON2[3:1] 3bit value from 0 ~ 7

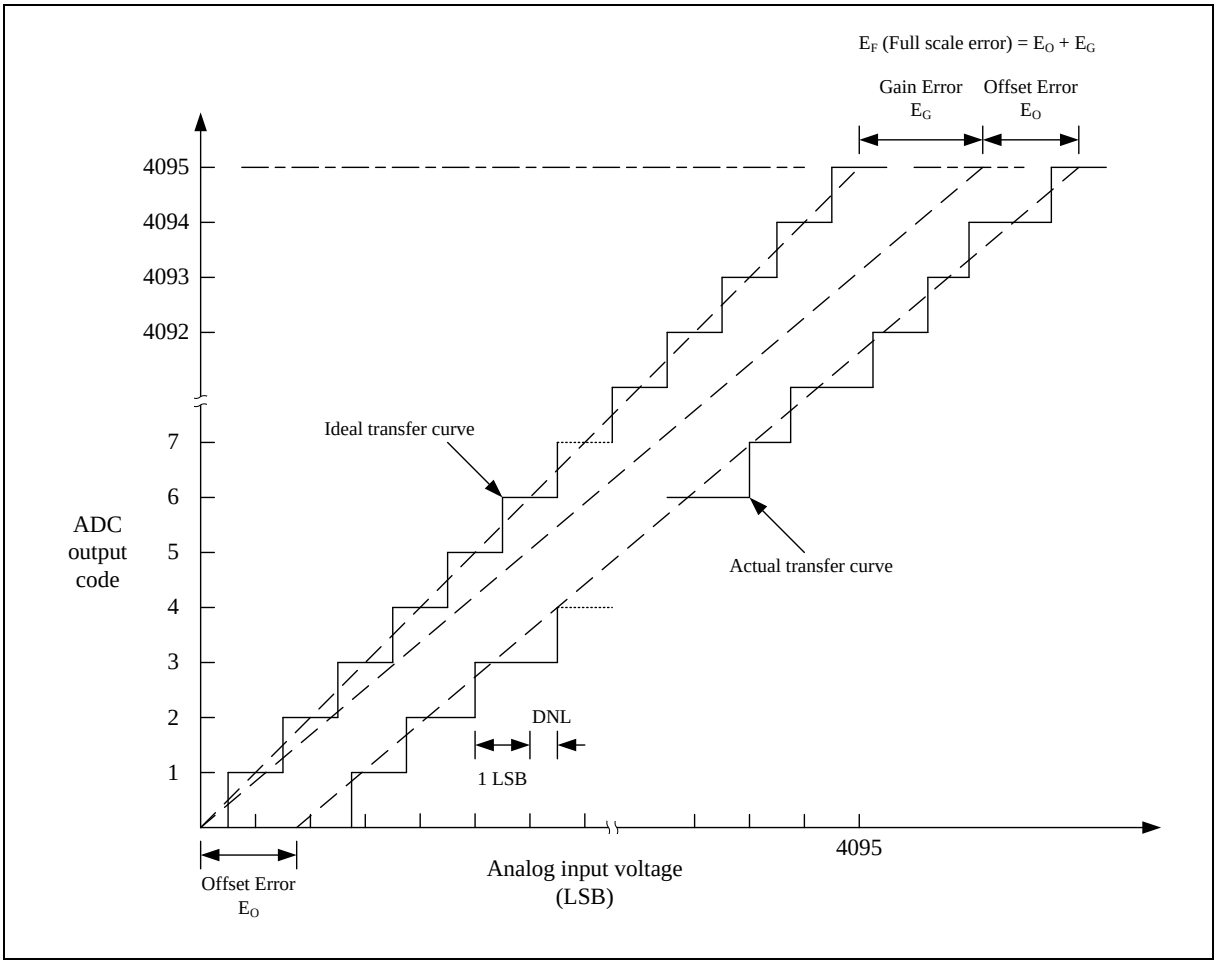
   and $F_{ADCCLK} = \frac{F_{SYS}}{ADCDIV}$, where ADCDIV is defined in ADCCON1[5:4] .

   When F_{SYS} = 16MHz, ADC Sampling Time Minimum value is $\frac{6}{16MHz}$ (ADCAQT = 0, ADCDIV = 0), ADC Sampling Time Maximum value is $\frac{4*7+6}{16MHz/8}$ (ADCAQT = 7, ADCDIV = 8) .

   When F_{SYS} = 24MHz, Due to limitations in sampling timing, we recommend setting ADCAQT to at least 1. ADC Sampling Time Minimum value is $\frac{4*1+6}{24MHz}$ (ADCAQT = 1, ADCDIV = 0), ADC Sampling Time Maximum value is $\frac{4*7+6}{24MHz/8}$ (ADCAQT = 7, ADCDIV = 8).
3. R_{EX} maximum formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (TSMP). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} < \frac{k}{F_{ADCCOV} \times (C_{IN} + C_{EX}) \times \ln(2^{N+2})} - R_{IN}$$

Table 8.4-3 ADC Characteristics



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer

curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5 Communications Characteristics

8.5.1 SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/T_{SPICLK}$	SPI clock frequency	-	-	$F_{SYS}/2$	MHz	2.4 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	$T_{SPICLK}/2$			ns	
t_{CLKL}	Clock output Low time	$T_{SPICLK}/2$			ns	
t_{DS}	Data input setup time	2	-	-	ns	
t_{DH}	Data input hold time	$1/F_{SYS}$	-	-	ns	
t_V	Data output valid time	-	-	5	ns	Matser mode 2.4 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
				$1/F_{SYS}$	ns	Slave mode 2.4 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF

Note:

1. All data except as otherwise noted is guaranteed by characterization results, not tested in production.

Table 8.5-1 SPI Master Mode Characteristics

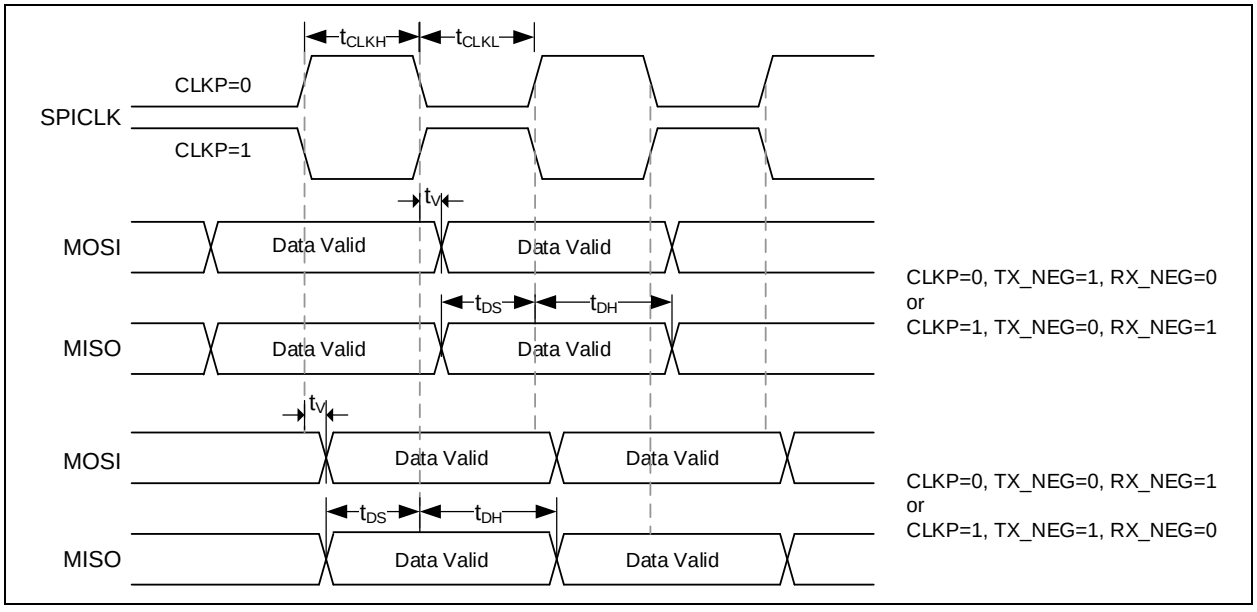


Figure 8.5-1 SPI Master Mode Timing Diagram

8.5.2 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	µS
t_{HIGH}	SCL high period	4	-	0.6	-	µS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	µS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	µS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	µS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	µS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	µS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. All data except as otherwise noted is guaranteed by characterization results, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.5-2 I²C Characteristics

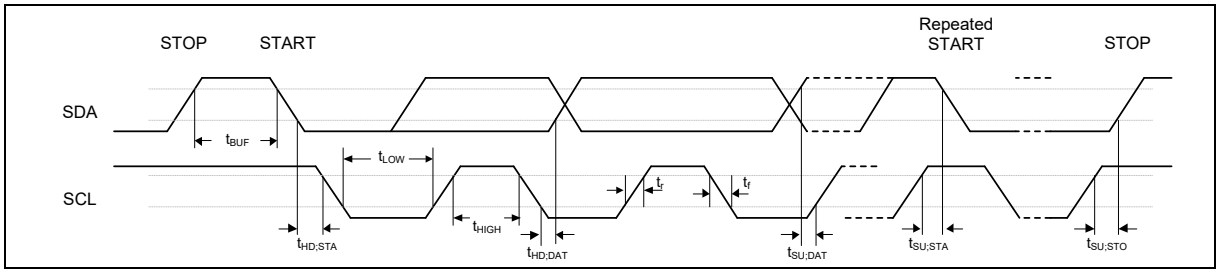


Figure 8.5-2 I²C Timing Diagram

8.6 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_{ERASE}	Page erase time	-	5	-	ms	T_A = 25℃
T_{PROG}	Program time	-	20	-	µs	
I_{DD1}	Read current	-	4	-	mA	
I_{DD2}	Program current	-	2	-	mA	
I_{DD3}	Erase current	-	2	-	mA	
N_{ENDUR}	Endurance	100,000	-		cycles[2]	T_J = -40℃~125℃
T_{RET}	Data retention	50	-	-	year	100 kcycle[2] T_A = 55℃
		25	-	-	year	100 kcycle[2] T_A = 85℃
		10	-	-	year	100 kcycle[2] T_A = 105℃

Notes:

1. All data except as otherwise noted is guaranteed by characterization results, not tested in production.
2. Number of program/erase cycles.

Table 8.6-1 Flash Memory Characteristics

8.7 Absolute Maximum Ratings

Voltage Stesses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.7.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	6.5	V
ΔV_{DD}	Variations between different power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on I/O	V_{SS}-0.3	5.5	V

Notes:

1. All main power (V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.

Table 8.7-1 Voltage Characteristics

8.7.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	150	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	150	
I_{IO}	Maximum current sunk by a I/O Pin	-	22	
	Maximum current sourced by a I/O Pin	-	10	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$ [*3]	Maximum injected current by an I/O Pin	-	±5	$I_{INJ(PIN)}$ [*3]
$\Sigma I_{INJ(PIN)}$ [*3]	Maximum injected current by total I/O Pins	-	±25	$\Sigma I_{INJ(PIN)}$ [*3]

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by V_{IN}>A_{VDD} and a negative injection is caused by V_{IN}<V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.7-2 Current Characteristics

8.7.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	℃
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 20-pin QFN(3x3 mm)	-	68	-	℃/Watt
	Thermal resistance junction-ambient 20-pin TSSOP(4.4x6.5 mm)	-	38	-	
Note: Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions					

Table 8.7-3 Thermal Characteristics

8.7.4 EMC Characteristics

8.7.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.7.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.7.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-7000	-	+7000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-1000	-	+1000	
LU[*3]	Pin current for latch-up[*3]	-200	-	+200	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4.4	-	+4.4	kV

Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 8.7-4 EMC Characteristics

8.7.5 Soldering Profile

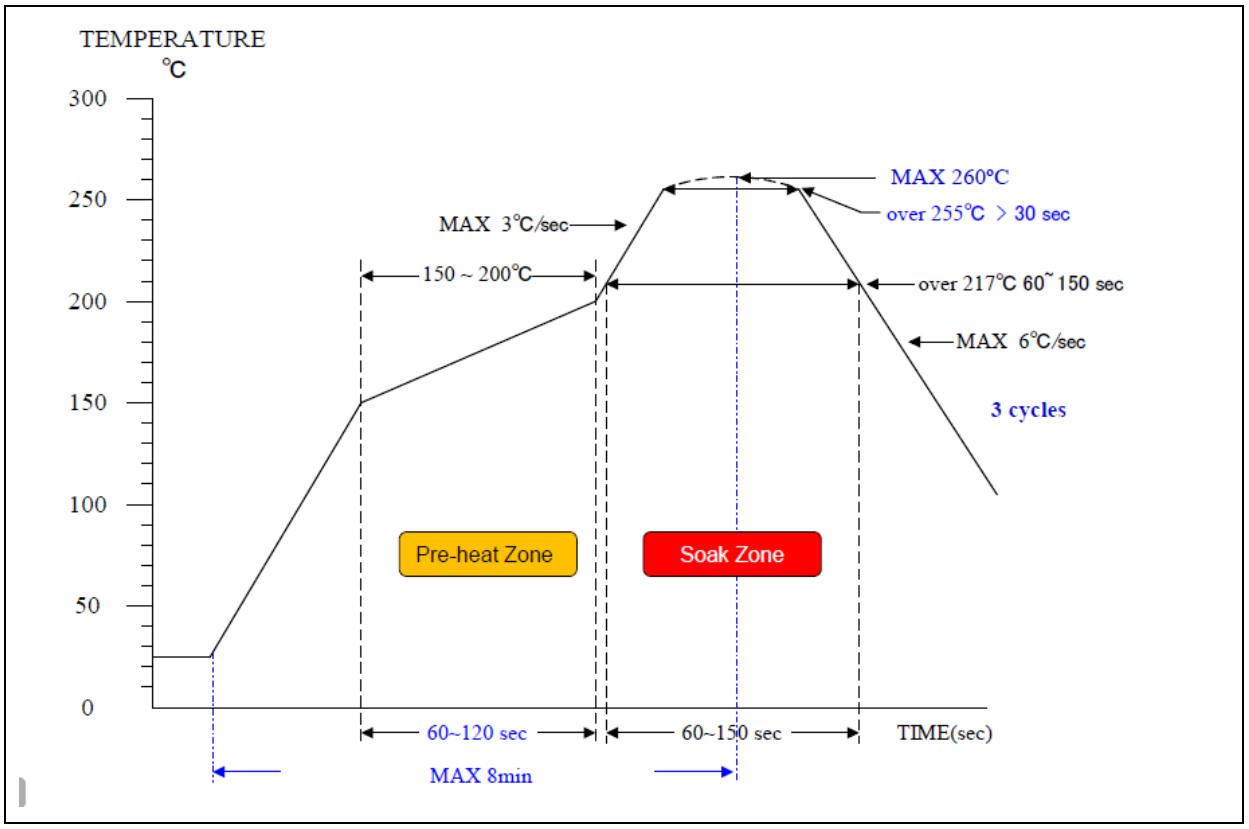


Figure 8.7-1 Soldering Profile

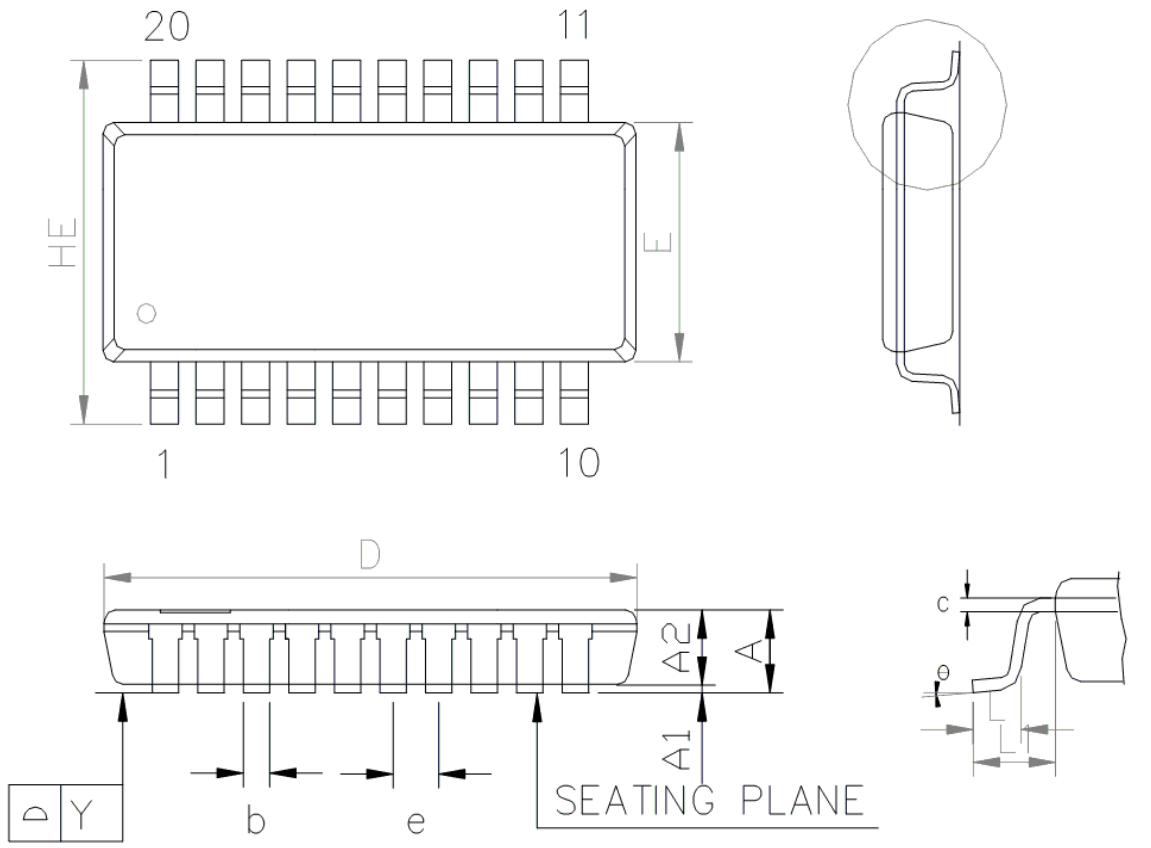
Porfile Feature	Pb Free Package
Average ramp-up rate (217℃ to peak)	3℃/sec. max
Preheat temperature 150℃ ~200℃	60 sec. to 120 sec.
Temperature maintained above 217℃	60 sec. to 150 sec.
Time with 5℃ of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6℃/sec max.
Time 25℃ to peak temperature	8 min. max
Note: 1.Determined according to J-STD-020C	

Table 8.7-5 Soldering Profile

9 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

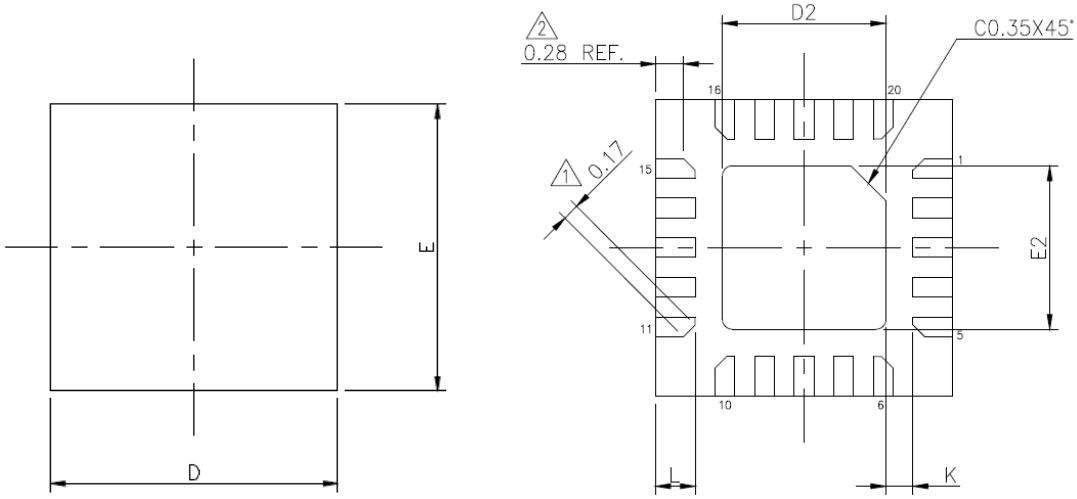
9.1 TSSOP 20-pin (4.4 x 6.5 x 0.9 mm)

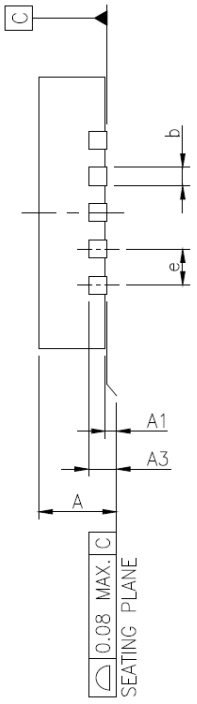


SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	-	0.30	0.007	-	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	-	0.20	0.004	-	0.008
θ	0°	-	8°	0°	-	8°
Y	0.10 BASIC			0.004 BASIC		

Figure 9.1-1 TSSOP-20 Package Dimension

9.2 QFN 20-pin (3.0 x 3.0 x 0.8 mm)





JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X319)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.40 BSC		
K	0.20	—	—

PAD SIZE	D2			E2			L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
75*X75* MIL	1.60	1.65	1.70	1.60	1.65	1.70	0.30	0.40	0.50

Figure 9.2-1 QFN-20 Package Dimension

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
BOD	Brown-out Detection
GPIO	General-Purpose Input/Output
Fsys	Frequency of system clock
HIRC	12 MHz Internal High Speed RC Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LVR	Low Voltage Reset
POR	Power On Reset
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WKT	Wakeup Timer
WDT	Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Chapter	Description
2023.05.02	1.00		Initial version.
2025.05.13	1.01		Change CM1003 to CM1003xFxAE
		Section 2	Delete 18K Flash size
		Section 3.2	Modify CM1003 Series Naming Rule
		Section 3.3	Modify CM1003 Series Selection Gude
		Section 4.1.1	Modify Figure 4.1-1 Pin Assignment of TSSOP-20 Package
		Section 6.1	Modify Memory Organization
		Section 8.1	Add items to Table 8.1-1 General Operating
		Section 8.2.3	Modify the parameter description in Table 8.2-5
		Section 8.3.1	Modify the test temperatures in Table 8.3-1 and Table 8.3-2 and page7
		Section 8.4.1	Modify Figure 8.4-1 Power Ramp Up/Down Condition
		Section 8.4.1	Add items to Table 8.4-1 Reset and Power Control Unit
		Section 8.4.2	Modify Table 8.4-3
		Section 8.5	Add Communications Characteristics
		Section 8.6	Modify Table 8.6-1 Flash Memory Characteristics
		Section 8.7.2	Add items to Table 8.7-2 Current Characteristics
		Section 8.7.4.3	Modify Table 8.7-4 EMC Characteristics
		Section 9.2	Modify Figure 9.2-1 QFN-20 Package Dimension
2025.08.06			Delete MSL related descriptions

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