8-bit Parallel-in, Serial out Shift Register

CJ74HC/HCT165 Logic

1 Introduction

The CJ74HC/HCT165 is 8-bit serial or parallel-in/serial-out shift registers. The device features a serial data input (DS), eight parallel data inputs (D0 to D7) and two complementary serial outputs (Q7 and /Q7). When the parallel load input (/PL) is LOW the data from D0 to D7 is loaded into the shift register asynchronously. When /PL is HIGH data enters the register serially at DS. When the clock enable input (/CE) is LOW data is shifted on the LOW-to-HIGH transitions of the CP input. A HIGH on /CE will disable the CP input. Inputs are overvoltage tolerant to 15V. This enables the device to be used in HIGH-to-LOW level shifting applications.

2 Available Packages

PART NUMBER	PACKAGE
CJ74HC165	SOP16
	TSSOP16
CJ74HCT165	SOP16
	TSSOP16

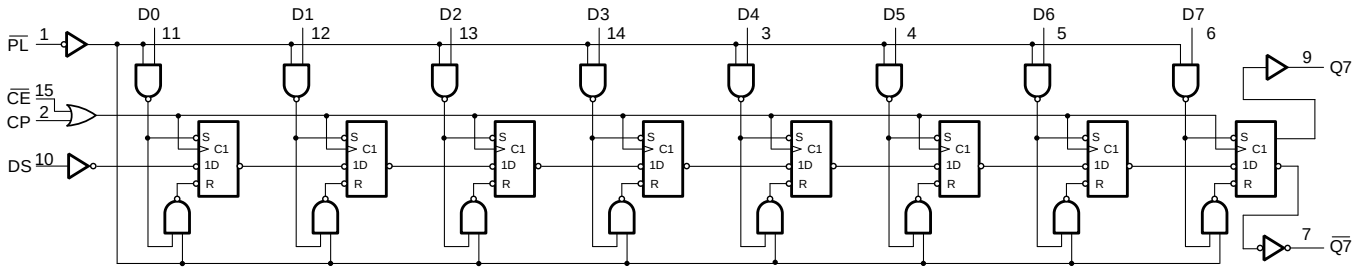
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Input levels:
  - For CJ74HC165: CMOS level
  - For CJ74HCT165: TTL level
- Asynchronous 8-bit parallel load
- Synchronous serial input
- ESD-HBM:3000V
- ESD-CDM:1000V
- Specified from -40°C to +125°C

4 Applications

- Programable Logic Controllers
- Appliances
- Video Display Systems
- Output Expander
- Keyboards



Function diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74HC165AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HCT165AEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CJ74HC165BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active
CJ74HCT165BEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

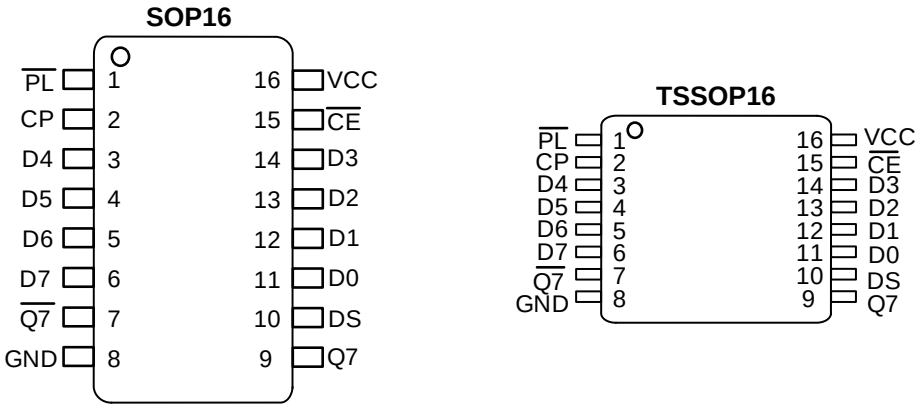


Figure 6-1 Pin Configuration

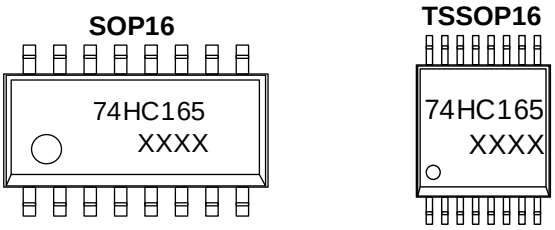
6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	$\overline{PL}$	I	Asynchronous parallel load input (active LOW)
2	CP	I	Clock input (LOW-to-HIGH, edge-triggered)
3	D4	I	Parallel data input (also referred to as Dn)
4	D5	I	Parallel data input (also referred to as Dn)
5	D6	I	Parallel data input (also referred to as Dn)
6	D7	I	Parallel data input (also referred to as Dn)
7	$\overline{Q7}$	O	Complementary output from the last stage
8	GND	G	Ground (0V)
9	Q7	O	Serial output from the last stage
10	DS	I	Serial data input
11	D0	I	Parallel data input (also referred to as Dn)
12	D1	I	Parallel data input (also referred to as Dn)
13	D2	I	Parallel data input (also referred to as Dn)
14	D3	I	Parallel data input (also referred to as Dn)
15	$\overline{CE}$	I	Clock enable input (active LOW)
16	VCC	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information

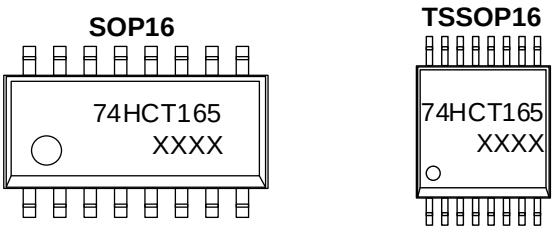
6.3.1 CJ74HC165



74HC165: Device number.

XXXX: Code, indicates weekly record information.

6.3.2 CJ74HCT165



74HCT165: Device number.

XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{CC}	Supply voltage	-		-0.5	+7	V
I_{IK}	Input clamping current	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$		-	±20	mA
I_{OK}	Output clamping current	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$		-	±20	mA
I_O	Output current	$-0.5V < V_O < V_{CC}+0.5V$		-	±25	mA
I_{CC}	Supply current	-		-	50	mA
I_{GND}	Ground current	-		-50	-	mA
P_{tot}	Total power dissipation	-		-	500	mW
T_{stg}	Storage temperature	-		-65	+150	°C
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CJ74HC165						
V_{CC}	Supply voltage	-	2.0	5.0	6.0	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C
CJ74HCT165						
V_{CC}	Supply voltage	-	4.5	5.0	5.5	V
V_I	Input voltage	-	0	-	V_{CC}	V
V_O	Output voltage	-	0	-	V_{CC}	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM)(1)	±4000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC165							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8	uA
C_I	Input capacitance	-		-	3.5	-	pF
CJ74HCT165							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	1.6	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	1.2	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	4.5	-	V
			I_O=-4.0mA	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V	Dn and DS inputs	-	35	126	uA
			CP, $\overline{CE}$, and $\overline{PL}$ inputs	-	65	234	uA
C_I	Input capacitance	-		-	3.5	-	pF

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC165							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
CJ74HCT165							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4.0mA	3.84	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V	Dn and DS inputs	-	-	157.5	uA
			CP, $\overline{CE}$, and $\overline{PL}$ inputs	-	-	292.5	uA

7.4.3 DC Characteristics 3

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC165							
V_{IH}	HIGH-level input voltage	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
CJ74HCT165							
V_{IH}	HIGH-level input voltage	V_{CC}=4.5V to 5.5V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC}=4.5V to 5.5V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4.0mA	3.7	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
I_I	Input leakage current	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1	uA
I_{CC}	Supply current	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
ΔI_{CC}	Additional supply current	Per input pin; V_I=V_{CC}-2.1V; Other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V	Dn and DS inputs	-	-	171.5	uA
			CP, $\overline{CE}$, and $\overline{PL}$ inputs	-	-	318.5	uA

7.4.4 AC Characteristics 1

T_{amb}=25°C, GND=0V, C_L=50pf, unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC165							
t_{PLH}, t_{PHL}	Propagation delay	CP, $\overline{CE}$ to Q7, $\overline{Q7}$; See Figure 8-6	V_{CC}=2.0V	-	52	165	ns
			V_{CC}=4.5V	-	19	33	ns
			V_{CC}=5.0V; C_L=15pF	-	16	-	ns
			V_{CC}=6.0V	-	15	28	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; See Figure 8-7	V_{CC}=2.0V	-	50	165	ns
			V_{CC}=4.5V	-	18	33	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
			V_{CC}=6.0V	-	14	28	ns
		D7 to Q7, $\overline{Q7}$; See Figure 8-8	V_{CC}=2.0V	-	36	120	ns
			V_{CC}=4.5V	-	13	35	ns
			V_{CC}=5.0V; C_L=15pF	-	11	-	ns
			V_{CC}=6.0V	-	10	32	ns
t_{THL}, t_{TLH}	Transition time	Q7, $\overline{Q7}$ output; See Figure 8-6	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
t_W	Pulse width	CP input HIGH or LOW; See Figure 8-6	V_{CC}=2.0V	80	17	-	ns
			V_{CC}=4.5V	16	6	-	ns
			V_{CC}=6.0V	14	5	-	ns
		$\overline{PL}$ input LOW; See Figure 8-7	V_{CC}=2.0V	80	14	-	ns
			V_{CC}=4.5V	16	5	-	ns
			V_{CC}=6.0V	14	4	-	ns
t_{rec}	Recovery time	$\overline{PL}$ to CP, $\overline{CE}$; See Figure 8-7	V_{CC}=2.0V	100	22	-	ns
			V_{CC}=4.5V	20	8	-	ns
			V_{CC}=6.0V	17	6	-	ns
t_{su}	Set-up time	DS to CP, $\overline{CE}$; See Figure 8-9	V_{CC}=2.0V	80	11	-	ns
			V_{CC}=4.5V	16	4	-	ns
			V_{CC}=6.0V	14	3	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; See Figure 8-9	V_{CC}=2.0V	80	17	-	ns
			V_{CC}=4.5V	16	6	-	ns
			V_{CC}=6.0V	14	5	-	ns
		Dn to $\overline{PL}$; See Figure 8-10	V_{CC}=2.0V	80	22	-	ns
			V_{CC}=4.5V	16	8	-	ns
			V_{CC}=6.0V	14	6	-	ns
t_h	Hold time	DS to CP, $\overline{CE}$ and Dn to	V_{CC}=2.0V	5	2	-	ns

		$\overline{PL}$; See Figure 8-9	V_{CC}=4.5V	5	2	-	ns
			V_{CC}=6.0V	5	2	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; See Figure 8-9	V_{CC}=2.0V	5	-17	-	ns
			V_{CC}=4.5V	5	-6	-	ns
			V_{CC}=6.0V	5	-5	-	ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	V_{CC}=2.0V	6	17	-	MHz
			V_{CC}=4.5V	30	-	-	MHz
			V_{CC}=5.0V; C_L=15pF	32	-	-	MHz
			V_{CC}=6.0V	35	-	-	MHz
CJ74HCT165							
t_{PLH}, t_{PHL}	Propagation delay	CP, $\overline{CE}$ to Q7, $\overline{Q7}$; See Figure 8-6	V_{CC}=4.5V	-	17	34	ns
			V_{CC}=5.0V; C_L=15pF	-	14	-	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; See Figure 8-7	V_{CC}=4.5V	-	20	40	ns
			V_{CC}=5.0V; C_L=15pF	-	17	-	ns
		D7 to Q7, $\overline{Q7}$; See Figure 8-8	V_{CC}=4.5V	-	14	35	ns
			V_{CC}=5.0V;C_L=15pF	-	11	-	ns
t_{THL}, t_{TLH}	Transition time	Q7, $\overline{Q7}$ output; See Figure 8-6	V_{CC}=4.5V	-	7	15	ns
t_W	Pulse width	CP input; See Figure 8-6	V_{CC}=4.5V	16	6	-	ns
		$\overline{PL}$ input; See Figure 8-7	V_{CC}=4.5V	20	9	-	ns
t_{rec}	Recovery time	$\overline{PL}$ to CP, $\overline{CE}$; See Figure 8-7	V_{CC}=4.5V	20	8	-	ns
t_{su}	Set-up time	DS to CP, $\overline{CE}$; See Figure 8-9	V_{CC}=4.5V	20	2	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; See Figure 8-9	V_{CC}=4.5V	20	7	-	ns
		Dn to $\overline{PL}$; See Figure 8-10	V_{CC}=4.5V	20	10	-	ns
t_h	Hold time	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$; See Figure 8-9	V_{CC}=4.5V	7	-1	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; See Figure 8-9	V_{CC}=4.5V	0	-7	-	ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	V_{CC}=4.5V	26	-	-	MHz
			V_{CC}=5.0V; C_L=15pF	28	-	-	MHz

7.4.5 AC Characteristics 2

T_{amb}=-40°C to +85°C, GND=0V, C_L=50pf, unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC165							
t_{PLH}, t_{PHL}	Propagation delay	CP, $\overline{CE}$ to Q7, $\overline{Q7}$; See Figure 8-6	V_{CC}=2.0V	-	-	205	ns
			V_{CC}=4.5V	-	-	41	ns
			V_{CC}=6.0V	-	-	35	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; See Figure 8-7	V_{CC}=2.0V	-	-	205	ns
			V_{CC}=4.5V	-	-	41	ns
			V_{CC}=6.0V	-	-	35	ns
		D7 to Q7, $\overline{Q7}$; See Figure 8-8	V_{CC}=2.0V	-	-	150	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	35	ns
t_{THL}, t_{TLH}	Transition time	Q7, $\overline{Q7}$ output; See Figure 8-6	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	16	ns
t_W	Pulse width	CP input HIGH or LOW; See Figure 8-6	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
		$\overline{PL}$ input LOW; See Figure 8-7	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
t_{rec}	Recovery time	$\overline{PL}$ to CP, $\overline{CE}$; See Figure 8-7	V_{CC}=2.0V	125	-	-	ns
			V_{CC}=4.5V	25	-	-	ns
			V_{CC}=6.0V	21	-	-	ns
t_{su}	Set-up time	DS to CP, $\overline{CE}$; See Figure 8-9	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; See Figure 8-9	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
		Dn to $\overline{PL}$; See Figure 8-10	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
t_h	Hold time	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$; See Figure 8-9	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$;	V_{CC}=2.0V	5	-	-	ns

		See Figure 8-9	V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	V_{CC}=2.0V	5	-	-	MHz
			V_{CC}=4.5V	24	-	-	MHz
			V_{CC}=6.0V	28	-	-	MHz
CJ74HCT165							
t_{PLH}, t_{PHL}	Propagation delay	CP, $\overline{CE}$ to Q7, $\overline{Q7}$; See Figure 8-6	V_{CC}=4.5V	-	-	43	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; See Figure 8-7	V_{CC}=4.5V	-	-	50	ns
		D7 to Q7, $\overline{Q7}$; See Figure 8-8	V_{CC}=4.5V	-	-	38	ns
t_{THL}, t_{TLH}	Transition time	Q7, $\overline{Q7}$ output; See Figure 8-6	V_{CC}=4.5V	-	-	19	ns
t_W	Pulse width	CP input; See Figure 8-6	V_{CC}=4.5V	20	-	-	ns
		$\overline{PL}$ input; See Figure 8-7	V_{CC}=4.5V	25	-	-	ns
t_{rec}	Recovery time	$\overline{PL}$ to CP, $\overline{CE}$; See Figure 8-7	V_{CC}=4.5V	25	-	-	ns
t_{su}	Set-up time	DS to CP, $\overline{CE}$; See Figure 8-9	V_{CC}=4.5V	25	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; See Figure 8-9	V_{CC}=4.5V	25	-	-	ns
		Dn to $\overline{PL}$; See Figure 8-10	V_{CC}=4.5V	25	-	-	ns
t_h	Hold time	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$; See Figure 8-9	V_{CC}=4.5V	9	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; See Figure 8-9	V_{CC}=4.5V	0	-	-	ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	V_{CC}=4.5V	21	-	-	MHz

7.4.6 AC Characteristics 3

T_{amb}=-40°C to +125°C, GND=0V, C_L=50pf, unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CJ74HC165							
t_{PLH}, t_{PHL}	Propagation delay	CP, $\overline{CE}$ to Q7, $\overline{Q7}$; See Figure 8-6	V_{CC}=2.0V	-	-	250	ns
			V_{CC}=4.5V	-	-	50	ns
			V_{CC}=6.0V	-	-	43	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; See Figure 8-7	V_{CC}=2.0V	-	-	250	ns
			V_{CC}=4.5V	-	-	50	ns
			V_{CC}=6.0V	-	-	43	ns
		D7 to Q7, $\overline{Q7}$; See Figure 8-8	V_{CC}=2.0V	-	-	180	ns
			V_{CC}=4.5V	-	-	42	ns

			V_{CC}=6.0V	-	-	38	ns
t_{THL}, t_{TLH}	Transition time	Q7, $\overline{Q7}$ output; See Figure 8-6	V_{CC}=2.0V	-	-	110	ns
			V_{CC}=4.5V	-	-	22	ns
			V_{CC}=6.0V	-	-	19	ns
t_W	Pulse width	CP input HIGH or LOW; See Figure 8-6	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
		$\overline{PL}$ input LOW; See Figure 8-7	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
t_{rec}	Recovery time	$\overline{PL}$ to CP, $\overline{CE}$; See Figure 8-7	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
t_{su}	Set-up time	DS to CP, $\overline{CE}$; See Figure 8-9	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; See Figure 8-9	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
		Dn to $\overline{PL}$; See Figure 8-10	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
t_h	Hold time	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$; See Figure 8-9	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; See Figure 8-9	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	V_{CC}=2.0V	5	-	-	MHz
			V_{CC}=4.5V	20	-	-	MHz
			V_{CC}=6.0V	24	-	-	MHz
CJ74HCT165							
t_{PLH}, t_{PHL}	Propagation delay	CP, $\overline{CE}$ to Q7, $\overline{Q7}$; See Figure 8-6	V_{CC}=4.5V	-	-	51	ns
		$\overline{PL}$ to Q7, $\overline{Q7}$; See Figure 8-7	V_{CC}=4.5V	-	-	60	ns
		D7 to Q7, $\overline{Q7}$; See Figure 8-8	V_{CC}=4.5V	-	-	42	ns
t_{THL}, t_{TLH}	Transition time	Q7, $\overline{Q7}$ output; See Figure 8-6	V_{CC}=4.5V	-	-	22	ns

t_W	Pulse width	CP input; See Figure 8-6	V_{CC}=4.5V	24	-	-	ns
		$\overline{PL}$ input; See Figure 8-7	V_{CC}=4.5V	30	-	-	ns
t_{rec}	Recovery time	$\overline{PL}$ to CP, $\overline{CE}$; See Figure 8-7	V_{CC}=4.5V	30	-	-	ns
t_{su}	Set-up time	DS to CP, $\overline{CE}$; See Figure 8-9	V_{CC}=4.5V	30	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; See Figure 8-9	V_{CC}=4.5V	30	-	-	ns
		Dn to $\overline{PL}$; See Figure 8-10	V_{CC}=4.5V	30	-	-	ns
t_h	Hold time	DS to CP, $\overline{CE}$ and Dn to $\overline{PL}$; See Figure 8-9	V_{CC}=4.5V	11	-	-	ns
		$\overline{CE}$ to CP and CP to $\overline{CE}$; See Figure 8-9	V_{CC}=4.5V	0	-	-	ns
f_{max}	Maximum frequency	CP input; See Figure 8-6	V_{CC}=4.5V	17	-	-	MHz

8 Detailed Description

8.1 Overview

The CJ74HC/HCT165 is 8-bit serial or parallel-in/serial-out shift registers. The device features a serial data input (DS), eight parallel data inputs (D0 to D7) and two complementary serial outputs (Q7 and /Q7). When the parallel load input (/PL) is LOW the data from D0 to D7 is loaded into the shift register asynchronously. When /PL is HIGH data enters the register serially at DS. When the clock enable input (/CE) is LOW data is shifted on the LOW-to-HIGH transitions of the CP input. A HIGH on /CE will disable the CP input. Inputs are overvoltage tolerant to 15V. This enables the device to be used in HIGH-to-LOW level shifting applications.

8.2 Functional Block Diagram

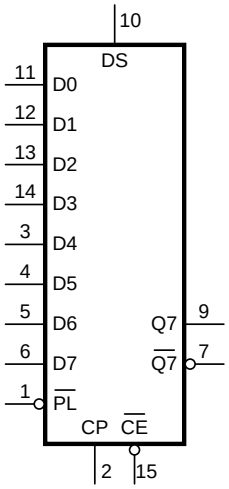


Figure 8-1 Logic symbol

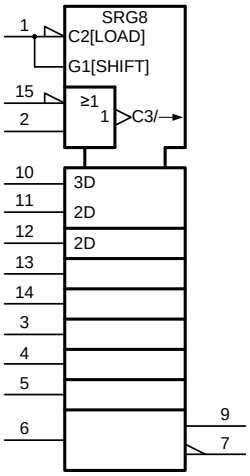


Figure 8-2 IEC logic symbol

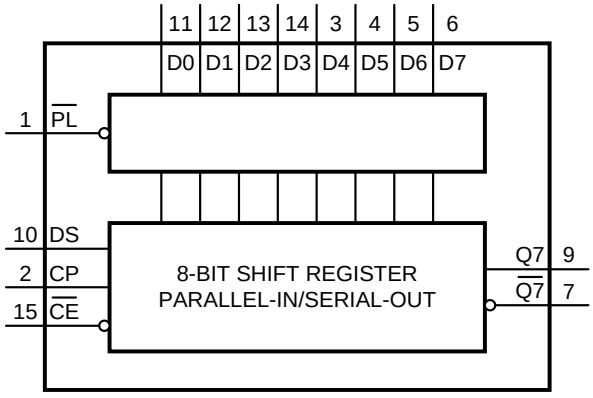


Figure 8-3 Functional diagram

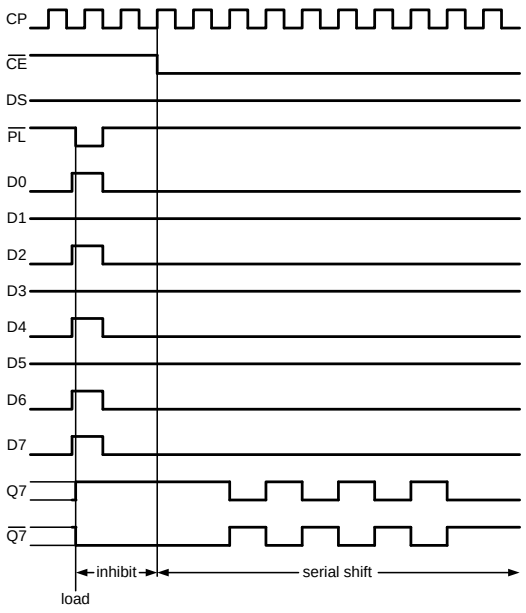


Figure 8-4 Timing diagram

8.3 Function Table(1)

OPERATING MODE	INPUT					QN REGISTER		OUTPUT	
	$\overline{PL}$	$\overline{CE}$	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7	$\overline{Q7}$
Parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
Serial shift	H	L	↑	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	L	↑	h	X	H	q0 to q5	q6	$\overline{q6}$
	H	↑	L	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	↑	L	h	X	H	q0 to q5	q6	$\overline{q6}$
Hold "do nothing"	H	H	X	X	X	q0	q1 to q6	q7	$\overline{q7}$
	H	X	H	X	X	q0	q1 to q6	q7	$\overline{q7}$

(1) H=HIGH voltage level; L=LOW voltage level; ↑=LOW-to-HIGH clock transition;
h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
q=state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;
X=don't care;
↑ =LOW-to-HIGH clock transition.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

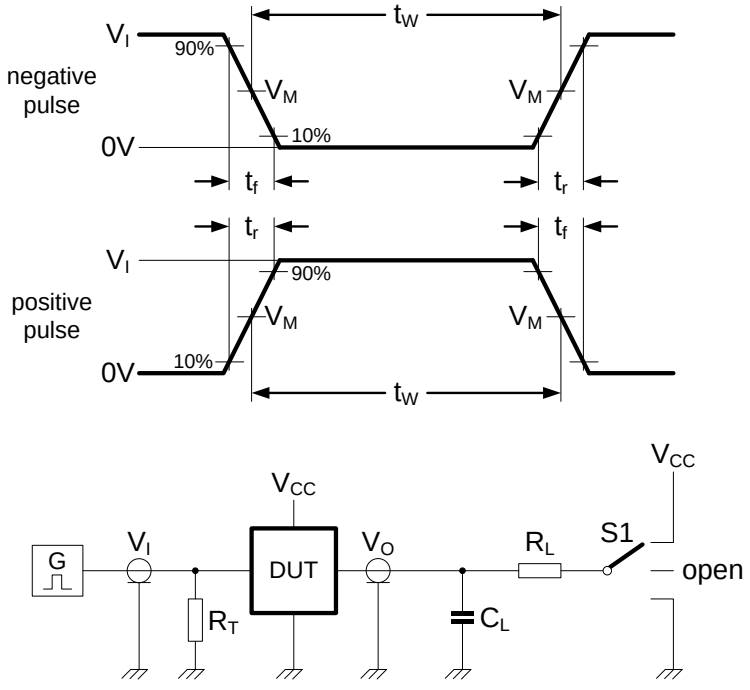


Figure 8-5 Test circuit for measuring switching times

Definitions for test circuit:

C_L=load capacitance including jig and probe capacitance.

R_T=termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L=Load resistance.

S1=Test selection switch.

8.4.2 AC Testing Waveforms

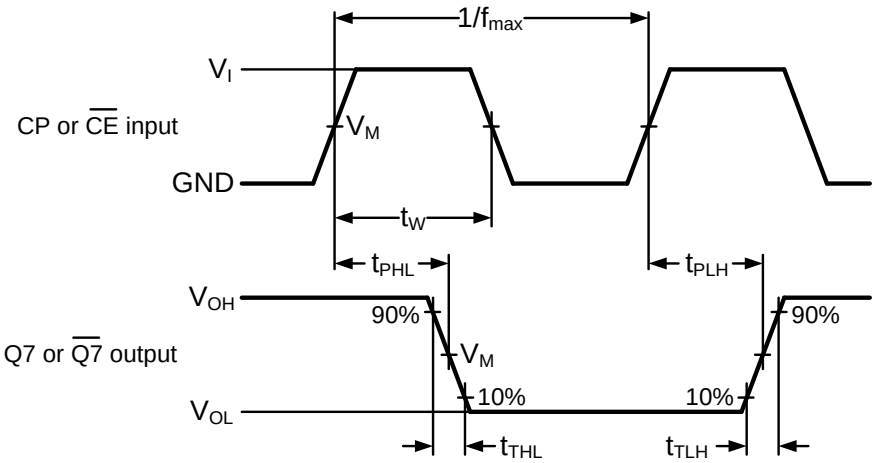


Figure 8-6 The clock (CP) or clock enable ($\overline{CE}$) to output (Q7 or $\overline{Q7}$) propagation delays, the clock pulse width, the maximum clock frequency and the output transition times

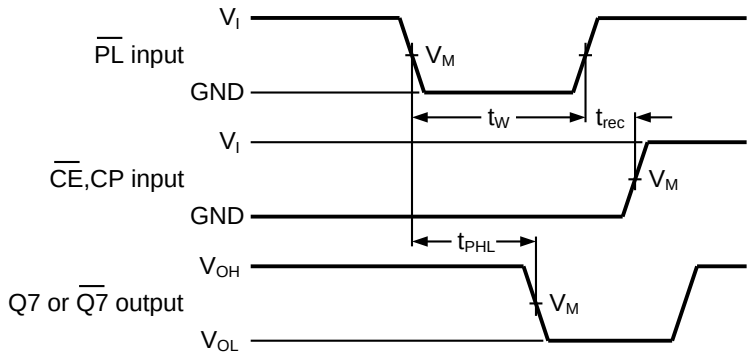


Figure 8-7 The parallel load ($\overline{PL}$) pulse width, the parallel load to output (Q7 or $\overline{Q7}$) propagation delays, the parallel load to clock (CP) and clock enable ($\overline{CE}$) recovery time

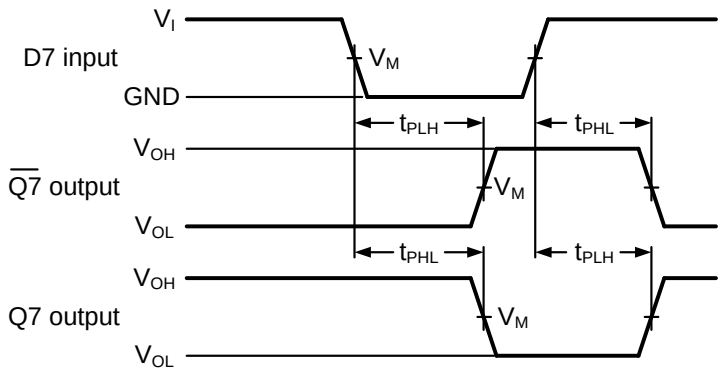
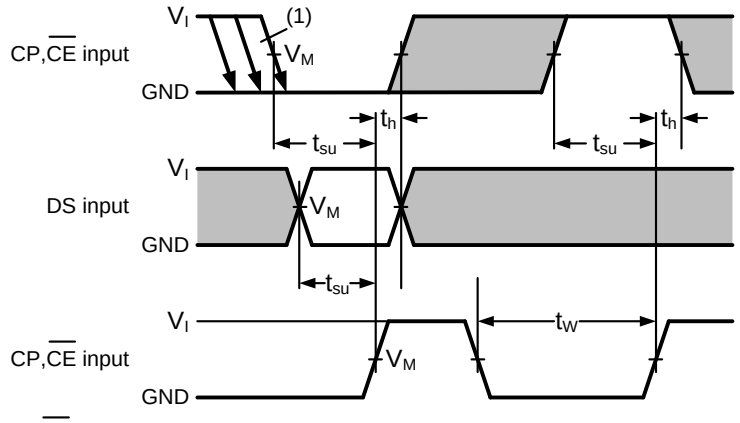


Figure 8-8 The data input (D7) to output (Q7 or $\overline{Q7}$) propagation delays when $\overline{PL}$ is LOW



(1) $\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW.

Figure 8-9 The set-up and hold times from the serial data input (DS) to the clock (CP) and clock enable ($\overline{CE}$) inputs, from the clock enable input ($\overline{CE}$) to the clock input (CP) and from the clock input (CP) to the clock enable input ($\overline{CE}$)

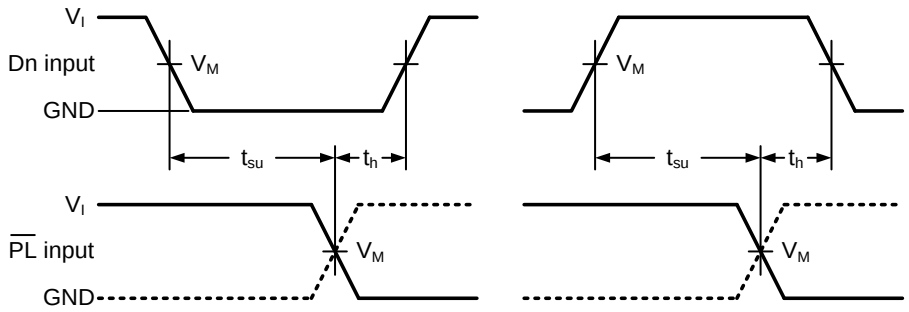


Figure 8-10 The set-up and hold times from the data inputs (Dn) to the parallel load input ($\overline{PL}$)

8.4.3 Measurement Points

TYPE	INPUT		OUTPUT
	V_I	V_M	V_M
CJ74HC165	V_{CC}	0.5xV_{CC}	0.5xV_{CC}
CJ74HCT165	3V	1.3V	1.3V

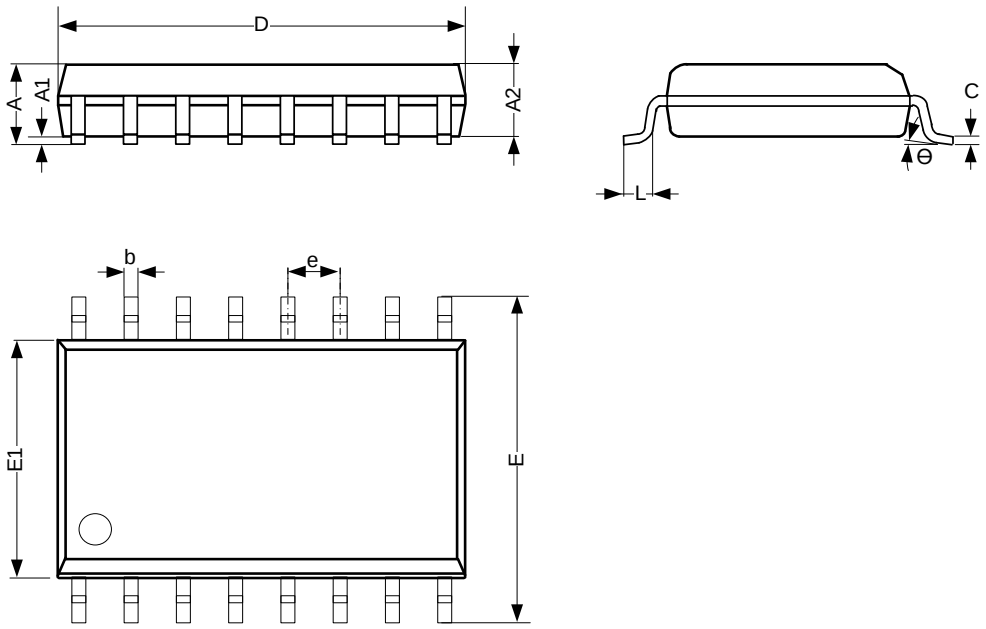
8.4.4 Test Data

TYPE	INPUT		LOAD		S1 POSITION
	V_I	t_r , t_f	C_L	R_L	t_{PHL}, t_{PLH}
CJ74HC165	V_{CC}	6.0ns	15pF, 50pF	1kΩ	Open
CJ74HCT165	3.0V	6.0ns	15pF, 50pF	1kΩ	Open

9 Mechanical Information

9.1 SOP16 Mechanical Information

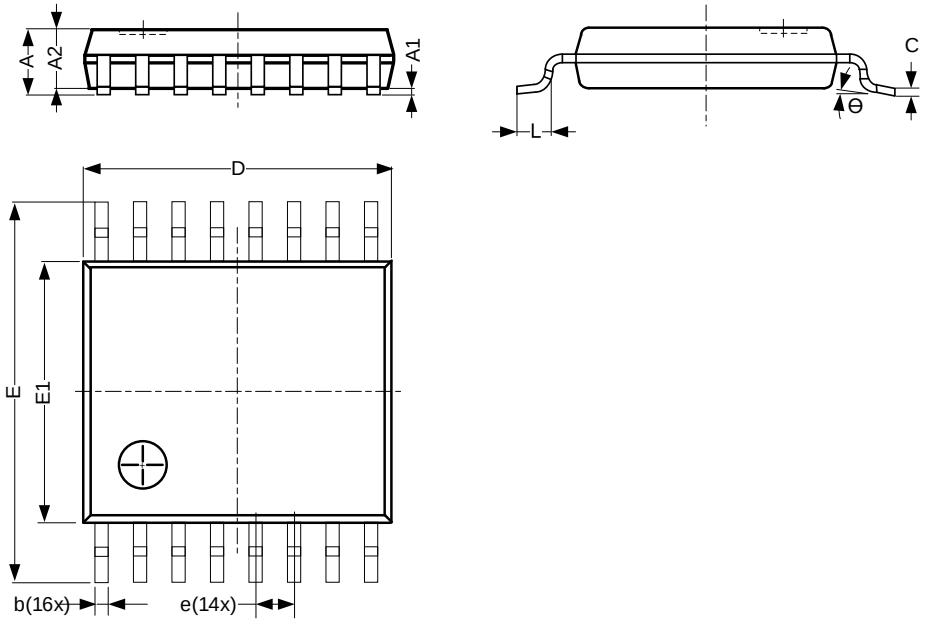
9.1.1 SOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.80
A1	0.10	-	0.25
A2	1.25	-	1.55
b	0.33	-	0.51
c	0.19	-	0.25
D	9.50	-	10.10
E	5.80	-	6.30
E1	3.70	-	4.10
e	1.27 BSC		
L	0.35	-	0.89
Θ	0°	-	8°
Unit: mm			

9.2 TSSOP16 Mechanical Information

9.2.1 TSSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

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