JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD.

8-channel Analog Multiplexer/Demultiplexer

CD4051H Logic

1 Introduction

The CD4051H is an 8-channel analog multiplexer/demultiplexer with three address inputs (S1 to S3), an active LOW enable input (/E), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z). The device contains eight bidirectional analog switches, each with one side connected to an independent input/output (Y0 to Y7) and the other side connected to a common input/output (Z). With /E LOW, one of the eight switches is selected (low-impedance ON-state) by S1 to S3. With /E HIGH, all switches are in the high-impedance OFF-state, independent of S1 to S3. If break before make is needed, then it is necessary to use the enable input.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S1 to S3, and /E). The V_{DD} to V_{SS} range is 3V to 18V. The analog inputs/outputs (Y0 to Y7, and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}-V_{EE} may not exceed 18V. Unused inputs must be connected to V_{DD}, V_{SS}, or another input. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground). V_{EE} and V_{SS} are the supply voltage connections for the switches.

2 Available Packages

PART NUMBER	PACKAGE
CD4051H	SOP16
	TSSOP16
	QFN3.5x2.5-16L

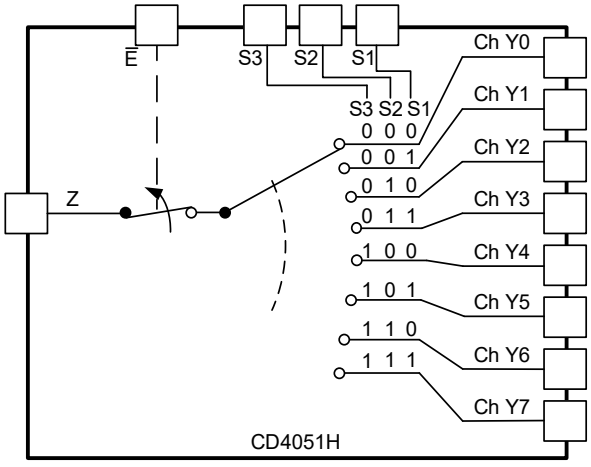
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range from 3V to 18V
- Fully static operation
- 5V, 10V and 18V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C

4 Applications

- Analog and digital multiplexing and demultiplexing
- Analog to digital and digital to analog conversion
- Signal gating
- Factory automation
- Televisions
- Appliances
- Consumer audio
- Programmable logic circuits
- Sensors



Functional diagrams

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CD4051HAEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units/Reel	Active
CD4051HBEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units/Reel	Active
CD4051HQEN	QFN3.5x2.5-16L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units/Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

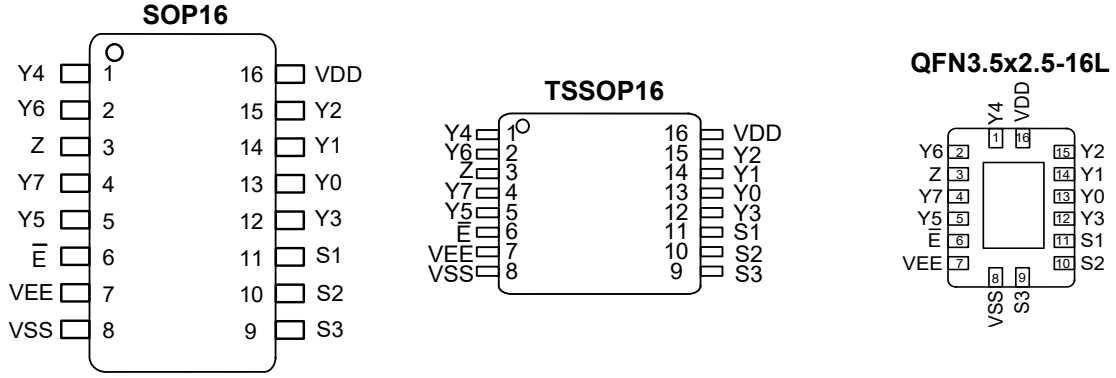


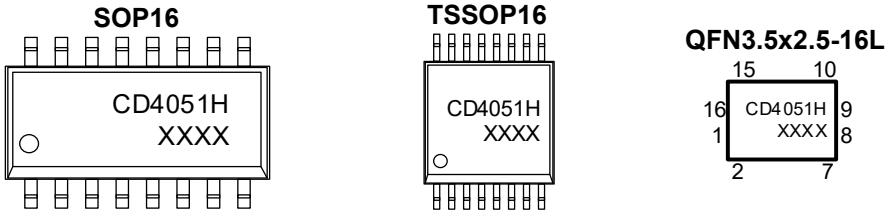
Figure 6-1 Pin configuration

6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	Y4	I/O	Independent input or output
2	Y6	I/O	Independent input or output
3	Z	I/O	Common output or input
4	Y7	I/O	Independent input or output
5	Y5	I/O	Independent input or output
6	$\overline{E}$	I	Enable input (active LOW)
7	VEE	P	Supply voltage
8	VSS	G	Ground (0V)
9	S3	I	Select input
10	S2	I	Select input
11	S1	I	Select input
12	Y3	I/O	Independent input or output
13	Y0	I/O	Independent input or output
14	Y1	I/O	Independent input or output
15	Y2	I/O	Independent input or output
16	VDD	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground.

6.3 Marking Information



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	Supply voltage	-	-0.5	+21	V
V_{EE}	Supply voltage	-	-21	+0.5	V
V_I	Input voltage	-	-0.5	V_{DD}+0.5	V
I_{IK}	Input clamping current	V_I<-0.5V or V_I>V_{DD}+0.5V	-	±10	mA
I_{IO}	Input/output current	-	-	±10	mA
I_{DD}	Supply current	-	-	50	mA
T_{stg}	Storage temperature	-	-65	+150	°C
T_{amb}	Ambient temperature	-	-40	+125	°C
P_{tot}	Total power dissipation	-	-	500	mW
P	Device dissipation	Per output transistor	-	100	mW
T_L	Soldering temperature	10s	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	-	3	-	18	V
V_{EE}	Supply voltage	-	-15	-	0	V
V_{DD}-V_{EE}	Supply voltage	-	3	-	18	V
V_I	Input voltage	-	0	-	V_{DD}	V
T_{amb}	Ambient temperature	In free air	-40	-	+125	°C
Δt/ΔV	Input transition rise and fall rate	V_{DD}=5V	-	-	3.75	us/V
		V_{DD}=10V	-	-	0.5	us/V
		V_{DD}=18V	-	-	0.08	us/V

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V H1BM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=25°C, V_{SS}=V_{EE}=0V; V_I=V_{SS} or V_{DD}, I_{SW}=200uA, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		T_{amb}=25°C			UNIT
				MIN.	TYP.	MAX.	
V_{IH}	HIGH-level input voltage	|I_O|<1uA	V_{DD}=5V	3.5	-	-	V
			V_{DD}=10V	7.0	-	-	V
			V_{DD}=18V	12.6	-	-	V
V_{IL}	LOW-level input voltage	|I_O|<1uA	V_{DD}=5V	-	-	1.5	V
			V_{DD}=10V	-	-	3.0	V
			V_{DD}=18V	-	-	5.4	V
I_{DD}	Supply current	I_O=0A	V_{DD}=5V	-	-	5	uA
			V_{DD}=10V	-	-	10	uA
			V_{DD}=18V	-	-	20	uA
I_I	Input leakage current	V_{DD}=18V		-	-	±1.0	uA
$I_{S(OFF)}$	OFF-state leakage current	V_{DD}=18V	Z port; All channels OFF; See Figure 8-6	-	-	±1.0	uA
			Y port; Per channel; See Figure 8-7	-	-	±1.0	uA
$R_{ON(peak)}$	ON resistance (peak)	V_I=0V to V_{DD}-V_{EE}; See Figure 8-8 and Figure 8-9	V_{DD}-V_{EE}=5V	-	117	836	Ω
			V_{DD}-V_{EE}=10V	-	58	178	Ω
			V_{DD}-V_{EE}=15V	-	41	120	Ω
			V_{DD}-V_{EE}=20V	-	36	105	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_I=0V; See Figure 8-8 and Figure 8-9	V_{DD}-V_{EE}=5V	-	44	130	Ω
			V_{DD}-V_{EE}=10V	-	29	93	Ω
			V_{DD}-V_{EE}=15V	-	24	69	Ω
			V_{DD}-V_{EE}=20V	-	22	63	Ω
		V_I=V_{DD}-V_{EE}; See Figure 8-8 and Figure 8-9	V_{DD}-V_{EE}=5V	-	82	249	Ω
			V_{DD}-V_{EE}=10V	-	51	157	Ω
			V_{DD}-V_{EE}=15V	-	41	127	Ω
			V_{DD}-V_{EE}=20V	-	36	112	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_I=0V to V_{DD}-V_{EE}; See Figure 8-8	V_{DD}-V_{EE}=5V	-	25	-	Ω
			V_{DD}-V_{EE}=10V	-	10	-	Ω
			V_{DD}-V_{EE}=15V	-	5	-	Ω
			V_{DD}-V_{EE}=20V	-	5	-	Ω
C_I	Input capacitance	Sn, $\overline{E}$ inputs		-	-	7.5	pF

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, V_{SS}=V_{EE}=0V; V_I=V_{SS} or V_{DD}, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		T_{amb}=-40°C		T_{amb}=+85°C		T_{amb}=+125°C		UNIT
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage	$\|I_O\|$<1uA	V_{DD}=5V	3.5	-	3.5	-	3.5	-	V
			V_{DD}=10V	7.0	-	7.0	-	7.0	-	V
			V_{DD}=18V	12.6	-	12.6	-	12.6	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$<1uA	V_{DD}=5V	-	1.5	-	1.5	-	1.5	V
			V_{DD}=10V	-	3.0	-	3.0	-	3.0	V
			V_{DD}=18V	-	5.4	-	5.4	-	5.4	V
I_{DD}	Supply current	I_O=0A	V_{DD}=5V	-	5	-	150	-	150	uA
			V_{DD}=10V	-	10	-	300	-	300	uA
			V_{DD}=18V	-	20	-	600	-	600	uA
I_I	Input leakage current	V_{DD}=18V		-	±1.0	-	±1.0	-	±1.0	uA

7.4.3 AC Characteristics 1

T_{amb}=25°C, V_{EE}=V_{SS}=0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{PHL}	HIGH to LOW propagation delay time	Yn to Z; Z to Yn; See Figure 8-11	V_{DD}=5V	-	15	30	ns
			V_{DD}=10V	-	5	10	ns
			V_{DD}=18V	-	5	10	ns
		Sn to Yn, Z; See figure 8-12	V_{DD}=5V	-	150	300	ns
			V_{DD}=10V	-	60	120	ns
			V_{DD}=18V	-	45	90	ns
t_{PLH}	LOW to HIGH propagation delay	Yn to Z; Z to Yn; See Figure 8-11	V_{DD}=5V	-	15	30	ns
			V_{DD}=10V	-	5	10	ns
			V_{DD}=18V	-	5	10	ns
		Sn to Yn, Z; See Figure 8-12	V_{DD}=5V	-	150	300	ns
			V_{DD}=10V	-	65	130	ns
			V_{DD}=18V	-	45	90	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{E}$ to Yn, Z; See Figure 8-13	V_{DD}=5V	-	120	240	ns
			V_{DD}=10V	-	90	180	ns
			V_{DD}=18V	-	85	170	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{E}$ to Yn, Z; See Figure 8-13	V_{DD}=5V	-	145	290	ns
			V_{DD}=10V	-	120	240	ns
			V_{DD}=18V	-	115	230	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{E}$ to Yn, Z; See Figure 8-13	V_{DD}=5V	-	140	280	ns
			V_{DD}=10V	-	55	110	ns

			V_{DD}=18V	-	40	80	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{E}$ to Yn, Z; See Figure 8-13	V_{DD}=5V	-	140	280	ns
			V_{DD}=10V	-	55	110	ns
			V_{DD}=18V	-	40	80	ns

7.4.4 AC Characteristics 2

T_{amb}=25°C, V_{EE}=V_{SS}=0V, V_I=0.5V_{DD} (p-p), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
THD	Total harmonic distortion	See Figure 8-14; R_L=10kΩ; C_L=15pF; Channel ON; f_i=1kHz	V_{DD}=5V	-	0.25	-	%
			V_{DD}=10V	-	0.04	-	%
			V_{DD}=18V	-	0.04	-	%
$f_{(-3dB)}$	-3dB frequency response	See Figure 8-15; R_L=1kΩ; C_L=5pF; Channel ON;	V_{DD}=5V	-	13	-	MHz
			V_{DD}=10V	-	40	-	MHz
			V_{DD}=18V	-	70	-	MHz
α_{iso}	Isolation (OFF-state)	See Figure 8-16; f_i=1MHz; R_L=1kΩ; C_L=5pF; Channel OFF; V_{DD}=10V		-	-50	-	dB
V_{ct}	Crosstalk voltage	Digital inputs to switch; See Figure 8-17; R_L=10kΩ; C_L=15pF; $\overline{E}$ or Sn=V_{DD} (square-wave); V_{DD}=10V		-	50	-	mV
Xtalk	Crosstalk	Between switches; See Figure 8-18; f_i=1MHz; R_L=1kΩ; V_{DD}=10V		-	-50	-	dB

(1) f_i is biased at 0.5V_{DD}; V_I=0.5V_{DD} (p-p).

8 Detailed Description

8.1 Overview

The CD4051H is an 8-channel analog multiplexer/demultiplexer with three address inputs (S1 to S3), an active LOW enable input (/E), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z). The device contains eight bidirectional analog switches, each with one side connected to an independent input/output (Y0 to Y7) and the other side connected to a common input/output (Z). With /E LOW, one of the eight switches is selected (low-impedance ON-state) by S1 to S3. With /E HIGH, all switches are in the high-impedance OFF-state, independent of S1 to S3. If break before make is needed, then it is necessary to use the enable input.

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8.2 Functional Block Diagram

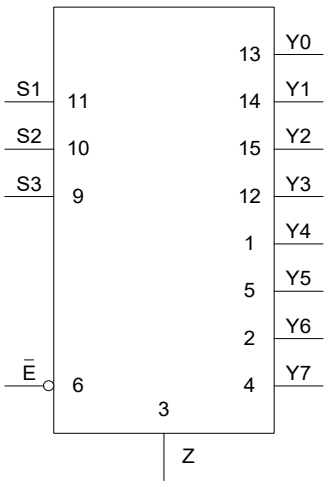


Figure 8-1 Logic symbol

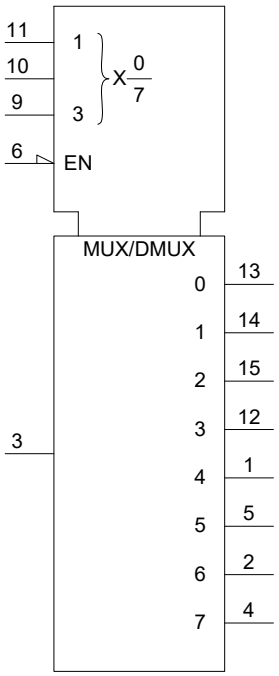


Figure 8-2 IEC logic symbol

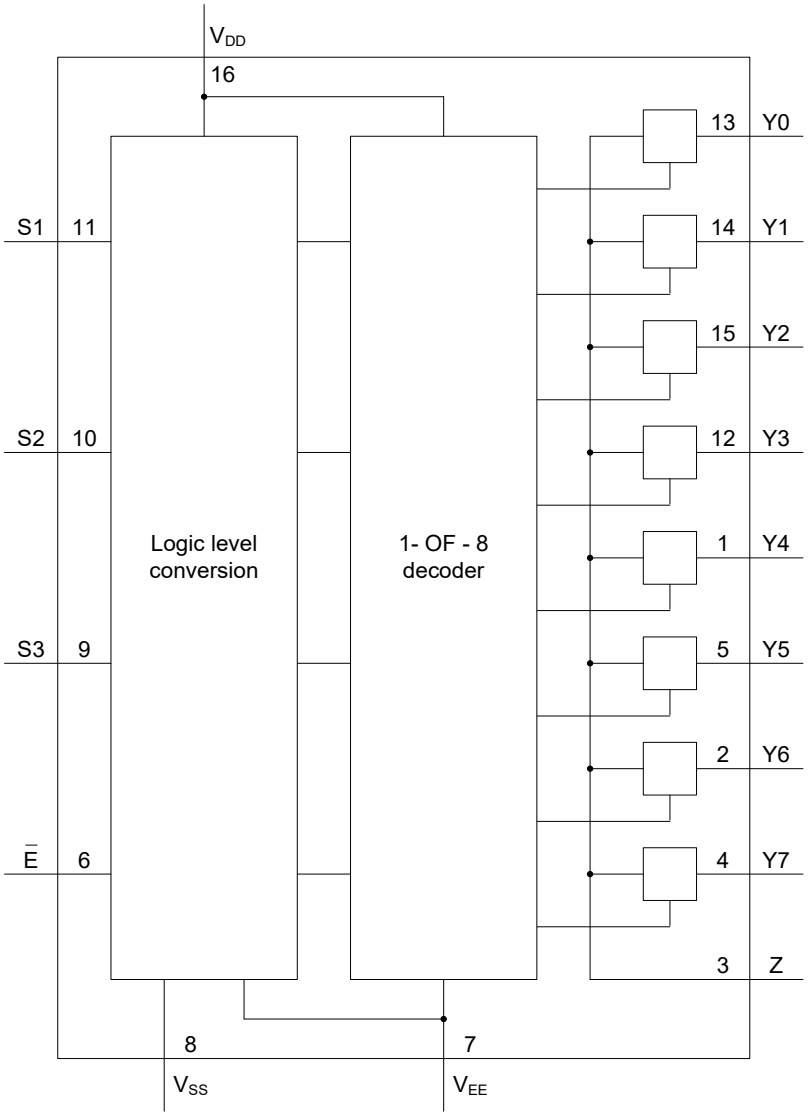


Figure 8-3 Functional diagram

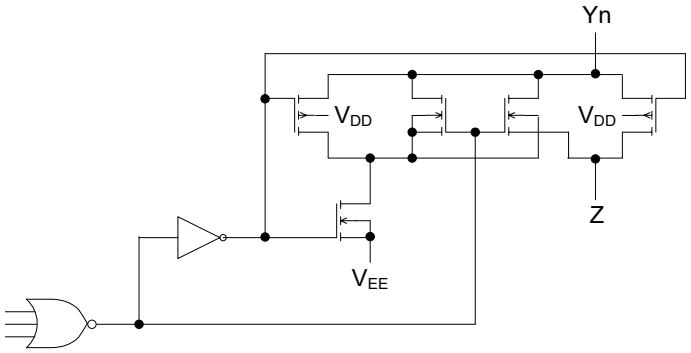


Figure 8-4 Schematic diagram (one switch)

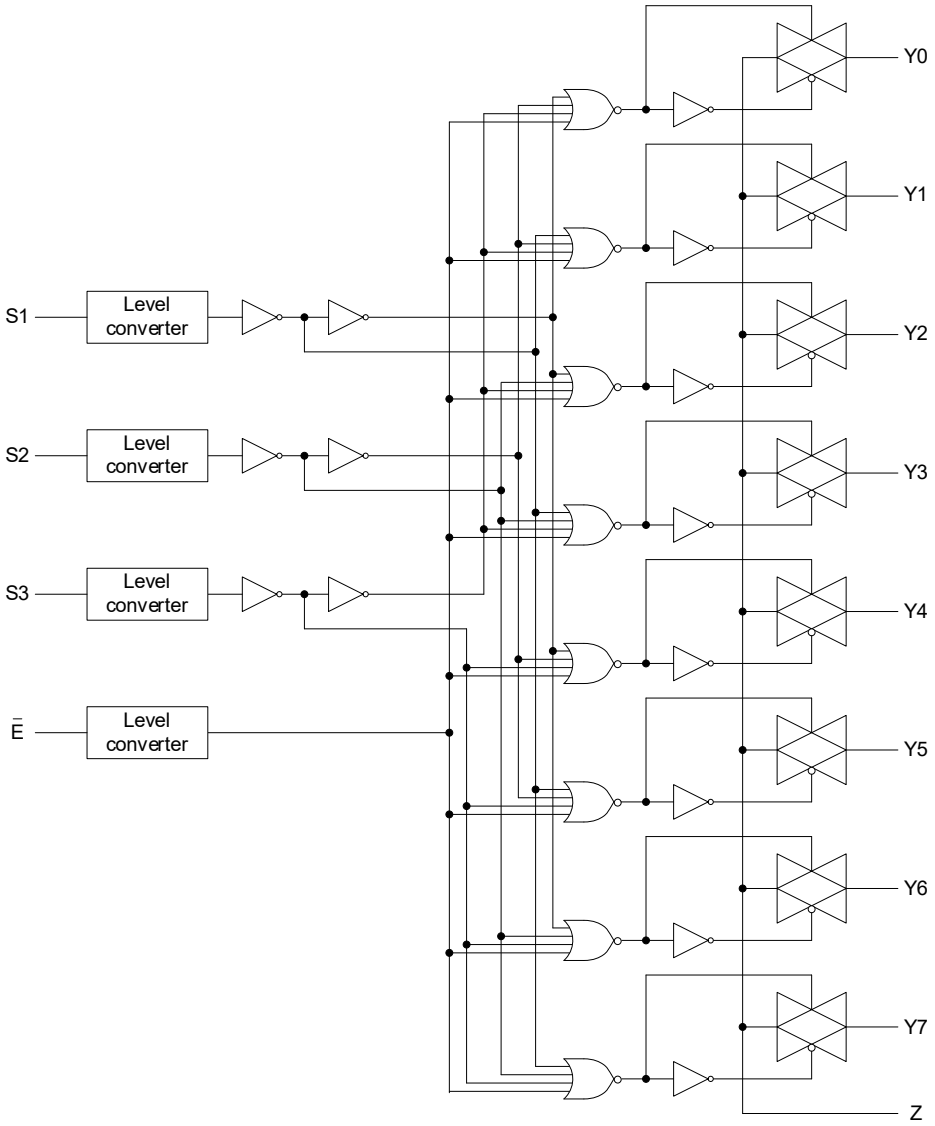


Figure 8-5 Logic diagram

8.3 Function Table(1)

INPUT				CHANNEL ON
$\bar{E}$	S3	S2	S1	
L	L	L	L	Y0 to Z
L	L	L	H	Y1 to Z
L	L	H	L	Y2 to Z
L	L	H	H	Y3 to Z
L	H	L	L	Y4 to Z
L	H	L	H	Y5 to Z
L	H	H	L	Y6 to Z
L	H	H	H	Y7 to Z
H	X	X	X	Switches off

(1) H=HIGH voltage level; L=LOW voltage level; X=don't care.

8.4 Testing Circuit

8.4.1 DC Testing Circuit

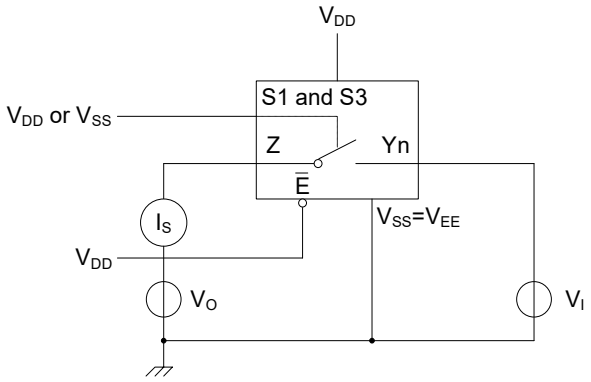


Figure 8-6 Test circuit for measuring OFF-state leakage current Z port

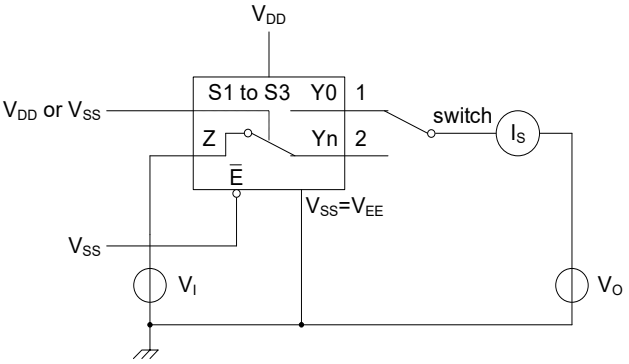
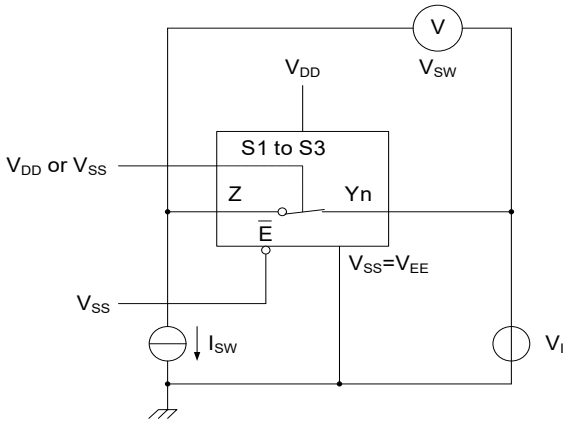


Figure 8-7 Test circuit for measuring OFF-state leakage current Yn port

8.4.2 ON Resistance Testing Circuit



$R_{ON}=V_{SW}/I_{SW}$.

Figure 8-8 Test circuit for measuring R_{ON}

8.4.3 ON Resistance Waveforms

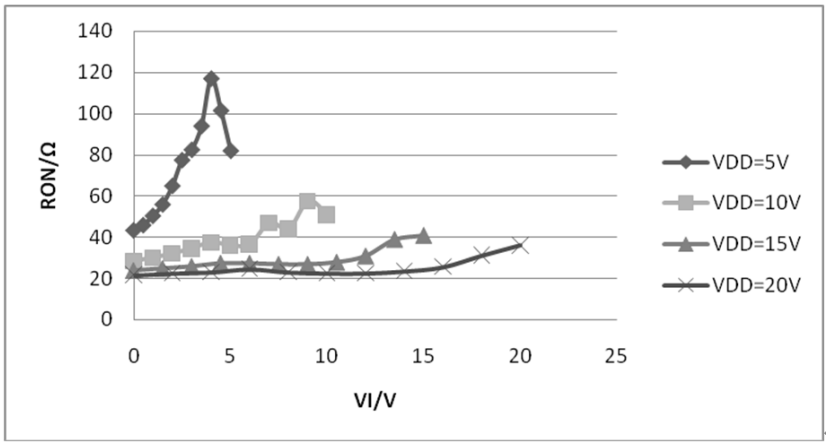


Figure 8-9 Typical R_{ON} as a function of input voltage

8.4.4 AC Testing Circuit 1

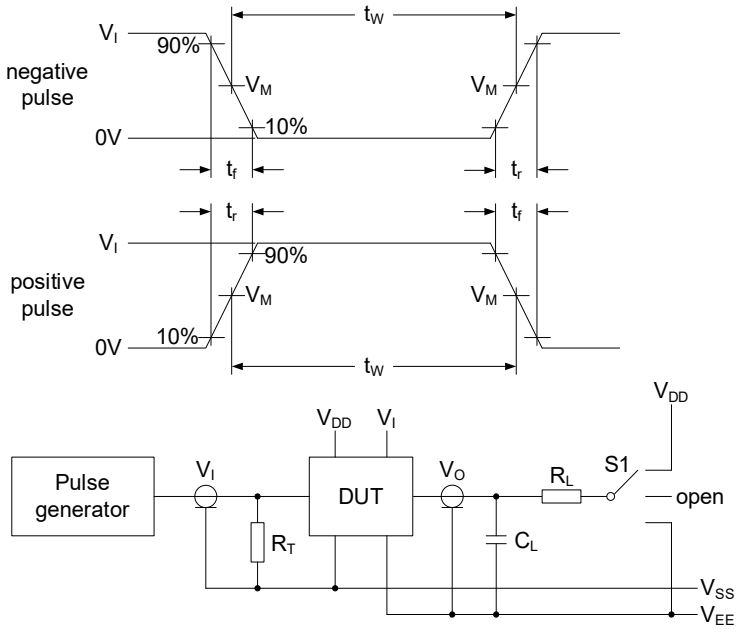


Figure 8-10 Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L=Load resistance.

8.4.5 AC Testing Waveforms

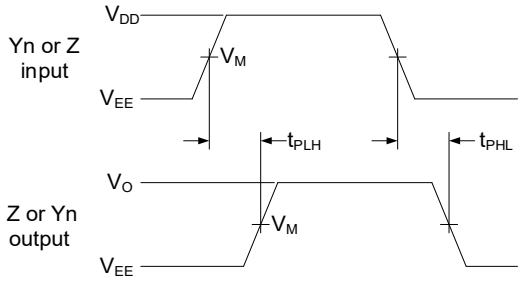


Figure 8-11 Yn, Z to Z, Yn propagation delays

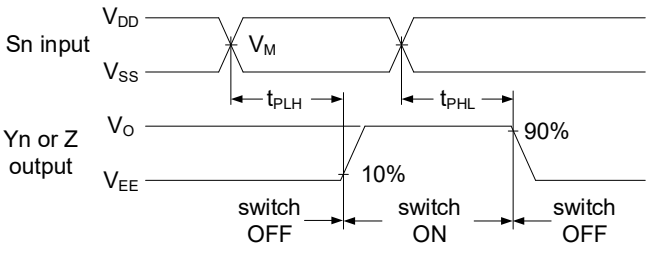


Figure 8-12 Sn to Yn, Z propagation delays

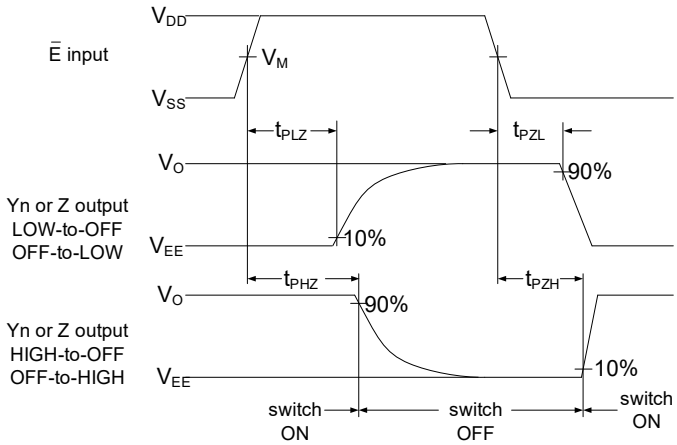


Figure 8-13 Enable and disable times

8.4.6 AC Testing Circuit 2

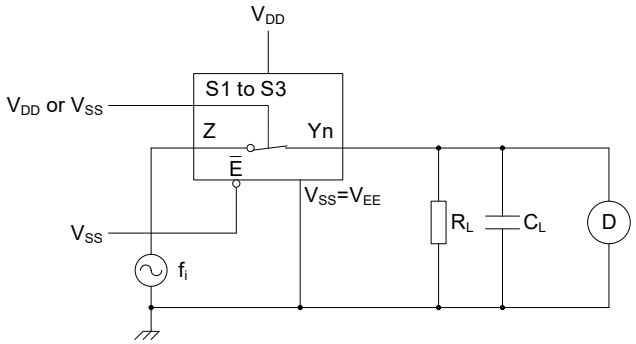


Figure 8-14 Test circuit for measuring total harmonic distortion

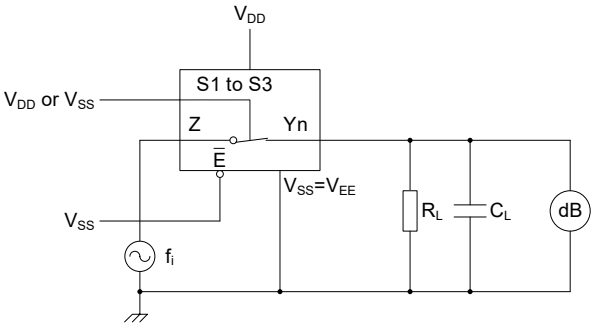


Figure 8-15 Test circuit for measuring frequency response

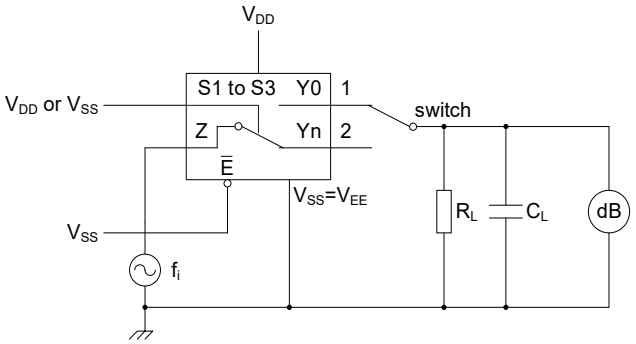
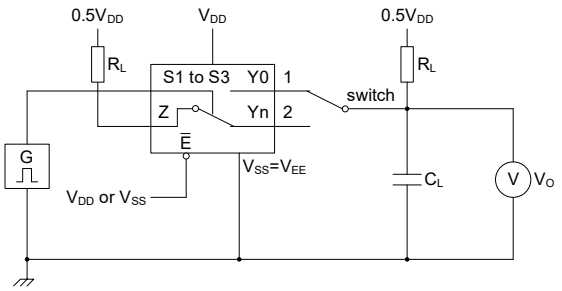
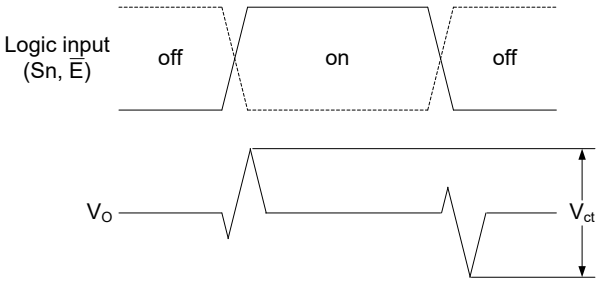


Figure 8-16 Test circuit for measuring isolation (OFF-state)

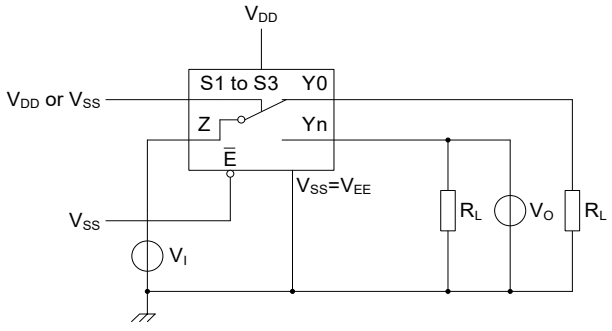


a. Test circuit

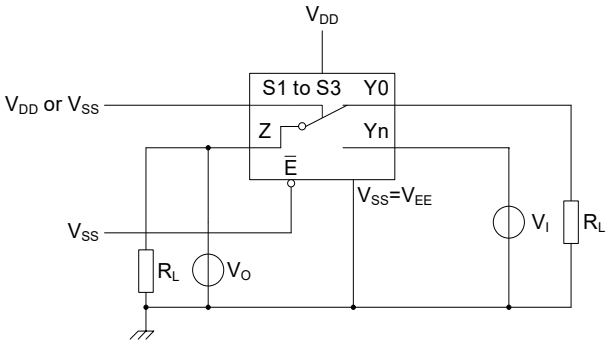


b. Input and output pulse definitions

Figure 8-17 Test circuit for measuring crosstalk voltage between digital inputs and switch



a. Switch closed condition



b. Switch open condition

Figure 8-18 Test circuit for measuring crosstalk between switches

8.4.7 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{DD}	V_M	V_M
5V to 18V	0.5xV_{DD}	0.5xV_{DD}

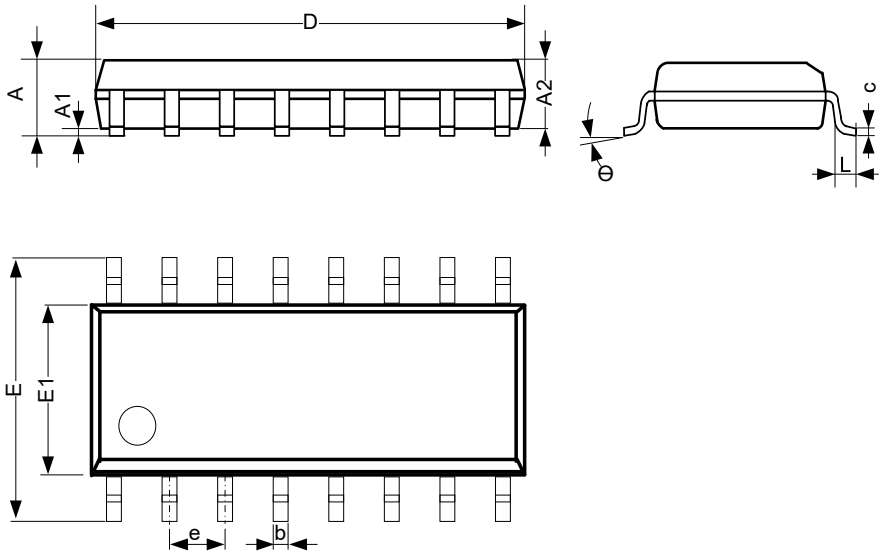
8.4.8 Test Data

INPUT				LOAD		S1 POSITION				
Yn, Z	Sn and $\overline{E}$	t_r, t_f	V_M	C_L	R_L	t_{PHL}	t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}	Other
V_{DD} or V_{EE}	V_{DD} or V_{SS}	≤20ns	0.5xV_{DD}	50pF	10kΩ	V_{DD} or V_{EE}	V_{EE}	V_{EE}	V_{DD}	V_{EE}

9 Mechanical Information

9.1 SOP16 Mechanical Information

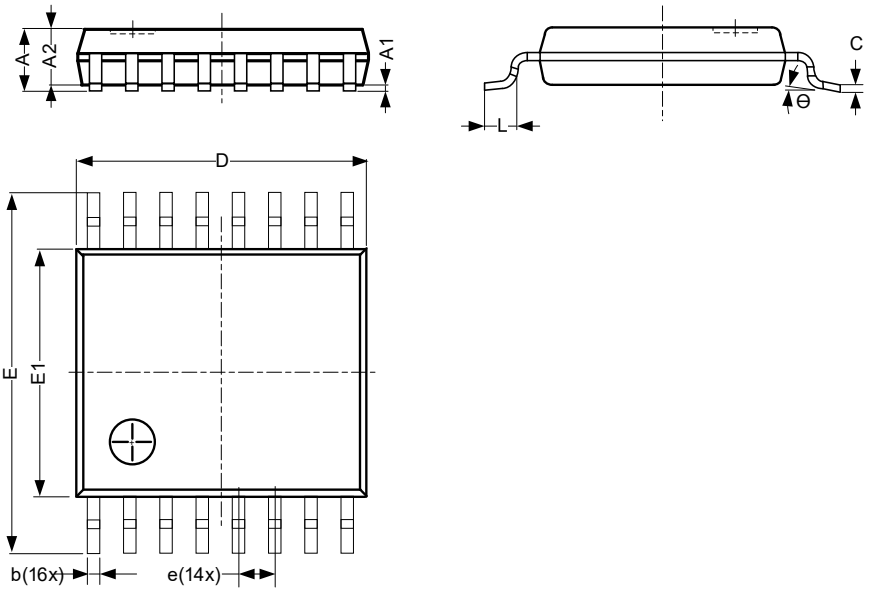
9.1.1 SOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.80
A1	0.10	-	0.25
A2	1.25	-	1.55
b	0.33	-	0.51
c	0.19	-	0.25
D	9.50	-	10.10
E	5.80	-	6.30
E1	3.70	-	4.10
e	1.27 BSC		
L	0.35	-	0.89
Θ	0°	-	8°
Unit: mm			

9.2 TSSOP16 Mechanical Information

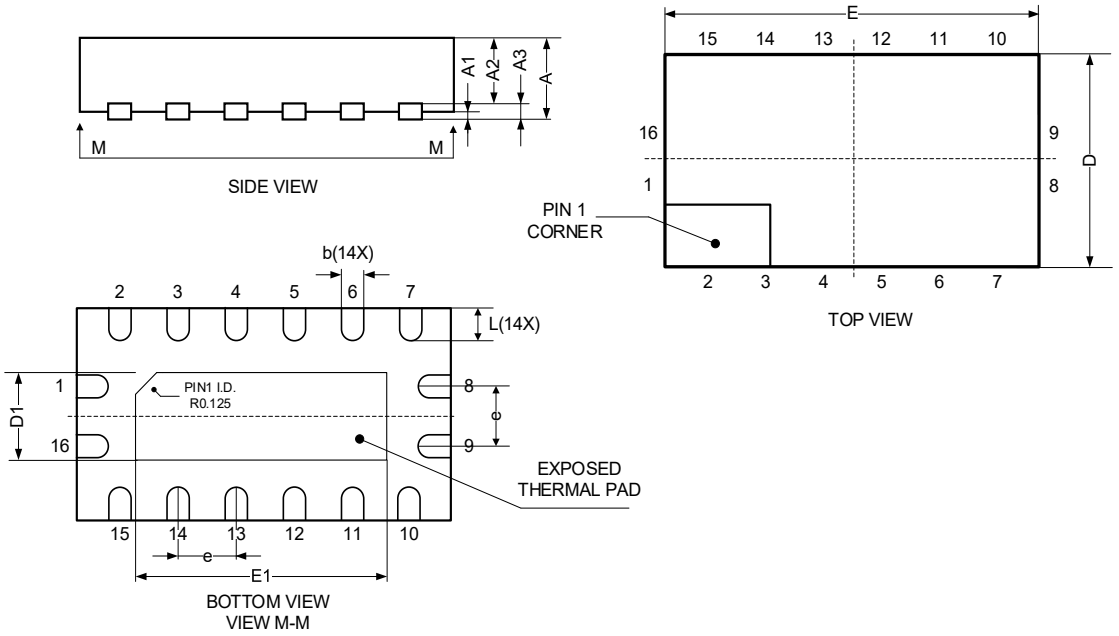
9.2.1 TSSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
Θ	0°	-	8°
Unit: mm			

9.3 QFN3.5x2.5-16L Mechanical Information

9.3.1 QFN3.5x2.5-16L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.80	-	1.00
A1	0.00	-	0.05
A2	0.60	-	0.70
A3	-	0.20	-
D	2.40	-	2.60
E	3.40	-	3.60
e	0.50 BSC		
b	0.18	-	0.30
L	0.30	-	0.50
D1	0.85	-	1.15
E1	1.85	-	2.15
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

June, 2025: rev - 1.1, Correct Figure 8-5.

July, 2025: rev - 1.2, Change marking information.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

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