Quad 2-input NAND Schmitt Gate

CD4093 Logic

1 Introduction

The CD4093 is a quad two-input NAND gate. Each input has a Schmitt trigger circuit.

The gate switches at different points for positive-going and negative-going signals. The difference between the positive voltage (V_{T+}) and the negative voltage (V_{T-}) is defined as hysteresis voltage (V_H).

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS}(usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2 Available Packages

PART NUMBER	PACKAGE
CD4093	SOP14
	TSSOP14

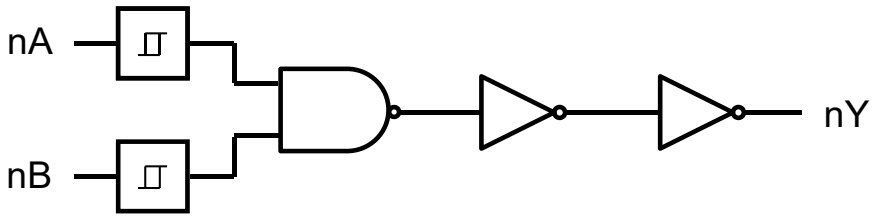
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range from 3V to 15V
- Schmitt trigger input discrimination
- Fully static operation
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C

4 Applications

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic



Logic diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CD4093ADN	SOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CD4093BDN	TSSOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

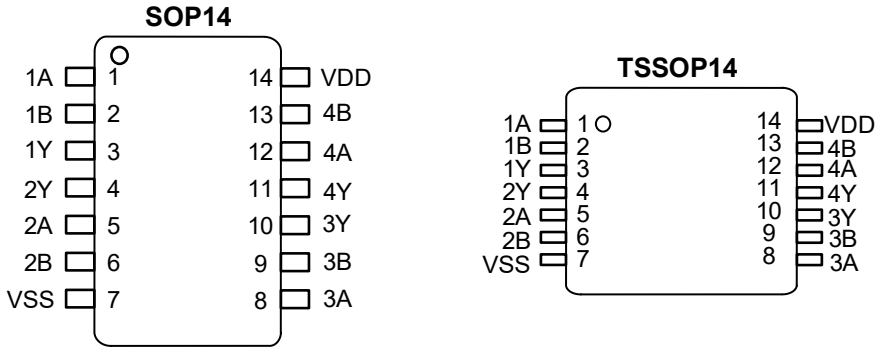


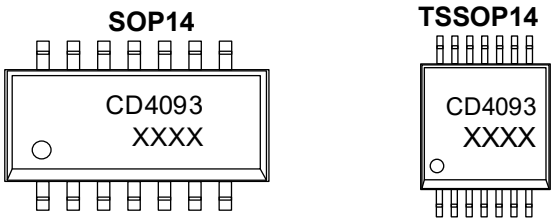
Figure 6-1 Pin configuration

6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	1A	I	Data input
2	1B	I	Data input
3	1Y	O	Data output
4	2Y	O	Data output
5	2A	I	Data input
6	2B	I	Data input
7	VSS	G	Ground (0V)
8	3A	I	Data input
9	3B	I	Data input
10	3Y	O	Data output
11	4Y	O	Data output
12	4A	I	Data input
13	4B	I	Data input
14	VDD	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{DD}	Supply voltage	-		-0.5	+18	V
I_{IK}	DC input current	Any one input		-	±10	mA
V_I	Input voltage	All inputs		-0.5	V_{DD}+0.5	V
T_{stg}	Storage temperature	-		-65	+150	°C
P_{tot}	Total power dissipation	-		-	500	mW
P	Device dissipation	Per output transistor		-	100	mW
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	-	3	-	15	V
T_{amb}	Ambient temperature	In free air	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM)(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=25°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			T_{amb}=25°C			UNIT
		V_O	V_{IN}	V_{DD}	MIN.	TYP.	MAX.	
I_{DD}	Supply current	-	0/5	5	-	-	1	uA
		-	0/10	10	-	-	2	uA
		-	0/15	15	-	-	4	uA
I_{OL}	LOW-level output current	0.4	0/5	5	0.51	1	-	mA
		0.5	0/10	10	1.3	2.6	-	mA
		1.5	0/15	15	3.4	6.8	-	mA
I_{OH}	HIGH-level output current	4.6	0/5	5	-0.51	-1	-	mA
		2.5	0/5	5	-1.6	-3.2	-	mA
		9.5	0/10	10	-1.3	-2.6	-	mA
		13.5	0/15	15	-3.4	-6.8	-	mA
V_{OL}	LOW-level output voltage	-	0/5	5	-	0	0.05	V
		-	0/10	10	-	0	0.05	V
		-	0/15	15	-	0	0.05	V
V_{OH}	HIGH-level output voltage	-	0/5	5	4.95	5	-	V
		-	0/10	10	9.95	10	-	V
		-	0/15	15	14.95	15	-	V
I_I	Input leakage current	-	0/15	15	-	-	±1	uA

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			T_{amb}=-40°C		T_{amb}=+85°C		T_{amb}=+125°C		UNIT
		V_O	V_{IN}	V_{DD}	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
I_{DD}	Supply current	-	0/5	5	-	1	-	30	-	30	uA
		-	0/10	10	-	2	-	60	-	60	uA
		-	0/15	15	-	4	-	120	-	120	uA
I_{OL}	LOW-level output current	0.4	0/5	5	0.61	-	0.42	-	0.36	-	mA
		0.5	0/10	10	1.5	-	1.1	-	0.9	-	mA
		1.5	0/15	15	4	-	2.8	-	2.4	-	mA
I_{OH}	HIGH-level output current	4.6	0/5	5	-0.61	-	-0.42	-	-0.36	-	mA
		2.5	0/5	5	-1.8	-	-1.3	-	-1.15	-	mA
		9.5	0/10	10	-1.5	-	-1.1	-	-0.9	-	mA
		13.5	0/15	15	-4	-	-2.8	-	-2.4	-	mA
V_{OL}	LOW-level output voltage	-	0/5	5	-	0.05	-	0.05	-	0.05	V
		-	0/10	10	-	0.05	-	0.05	-	0.05	V
		-	0/15	15	-	0.05	-	0.05	-	0.05	V
V_{OH}	HIGH-level output voltage	-	0/5	5	4.95	-	4.95	-	4.95	-	V
		-	0/10	10	9.95	-	9.95	-	9.95	-	V
		-	0/15	15	14.95	-	14.95	-	14.95	-	V
I_I	Input leakage current	-	0/15	15	-	±1	-	±1	-	±1	uA

7.4.3 AC Characteristics

T_{amb}=25°C, V_{SS}=0V, t_r, t_f=20ns, C_L=50pF, R_L=200kΩ, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t_{PHL}, t_{PLH}	Propagation delay time	See Figure 8-4	V_{DD}=5V	-	45	100	ns
			V_{DD}=10V	-	25	60	ns
			V_{DD}=15V	-	20	50	ns
t_{THL}, t_{TLH}	Transition time	See Figure 8-4	V_{DD}=5V	-	30	70	ns
			V_{DD}=10V	-	25	60	ns
			V_{DD}=15V	-	20	50	ns
C_I	Input capacitance	Any input		-	5	7.5	pF

7.4.4 Transfer Characteristics 1

T_{amb}=25°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			T_{amb}=25°C			UNIT
		V_O	V_{IN}	V_{DD}	MIN.	TYP.	MAX.	
V_{T+}	Positive-going threshold voltage	-	(1)	5	2.2	2.9	3.6	V
		-	(1)	10	4.6	5.9	7.1	V
		-	(1)	15	6.8	8.8	10.8	V
		-	(2)	5	2.6	3.3	4	V
		-	(2)	10	5.6	7	8.2	V
		-	(2)	15	6.3	9.4	12.7	V
V_{T-}	Negative-going threshold voltage	-	(1)	5	0.9	1.9	2.8	V
		-	(1)	10	2.5	3.9	5.2	V
		-	(1)	15	4	5.8	7.4	V
		-	(2)	5	1.4	2.3	3.2	V
		-	(2)	10	3.4	5.1	6.6	V
		-	(2)	15	4.8	7.3	9.6	V
V_H	Hysteresis voltage	-	(1)	5	0.3	0.9	1.6	V
		-	(1)	10	1.2	2.3	3.4	V
		-	(1)	15	1.6	3.5	5	V
		-	(2)	5	0.3	0.9	1.6	V
		-	(2)	10	1.2	2.3	3.4	V
		-	(2)	15	1.6	3.5	5	V

(1) Input on terminals 1, 5, 8, 12 or 2, 6, 9, 13; other inputs to V_{DD}.

(2) Input on terminals 1 and 2, 5 and 6, 8 and 9 or 12 and 13; other inputs to V_{DD}.

(3) See Figure 8-5 and Figure 8-6.

7.4.5 Transfer Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			T_{amb}=-40°C		T_{amb}=+85°C		T_{amb}=+125°C		UNIT
		V_O	V_{IN}	V_{DD}	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{T+}	Positive-going threshold voltage	-	(1)	5	2.2	3.6	2.2	3.6	2.2	3.6	V
		-	(1)	10	4.6	7.1	4.6	7.1	4.6	7.1	V
		-	(1)	15	6.8	10.8	6.8	10.8	6.8	10.8	V
		-	(2)	5	2.6	4	2.6	4	2.6	4	V
		-	(2)	10	5.6	8.2	5.6	8.2	5.6	8.2	V
		-	(2)	15	6.3	12.7	6.3	12.7	6.3	12.7	V
V_{T-}	Negative-going threshold voltage	-	(1)	5	0.9	2.8	0.9	2.8	0.9	2.8	V
		-	(1)	10	2.5	5.2	2.5	5.2	2.5	5.2	V
		-	(1)	15	4	7.4	4	7.4	4	7.4	V
		-	(2)	5	1.4	3.2	1.4	3.2	1.4	3.2	V
		-	(2)	10	3.4	6.6	3.4	6.6	3.4	6.6	V
		-	(2)	15	4.8	9.6	4.8	9.6	4.8	9.6	V
V_H	Hysteresis voltage	-	(1)	5	0.3	1.6	0.3	1.6	0.3	1.6	V
		-	(1)	10	1.2	3.4	1.2	3.4	1.2	3.4	V
		-	(1)	15	1.6	5	1.6	5	1.6	5	V
		-	(2)	5	0.3	1.6	0.3	1.6	0.3	1.6	V
		-	(2)	10	1.2	3.4	1.2	3.4	1.2	3.4	V
		-	(2)	15	1.6	5	1.6	5	1.6	5	V

(1) Input on terminals 1, 5, 8, 12 or 2, 6, 9, 13; other inputs to V_{DD}.

(2) Input on terminals 1 and 2, 5 and 6, 8 and 9 or 12 and 13; other inputs to V_{DD}.

(3) See Figure 8-5 and Figure 8-6.

8 Detailed Description

8.1 Overview

The CD4093 is a quad two-input NAND gate. Each input has a Schmitt trigger circuit.

The gate switches at different points for positive-going and negative-going signals. The difference between the positive voltage (V_{T+}) and the negative voltage (V_{T-}) is defined as hysteresis voltage (V_H).

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS}(usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

8.2 Functional Block Diagram

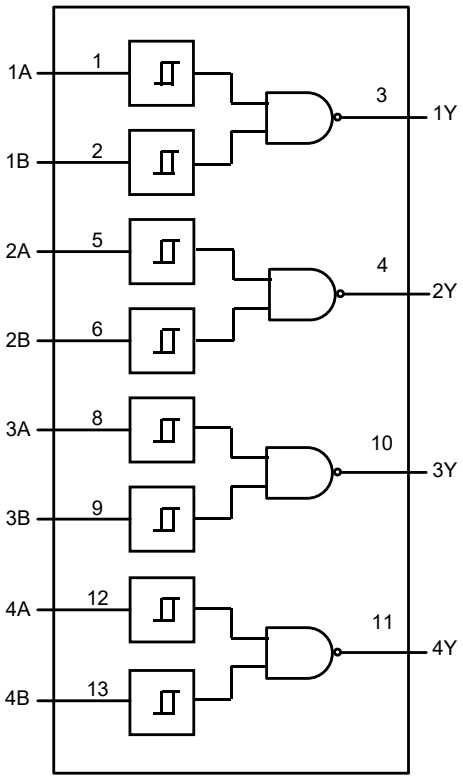


Figure 8-1 Functional diagram

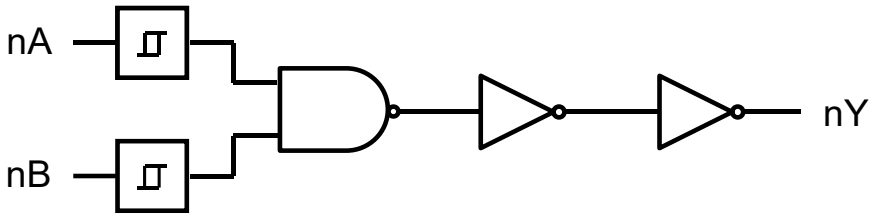


Figure 8-2 Logic diagram (one gate)

8.3 Function Table(1)

INPUT		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

(1) H=HIGH voltage level; L=LOW voltage level; X=don't care.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

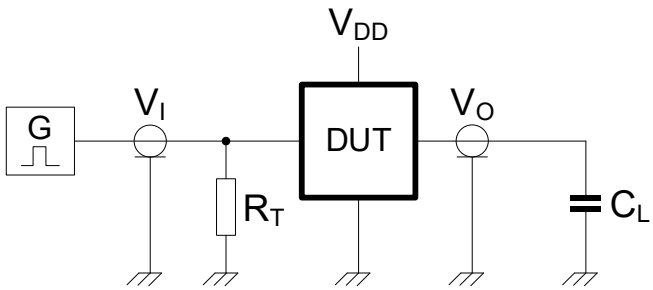


Figure 8-3 Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

8.4.2 AC Testing Waveforms

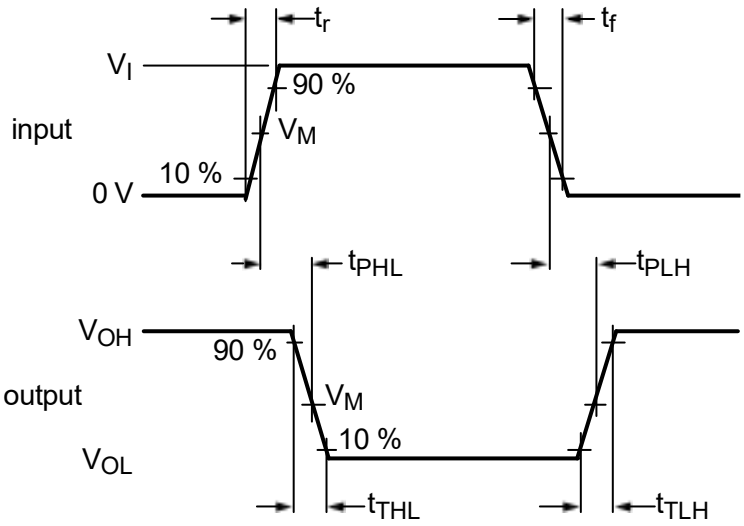


Figure 8-4 Propagation delay and output transition time

8.4.3 Transfer Characteristics Waveforms

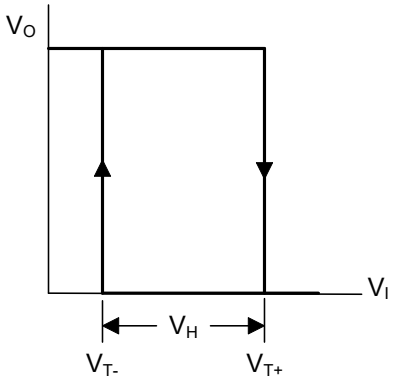


Figure 8-5 Transfer characteristic

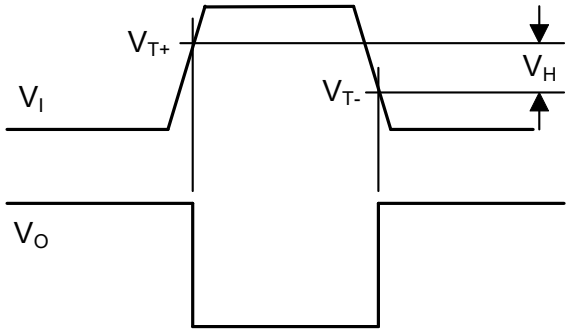
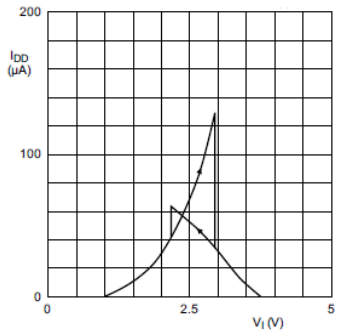
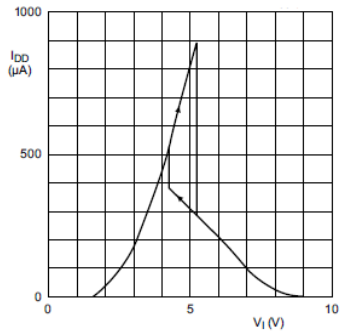


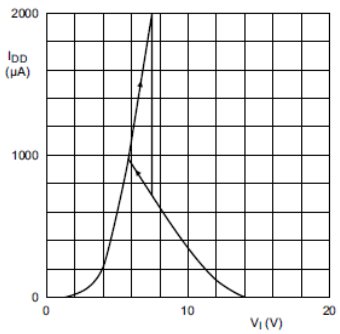
Figure 8-6 Waveforms showing definition of V_{T+} and V_{T-} (between limits at 30% and 70%) and V_H



a. V_{DD} = 5 V; T_{amb} = 25 °C



b. V_{DD} = 10 V; T_{amb} = 25 °C



c. V_{DD} = 15 V; T_{amb} = 25 °C

Figure 8-7 Typical drain current as a function of input

8.4.4 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{DD}	V_M	V_M
5V to 15V	0.5xV_{DD}	0.5xV_{DD}

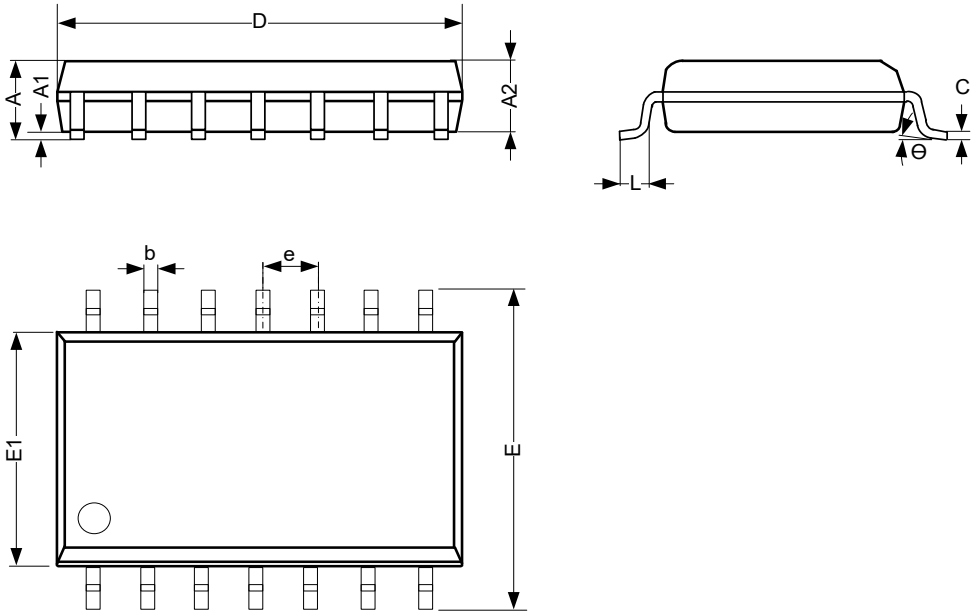
8.4.5 Test Data

SUPPLY VOLTAGE	INPUT		LOAD
V_{DD}	V_I	t_r , t_f	C_L
5V to 15V	V_{SS} or V_{DD}	≤ 20ns	50pF

9 Mechanical Information

9.1 SOP14 Mechanical Information

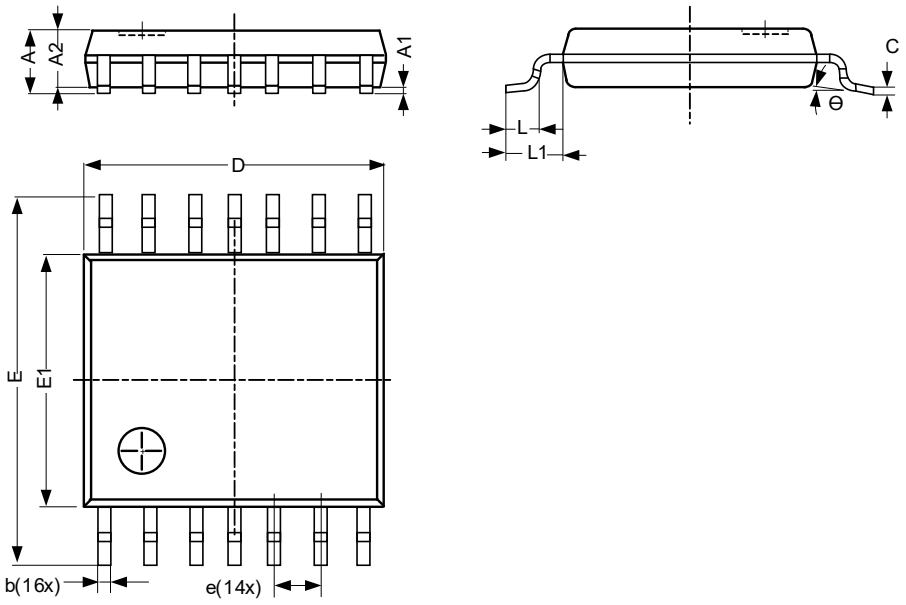
9.1.1 SOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.50	-	1.75
A1	0.05	-	0.25
A2	1.30	-	-
b	0.33	-	0.50
c	0.19	-	0.25
D	8.43	-	8.76
E	5.80	-	6.25
E1	3.75	-	4.00
e	1.27 BSC		
L	0.40	-	0.89
Θ	0°	-	8°
Unit: mm			

9.2 TSSOP14 Mechanical Information

9.2.1 TSSOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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