

8-bit Dual Supply Translating Transceiver: 3-state

CJ74LVC/LVCH8T245 Logic

1 Introduction

The CJ74LVC/LVCH8T245 are 8-bit dual supply translating transceivers with 3-state outputs that enable bidirectional level translation. They feature two data input-output ports (pins An and Bn), a direction control input (DIR), an output enable input (/OE) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 1.2V and 5.5V making the device suitable for translating between any of the low voltage nodes (1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5.0V). Pins An, /OE and DIR are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A HIGH on DIR allows transmission from An to Bn and a LOW on DIR allows transmission from Bn to An. The output enable input (/OE) can be used to disable the outputs so the buses are effectively isolated.

The devices are fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both A port and B port are in the high-impedance OFF-state.

Active bus hold circuitry in the CJ74LVCH8T245 holds unused or floating data inputs at a valid logic level.

2 Available Packages

PART NUMBER	PACKAGE
CJ74LVC8T245	TSSOP24
	QFN5.5x3.5-24L
CJ74LVCH8T245	TSSOP24
	QFN5.5x3.5-24L

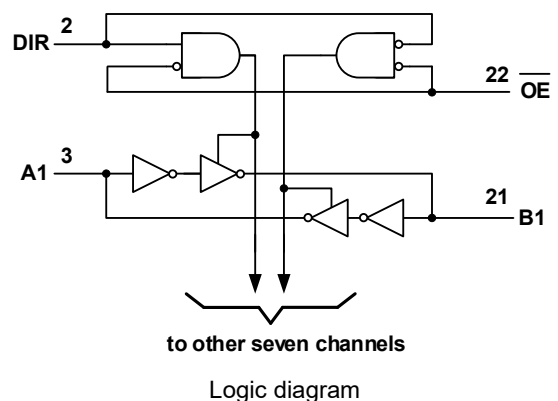
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range:
 - $V_{CC(A)}$: 1.2V to 5.5V
 - $V_{CC(B)}$: 1.2V to 5.5V
- Maximum data rates:
 - 420 Mbps (3.3V to 5.0V translation)
 - 210 Mbps (translate to 3.3V)
 - 140 Mbps (translate to 2.5V)
 - 75 Mbps (translate to 1.8V)
 - 60 Mbps (translate to 1.5V)
- Suspend mode
- $\pm 24mA$ output drive ($V_{CC}=3.0V$)
- Inputs accept voltages up to 5.5V
- Low power consumption: 30uA maximum I_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Specified from $-40^{\circ}C$ to $+125^{\circ}C$

4 Applications

- Personal electronic
- Industrial
- Enterprise
- Telecom



5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ74LVC8T245BHN	TSSOP24	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units/Reel	Active
CJ74LVCH8T245BHN	TSSOP24	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units/Reel	Active
CJ74LVC8T245QFN	QFN5.5x3.5-24L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units/Reel	Active
CJ74LVCH8T245QFN	QFN5.5x3.5-24L	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 3000 Units/Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

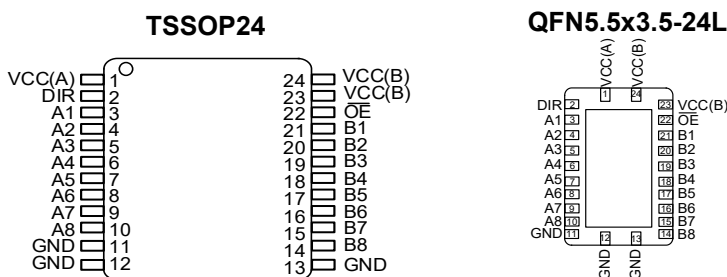


Figure 6-1 Pin configuration

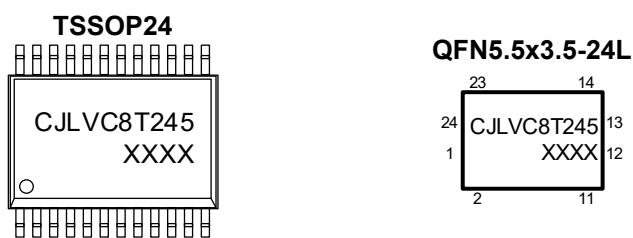
6.2 Pin Function

PIN		I/O ⁽¹⁾	DESCRIPTION
No.	NAME		
1	VCC(A)	P	Supply voltage A (An inputs/outputs, $\overline{\text{OE}}$ and DIR inputs are referenced to VCC(A))
2	DIR	-	Direction control
3,4,5,6,7,8,9,10	A1 to A8	I/O	Data input or output
11	GND ⁽¹⁾	G	Ground (0V)
12	GND ⁽¹⁾	G	Ground (0V)
13	GND ⁽¹⁾	G	Ground (0V)
21,20,19,18,17,16,15,14	B1 to B8	I/O	Data input or output
22	$\overline{\text{OE}}$	I	Output enable input (active LOW)
23	VCC(B)	P	Supply voltage B (Bn inputs/outputs are referenced to VCC(B))
24	VCC(B)	P	Supply voltage B (Bn inputs/outputs are referenced to VCC(B))

(1) All GND pins must be connected to ground (0V).

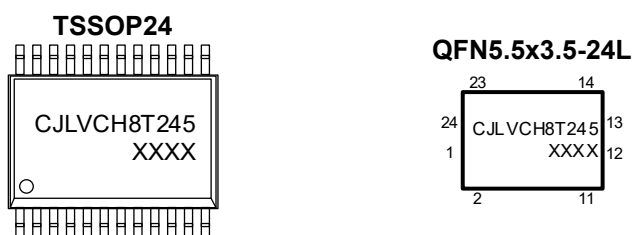
6.3 Marking Information

6.3.1 CJ74LVC8T245



XXXX: Code, indicates weekly record information.

6.3.2 CJ74LVCH8T245



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to GND(ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC(A)}$	Supply voltage A	-	-0.5	+6.5	V
$V_{CC(B)}$	Supply voltage B	-	-0.5	+6.5	V
I_{IK}	Input clamping current	$V_I < 0V$	-50	-	mA
V_I	Input voltage	-(1)	-0.5	+6.5	V
I_{OK}	Output clamping current	$V_O < 0V$	-50	-	mA
V_O	Output voltage	Active mode ⁽¹⁾ (2) (3)	-0.5	$V_{CCO}+0.5$	V
		Suspend or 3-state mode ⁽¹⁾	-0.5	+6.5	V
I_O	Output current	$V_O=0V$ to V_{CCO} ⁽²⁾	-	±50	mA
I_{CC}	Supply current	$I_{CC(A)}$ or $I_{CC(B)}$; per V_{CC} pin	-	100	mA
I_{GND}	Ground current	Per GND pin	-100	-	mA
T_{stg}	Storage temperature	-	-65	+150	°C
P_{tot}	Total power dissipation	-	-	500	mW
T_L	Soldering temperature	10s	-	260	°C

(1) The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

(2) V_{CCO} is the supply voltage associated with the output port.

(3) $V_{CCO}+0.5V$ should not exceed 6.5V.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC(A)}$	Supply voltage A	-	1.2	-	5.5	V
$V_{CC(B)}$	Supply voltage B	-	1.2	-	5.5	V
V_I	Input voltage	-	0	-	5.5	V
V_O	Output voltage	Active mode ⁽¹⁾	0	-	V_{CCO}	V
		Suspend or 3-state mode	0	-	5.5	V
T_{amb}	Ambient temperature	-	-40	-	+125	°C
$\Delta t/\Delta V$	Input transition rise and fall rate	$V_{CCI}=1.2V$ ⁽²⁾	-	-	20	ns/V
		$V_{CCI}=1.4V$ to $1.95V$	-	-	20	ns/V
		$V_{CCI}=2.3V$ to $2.7V$	-	-	20	ns/V
		$V_{CCI}=3.0V$ to $3.6V$	-	-	10	ns/V
		$V_{CCI}=4.5V$ to $5.5V$	-	-	5	ns/V

(1) V_{CCO} is the supply voltage associated with the output port.

(2) V_{CCI} is the supply voltage associated with the input port.

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{\text{ESD-HBM}}$	Electrostatic discharge	Human body model (HBM) ⁽¹⁾	±2000	V

(1) JEDEC document JEP155 states that 500-V H1BM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

$T_{\text{amb}}=25^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{OH}	HIGH-level output voltage	$V_{\text{I}}=V_{\text{IH}}$ or $V_{\text{IL}}^{(1)}$	$I_{\text{O}}=-3\text{mA}$; $V_{\text{CCO}}=1.2\text{V}$	-	1.09	-	V
V_{OL}	LOW-level output voltage	$V_{\text{I}}=V_{\text{IH}}$ or V_{IL}	$I_{\text{O}}=3\text{mA}$; $V_{\text{CCO}}=1.2\text{V}^{(1)}$	-	0.07	-	V
I_{I}	Input leakage current	DIR, OE input; $V_{\text{I}}=0\text{V}$ to 5.5V ; $V_{\text{CCI}}=1.2\text{V}$ to $5.5\text{V}^{(2)}$		-	-	±1	µA
I_{BHL}	Bus hold LOW current	A or B port; $V_{\text{I}}=0.42\text{V}$; $V_{\text{CCI}}=1.2\text{V}^{(2)}$		-	19	-	µA
I_{BHH}	Bus hold HIGH current	A or B port; $V_{\text{I}}=0.78\text{V}$; $V_{\text{CCI}}=1.2\text{V}^{(2)}$		-	-19	-	µA
I_{BHLO}	Bus hold LOW overdrive current	A or B port; $V_{\text{CCI}}=1.2\text{V}^{(2)(3)}$		-	19	-	µA
I_{BHHO}	Bus hold HIGH overdrive current	A or B port; $V_{\text{CCI}}=1.2\text{V}^{(2)(3)}$		-	-19	-	µA
I_{OZ}	OFF-state output current	A or B port; $V_{\text{O}}=0\text{V}$ or V_{CCO} ; $V_{\text{CCO}}=1.2\text{V}$ to $5.5\text{V}^{(1)}$		-	-	±1	µA
		Suspend mode A port; $V_{\text{O}}=0\text{V}$ or V_{CCO} ; $V_{\text{CC(A)}}=5.5\text{V}$; $V_{\text{CC(B)}}=0\text{V}^{(1)}$		-	-	±1	µA
		Suspend mode B port; $V_{\text{O}}=0\text{V}$ or V_{CCO} ; $V_{\text{CC(A)}}=0\text{V}$; $V_{\text{CC(B)}}=5.5\text{V}^{(1)}$		-	-	±1	µA
I_{OFF}	Power-off leakage current	A port; V_{I} or $V_{\text{O}}=0\text{V}$ to 5.5V ; $V_{\text{CC(A)}}=0\text{V}$; $V_{\text{CC(B)}}=1.2\text{V}$ to 5.5V		-	-	±1	µA
		B port; V_{I} or $V_{\text{O}}=0\text{V}$ to 5.5V ; $V_{\text{CC(B)}}=0\text{V}$; $V_{\text{CC(A)}}=1.2\text{V}$ to 5.5V		-	-	±1	µA
C_{I}	Input capacitance	DIR, OE input; $V_{\text{I}}=0\text{V}$ or 3.3V ; $V_{\text{CC(A)}}=3.3\text{V}$		-	3	-	pF
$C_{\text{I/O}}$	Input/output capacitance	A and B port; $V_{\text{O}}=3.3\text{V}$ or 0V ; $V_{\text{CC(A)}}=V_{\text{CC(B)}}=3.3\text{V}$		-	6.5	-	pF

(1) V_{CCO} is the supply voltage associated with the output port.

(2) V_{CCI} is the supply voltage associated with the data input port.

(3) To guarantee the node switches, an external driver must source/sink at least $I_{\text{BHLO}}/I_{\text{BHHO}}$ when the input is in the range V_{IL} to V_{IH} .

7.4.2 DC Characteristics 2

T_{amb}=−40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V _{IH}	HIGH-level input voltage	Data input ⁽¹⁾	V _{CCI} =1.2V	0.8V _{CCI}	-	-	V
			V _{CCI} =1.4V to 1.95V	0.65V _{CCI}	-	-	V
			V _{CCI} =2.3V to 2.7V	1.7	-	-	V
			V _{CCI} =3.0V to 3.6V	2.0	-	-	V
			V _{CCI} =4.5V to 5.5V	0.7V _{CCI}	-	-	V
		DIR, $\overline{\text{OE}}$ input	V _{CCI} =1.2V	0.8V _{CC(A)}	-	-	V
			V _{CCI} =1.4V to 1.95V	0.65V _{CC(A)}	-	-	V
			V _{CCI} =2.3V to 2.7V	1.7	-	-	V
			V _{CCI} =3.0V to 3.6V	2.0	-	-	V
			V _{CCI} =4.5V to 5.5V	0.7V _{CC(A)}	-	-	V
V _{IL}	LOW-level input voltage	Data input ⁽¹⁾	V _{CCI} =1.2V	-	-	0.2V _{CCI}	V
			V _{CCI} =1.4V to 1.95V	-	-	0.35V _{CCI}	V
			V _{CCI} =2.3V to 2.7V	-	-	0.7	V
			V _{CCI} =3.0V to 3.6V	-	-	0.8	V
			V _{CCI} =4.5V to 5.5V	-	-	0.3V _{CCI}	V
		DIR, $\overline{\text{OE}}$ input	V _{CCI} =1.2V	-	-	0.2V _{CC(A)}	V
			V _{CCI} =1.4V to 1.95V	-	-	0.35V _{CC(A)}	V
			V _{CCI} =2.3V to 2.7V	-	-	0.7	V
			V _{CCI} =3.0V to 3.6V	-	-	0.8	V
			V _{CCI} =4.5V to 5.5V	-	-	0.3V _{CC(A)}	V
V _{OH}	HIGH-level output voltage	V _I =V _{IH}	I _O =−100μA; V _{CCO} =1.2V to 4.5V ⁽²⁾	V _{CCO} −0.1	-	-	V
			I _O =−6mA; V _{CCO} =1.4V	1.0	-	-	V
			I _O =−8mA; V _{CCO} =1.65V	1.2	-	-	V
			I _O =−12mA; V _{CCO} =2.3V	1.9	-	-	V
			I _O =−24mA; V _{CCO} =3.0V	2.4	-	-	V
			I _O =−32mA; V _{CCO} =4.5V	3.8	-	-	V
V _{OL}	LOW-level output voltage	V _I =V _{IL} ⁽²⁾	I _O =100μA; V _{CCO} =1.2V to 4.5V	-	-	0.1	V
			I _O =6mA; V _{CCO} =1.4V	-	-	0.3	V
			I _O =8mA; V _{CCO} =1.65V	-	-	0.45	V
			I _O =12mA; V _{CCO} =2.3V	-	-	0.3	V
			I _O =24mA; V _{CCO} =3.0V	-	-	0.55	V
			I _O =32mA; V _{CCO} =4.5V	-	-	0.55	V
I _I	Input leakage current	DIR, $\overline{\text{OE}}$ input; V _I =0V to 5.5V; V _{CCI} =1.2V to 5.5V		-	-	±2	μA

I_{BHL}	Bus hold LOW current	A or B port ⁽¹⁾	$V_I=0.49V$; $V_{CCI}=1.4V$	15	-	-	μA
			$V_I=0.58V$; $V_{CCI}=1.65V$	25	-	-	μA
			$V_I=0.70V$; $V_{CCI}=2.3V$	45	-	-	μA
			$V_I=0.80V$; $V_{CCI}=3.0V$	100	-	-	μA
			$V_I=1.35V$; $V_{CCI}=4.5V$	100	-	-	μA
I_{BHH}	Bus hold HIGH current	A or B port ⁽¹⁾	$V_I=0.91V$; $V_{CCI}=1.4V$	-15	-	-	μA
			$V_I=1.07V$; $V_{CCI}=1.65V$	-25	-	-	μA
			$V_I=1.70V$; $V_{CCI}=2.3V$	-45	-	-	μA
			$V_I=2.00V$; $V_{CCI}=3.0V$	-100	-	-	μA
			$V_I=3.15V$; $V_{CCI}=4.5V$	-100	-	-	μA
I_{BHLO}	Bus hold LOW overdrive current	A or B port ⁽¹⁾⁽³⁾	$V_{CCI}=1.6V$	125	-	-	μA
			$V_{CCI}=1.95V$	200	-	-	μA
			$V_{CCI}=2.7V$	300	-	-	μA
			$V_{CCI}=3.6V$	500	-	-	μA
			$V_{CCI}=5.5V$	900	-	-	μA
I_{BHHO}	Bus hold HIGH overdrive current	A or B port ⁽¹⁾⁽³⁾	$V_{CCI}=1.6V$	-125	-	-	μA
			$V_{CCI}=1.95V$	-200	-	-	μA
			$V_{CCI}=2.7V$	-300	-	-	μA
			$V_{CCI}=3.6V$	-500	-	-	μA
			$V_{CCI}=5.5V$	-900	-	-	μA
I_{OZ}	OFF-state output current	A or B port; $V_O=0V$ or V_{CCO} ; $V_{CCO}=1.2V$ to $5.5V^{(2)}$		-	-	± 2	μA
		Suspend mode A port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=5.5V$; $V_{CC(B)}=0V^{(2)}$		-	-	± 2	μA
		Suspend mode B port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=0V$; $V_{CC(B)}=5.5V^{(2)}$		-	-	± 2	μA
I_{OFF}	Power-off leakage current	A port; V_I or $V_O=0V$ to $5.5V$; $V_{CC(A)}=0V$; $V_{CC(B)}=1.2V$ to $5.5V$		-	-	± 2	μA
		B port; V_I or $V_O=0V$ to $5.5V$; $V_{CC(B)}=0V$; $V_{CC(A)}=1.2V$ to $5.5V$		-	-	± 2	μA
I_{CC}	Supply current	A port; $V_I=0V$ or V_{CCI} ; $I_O=0A^{(1)}$	$V_{CC(A)}, V_{CC(B)}=1.2V$ to $5.5V$	-	-	15	μA
			$V_{CC(A)}=5.5V$; $V_{CC(B)}=0V$	-	-	15	μA
			$V_{CC(A)}=0V$; $V_{CC(B)}=5.5V$	-2	-	-	μA
		B port; $V_I=0V$ or V_{CCI} ; $I_O=0A$	$V_{CC(A)}, V_{CC(B)}=1.2V$ to $5.5V$	-	-	15	μA
			$V_{CC(B)}=0V$; $V_{CC(A)}=5.5V$	-2	-	-	μA
			$V_{CC(B)}=5.5V$; $V_{CC(A)}=0V$	-	-	15	μA
		A plus B port ($I_{CC(A)}+I_{CC(B)}$);	$V_{CC(A)}, V_{CC(B)}=1.2V$ to $5.5V$	-	-	25	μA

		$I_O=0A$; $V_I=0V$ or V_{CCI}					
ΔI_{CC}	Additional supply current	Per input; $V_{CC(A)}, V_{CC(B)}=3.0V$ to 5.5V	DIR and OE input; DIR or OE input at $V_{CC(A)}-0.6V$; A port at $V_{CC(A)}$ or GND; B port=open	-	-	50	μA
			A port; A port at $V_{CC(A)}-0.6V$; DIR at $V_{CC(A)}$; B port=open ⁽⁴⁾	-	-	50	μA
			B port; B port at $V_{CC(B)}-0.6V$; DIR at GND; A port=open ⁽⁴⁾	-	-	50	μA

(1) V_{CCI} is the supply voltage associated with the data input port.

(2) V_{CCO} is the supply voltage associated with the output port

(3) To guarantee the node switches, an external driver must source/sink at least I_{BHL}/I_{BHO} when the input is in the range V_{IL} to V_{IH} .

(4) For non bus hold parts only (CJ74LVC8T245).

7.4.3 DC Characteristics 3

$T_{amb}=-40^{\circ}C$ to $+125^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	Data input ⁽¹⁾	$V_{CCI}=1.2V$	$0.8V_{CCI}$	-	-	V
			$V_{CCI}=1.4V$ to $1.95V$	$0.65V_{CCI}$	-	-	V
			$V_{CCI}=2.3V$ to $2.7V$	1.7	-	-	V
			$V_{CCI}=3.0V$ to $3.6V$	2.0	-	-	V
			$V_{CCI}=4.5V$ to $5.5V$	$0.7V_{CCI}$	-	-	V
		DIR, OE input	$V_{CCI}=1.2V$	$0.8V_{CC(A)}$	-	-	V
			$V_{CCI}=1.4V$ to $1.95V$	$0.65V_{CC(A)}$	-	-	V
			$V_{CCI}=2.3V$ to $2.7V$	1.7	-	-	V
			$V_{CCI}=3.0V$ to $3.6V$	2.0	-	-	V
			$V_{CCI}=4.5V$ to $5.5V$	$0.7V_{CC(A)}$	-	-	V
V_{IL}	LOW-level input voltage	Data input ⁽¹⁾	$V_{CCI}=1.2V$	-	-	$0.2V_{CCI}$	V
			$V_{CCI}=1.4V$ to $1.95V$	-	-	$0.35V_{CCI}$	V
			$V_{CCI}=2.3V$ to $2.7V$	-	-	0.7	V
			$V_{CCI}=3.0V$ to $3.6V$	-	-	0.8	V
			$V_{CCI}=4.5V$ to $5.5V$	-	-	$0.3V_{CCI}$	V
		DIR, OE input	$V_{CCI}=1.2V$	-	-	$0.2V_{CC(A)}$	V
			$V_{CCI}=1.4V$ to $1.95V$	-	-	$0.35V_{CC(A)}$	V
			$V_{CCI}=2.3V$ to $2.7V$	-	-	0.7	V
			$V_{CCI}=3.0V$ to $3.6V$	-	-	0.8	V
			$V_{CCI}=4.5V$ to $5.5V$	-	-	$0.3V_{CC(A)}$	V
V_{OH}	HIGH-level output	$V_I=V_{IH}$	$I_O=-100\mu A$;	$V_{CCO}-0.1$	-	-	V

	voltage		$V_{CCO}=1.2V$ to $4.5V^{(2)}$				
			$I_O=-6mA$; $V_{CCO}=1.4V$	1.0	-	-	V
			$I_O=-8mA$; $V_{CCO}=1.65V$	1.2	-	-	V
			$I_O=-12mA$; $V_{CCO}=2.3V$	1.9	-	-	V
			$I_O=-24mA$; $V_{CCO}=3.0V$	2.4	-	-	V
			$I_O=-32mA$; $V_{CCO}=4.5V$	3.8	-	-	V
V_{OL}	LOW-level output voltage	$V_I=V_{IL}^{(2)}$	$I_O=100\mu A$; $V_{CCO}=1.2V$ to $4.5V$	-	-	0.1	V
			$I_O=6mA$; $V_{CCO}=1.4V$	-	-	0.3	V
			$I_O=8mA$; $V_{CCO}=1.65V$	-	-	0.45	V
			$I_O=12mA$; $V_{CCO}=2.3V$	-	-	0.3	V
			$I_O=24mA$; $V_{CCO}=3.0V$	-	-	0.55	V
			$I_O=32mA$; $V_{CCO}=4.5V$	-	-	0.55	V
I_I	Input leakage current	DIR, OE input; $V_I=0V$ or $5.5V$; $V_{CCI}=1.2V$ to $5.5V$		-	-	± 10	μA
I_{BHL}	Bus hold LOW current	A or B port ⁽¹⁾	$V_I=0.49V$; $V_{CCI}=1.4V$	10	-	-	μA
			$V_I=0.58V$; $V_{CCI}=1.65V$	20	-	-	μA
			$V_I=0.70V$; $V_{CCI}=2.3V$	45	-	-	μA
			$V_I=0.80V$; $V_{CCI}=3.0V$	80	-	-	μA
			$V_I=1.35V$; $V_{CCI}=4.5V$	100	-	-	μA
I_{BHH}	Bus hold HIGH current	A or B port ⁽¹⁾	$V_I=0.91V$; $V_{CCI}=1.4V$	-10	-	-	μA
			$V_I=1.07V$; $V_{CCI}=1.65V$	-20	-	-	μA
			$V_I=1.70V$; $V_{CCI}=2.3V$	-45	-	-	μA
			$V_I=2.00V$; $V_{CCI}=3.0V$	-80	-	-	μA
			$V_I=3.15V$; $V_{CCI}=4.5V$	-100	-	-	μA
I_{BHLO}	Bus hold LOW overdrive current	A or B port ⁽¹⁾⁽³⁾	$V_{CCI}=1.6V$	125	-	-	μA
			$V_{CCI}=1.95V$	200	-	-	μA
			$V_{CCI}=2.7V$	300	-	-	μA
			$V_{CCI}=3.6V$	500	-	-	μA
			$V_{CCI}=5.5V$	900	-	-	μA
I_{BHHO}	Bus hold HIGH overdrive current	A or B port ⁽¹⁾⁽³⁾	$V_{CCI}=1.6V$	-125	-	-	μA
			$V_{CCI}=1.95V$	-200	-	-	μA
			$V_{CCI}=2.7V$	-300	-	-	μA
			$V_{CCI}=3.6V$	-500	-	-	μA
			$V_{CCI}=5.5V$	-900	-	-	μA
I_{OZ}	OFF-state output current	A or B port; $V_O=0V$ or V_{CCO} ; $V_{CCO}=1.2V$ to $5.5V^{(2)}$		-	-	± 10	μA
		Suspend mode A port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=5.5V$;		-	-	± 10	μA

		$V_{CC(B)}=0V^{(2)}$					
		Suspend mode B port; $V_O=0V$ or V_{CCO} ; $V_{CC(A)}=0V$; $V_{CC(B)}=5.5V^{(2)}$		-	-	± 10	μA
I_{OFF}	Power-off leakage current	A port; V_I or $V_O=0V$ to $5.5V$; $V_{CC(A)}=0V$; $V_{CC(B)}=1.2V$ to $5.5V$		-	-	± 10	μA
		B port; V_I or $V_O=0V$ to $5.5V$; $V_{CC(B)}=0V$; $V_{CC(A)}=1.2V$ to $5.5V$		-	-	± 10	μA
I_{CC}	Supply current	A port; $V_I=0V$ or V_{CCI} ; $I_O=0A^{(1)}$	$V_{CC(A)}, V_{CC(B)}=1.2V$ to $5.5V$	-	-	20	μA
			$V_{CC(A)}=5.5V$; $V_{CC(B)}=0V$	-	-	20	μA
			$V_{CC(A)}=0V$; $V_{CC(B)}=5.5V$	-4	-	-	μA
		B port; $V_I=0V$ or V_{CCI} ; $I_O=0A$	$V_{CC(A)}, V_{CC(B)}=1.2V$ to $5.5V$	-	-	20	μA
			$V_{CC(B)}=0V$; $V_{CC(A)}=5.5V$	-4	-	-	μA
			$V_{CC(B)}=5.5V$; $V_{CC(A)}=0V$	-	-	20	μA
		A plus B port ($I_{CC(A)}+I_{CC(B)}$); $I_O=0A$; $V_I=0V$ or V_{CCI}	$V_{CC(A)}, V_{CC(B)}=1.2V$ to $5.5V$	-	-	30	μA
ΔI_{CC}	Additional supply current	Per input; $V_{CC(A)}, V_{CC(B)}=3.0V$ to $5.5V$	DIR and $\overline{OE}$ input; DIR or $\overline{OE}$ input at $V_{CC(A)}-0.6V$; A port at $V_{CC(A)}$ or GND; B port=open	-	-	75	μA
			A port; A port at $V_{CC(A)}-0.6V$; DIR at $V_{CC(A)}$; B port=open ⁽⁴⁾	-	-	75	μA
			B port; B port at $V_{CC(B)}-0.6V$; DIR at GND; A port=open ⁽⁴⁾	-	-	75	μA

(1) V_{CCI} is the supply voltage associated with the data input port.

(2) V_{CCO} is the supply voltage associated with the output port

(3) To guarantee the node switches, an external driver must source/sink at least I_{BHL0}/I_{BH0} when the input is in the range V_{IL} to V_{IH} .

(4) For non bus hold parts only (CJ74LVC8T245).

7.4.4 AC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	V _{CC(B)}										UNIT
			1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{CC(A)} =1.5V±0.1V													
t _{PLH} , t _{PHL}	Propagation delay	An to Bn	-	17.6	-	15.3	-	13.1	-	12.5	-	12.5	ns
		Bn to An	-	17.5	-	16.3	-	15.2	-	14.4	-	13.8	ns
t _{PLZ} , t _{PHZ}	Disable time	$\overline{\text{OE}}$ to An	-	29.1	-	29.1	-	29.1	-	29.1	-	29.1	ns
		$\overline{\text{OE}}$ to Bn	-	36.4	-	34.5	-	17.3	-	15.5	-	13.6	ns
t _{PZL} , t _{PZH}	Enable time	$\overline{\text{OE}}$ to An	-	33.6	-	33.6	-	33.6	-	33.6	-	33.6	ns
		$\overline{\text{OE}}$ to Bn	-	37.3	-	35.5	-	18.2	-	15.5	-	14.5	ns
V _{CC(A)} =1.8V±0.15V													
t _{PLH} , t _{PHL}	Propagation delay	An to Bn	-	16.4	-	13.1	-	11.1	-	10.1	-	10.0	ns
		Bn to An	-	15.2	-	12.7	-	11.4	-	10.6	-	10.1	ns
t _{PLZ} , t _{PHZ}	Disable time	$\overline{\text{OE}}$ to An	-	29.1	-	28.9	-	28.7	-	28.5	-	28.4	ns
		$\overline{\text{OE}}$ to Bn	-	36.4	-	32.9	-	15.5	-	14.5	-	13.0	ns
t _{PZL} , t _{PZH}	Enable time	$\overline{\text{OE}}$ to An	-	24.5	-	24.5	-	24.4	-	24.3	-	24.3	ns
		$\overline{\text{OE}}$ to Bn	-	35.5	-	34.5	-	18.2	-	14.2	-	13.5	ns
V _{CC(A)} =2.5V±0.2V													
t _{PLH} , t _{PHL}	Propagation delay	An to Bn	-	15.3	-	11.9	-	9.2	-	8.2	-	7.6	ns
		Bn to An	-	13.0	-	10.6	-	8.9	-	7.9	-	7.1	ns
t _{PLZ} , t _{PHZ}	Disable time	$\overline{\text{OE}}$ to An	-	10.9	-	10.9	-	10.9	-	10.9	-	10.9	ns
		$\overline{\text{OE}}$ to Bn	-	33.6	-	30.5	-	13.6	-	13.0	-	9.9	ns
t _{PZL} , t _{PZH}	Enable time	$\overline{\text{OE}}$ to An	-	15.5	-	15.5	-	15.5	-	15.5	-	15.5	ns
		$\overline{\text{OE}}$ to Bn	-	33.6	-	29.5	-	15.9	-	12.3	-	10.0	ns
V _{CC(A)} =3.3V±0.3V													
t _{PLH} , t _{PHL}	Propagation delay	An to Bn	-	14.6	-	11.2	-	8.1	-	7.0	-	6.5	ns
		Bn to An	-	12.3	-	9.8	-	7.9	-	6.8	-	6.0	ns
t _{PLZ} , t _{PHZ}	Disable time	$\overline{\text{OE}}$ to An	-	10.9	-	10.9	-	10.9	-	10.9	-	10.9	ns
		$\overline{\text{OE}}$ to Bn	-	30.9	-	28.2	-	13.2	-	11.4	-	9.5	ns
t _{PZL} , t _{PZH}	Enable time	$\overline{\text{OE}}$ to An	-	12.3	-	12.3	-	12.1	-	12.0	-	12.0	ns
		$\overline{\text{OE}}$ to Bn	-	33.5	-	28.5	-	16.5	-	11.3	-	9.5	ns
V _{CC(A)} =5.0V±0.5V													
t _{PLH} , t _{PHL}	Propagation delay	An to Bn	-	14.1	-	10.6	-	7.3	-	6.3	-	5.6	ns
		Bn to An	-	12.3	-	9.5	-	7.4	-	6.3	-	5.5	ns
t _{PLZ} , t _{PHZ}	Disable time	$\overline{\text{OE}}$ to An	-	8.4	-	8.4	-	8.4	-	8.4	-	8.4	ns
		$\overline{\text{OE}}$ to Bn	-	32.5	-	29.5	-	12.3	-	10.9	-	8.9	ns

t_{PZL}, t_{PZH}	Enable time	$\overline{OE}$ to An	-	9.7	-	9.7	-	9.7	-	9.7	-	9.7	ns
		$\overline{OE}$ to Bn	-	33.5	-	28.5	-	16.7	-	12.3	-	9.7	ns

7.4.5 AC Characteristics 2

$T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	V _{CC(B)}										UNIT
			1.5V±0.1V		1.8V±0.15V		2.5V±0.2V		3.3V±0.3V		5.0V±0.5V		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{CC(A)} =1.5V±0.1V													
t _{PLH} , t _{PHL}	Propagation delay	An to Bn	-	19.4	-	16.8	-	14.4	-	13.8	-	13.8	ns
		Bn to An	-	19.2	-	17.9	-	16.7	-	15.8	-	15.2	ns
t _{PLZ} , t _{PHZ}	Disable time	$\overline{OE}$ to An	-	32	-	32	-	32	-	32	-	32	ns
		$\overline{OE}$ to Bn	-	40	-	38	-	19	-	17	-	15	ns
t _{PZL} , t _{PZH}	Enable time	$\overline{OE}$ to An	-	37	-	37	-	37	-	37	-	37	ns
		$\overline{OE}$ to Bn	-	41	-	39	-	20	-	17	-	16	ns
V _{CC(A)} =1.8V±0.15V													
t _{PLH} , t _{PHL}	Propagation delay	An to Bn	-	18	-	14.4	-	12.2	-	11.1	-	11	ns
		Bn to An	-	16.7	-	14	-	12.5	-	11.7	-	11.1	ns
t _{PLZ} , t _{PHZ}	Disable time	$\overline{OE}$ to An	-	32	-	31.8	-	31.6	-	31.3	-	31.2	ns
		$\overline{OE}$ to Bn	-	40	-	36.2	-	17.1	-	16.0	-	14.3	ns
t _{PZL} , t _{PZH}	Enable time	$\overline{OE}$ to An	-	27	-	27	-	26.8	-	26.7	-	26.7	ns
		$\overline{OE}$ to Bn	-	39	-	38	-	20	-	15.6	-	14.8	ns
V _{CC(A)} =2.5V±0.2V													
t _{PLH} , t _{PHL}	Propagation delay	An to Bn	-	16.8	-	13.1	-	10.1	-	9	-	8.4	ns
		Bn to An	-	14.3	-	11.7	-	9.8	-	8.7	-	7.8	ns
t _{PLZ} , t _{PHZ}	Disable time	$\overline{OE}$ to An	-	12	-	12	-	12	-	12	-	12	ns
		$\overline{OE}$ to Bn	-	37	-	33.6	-	15	-	14.3	-	10.9	ns
t _{PZL} , t _{PZH}	Enable time	$\overline{OE}$ to An	-	17	-	17	-	17	-	17	-	17	ns
		$\overline{OE}$ to Bn	-	37	-	32.5	-	17.5	-	13.5	-	11	ns
V _{CC(A)} =3.3V±0.3V													
t _{PLH} , t _{PHL}	Propagation delay	An to Bn	-	16.1	-	12.3	-	8.9	-	7.7	-	7.2	ns
		Bn to An	-	13.5	-	10.8	-	8.7	-	7.5	-	6.6	ns
t _{PLZ} , t _{PHZ}	Disable time	$\overline{OE}$ to An	-	12	-	12	-	12	-	12	-	12	ns
		$\overline{OE}$ to Bn	-	34	-	31	-	14.5	-	12.5	-	10.4	ns
t _{PZL} , t _{PZH}	Enable time	$\overline{OE}$ to An	-	13.5	-	13.5	-	13.3	-	13.2	-	13.2	ns
		$\overline{OE}$ to Bn	-	36.8	-	31.4	-	18.1	-	12.4	-	10.5	ns
V _{CC(A)} =5.0V±0.5V													
	Propagation	An to Bn	-	15.5	-	11.7	-	8	-	6.9	-	6.2	ns

t_{PLH}, t_{PHL}	delay	Bn to An	-	13.5	-	10.5	-	8.1	-	6.9	-	6	ns
t_{PLZ}, t_{PHZ}	Disable time	$\overline{OE}$ to An	-	9.2	-	9.2	-	9.2	-	9.2	-	9.2	ns
		$\overline{OE}$ to Bn	-	35.8	-	32.5	-	13.5	-	12	-	9.8	ns
t_{PZL}, t_{PZH}	Enable time	$\overline{OE}$ to An	-	10.7	-	10.7	-	10.7	-	10.7	-	10.7	ns
		$\overline{OE}$ to Bn	-	36.8	-	31.4	-	18.4	-	13.5	-	10.7	ns

8 Detailed Description

8.1 Overview

The CJ74LVC/LVCH8T245 are 8-bit dual supply translating transceivers with 3-state outputs that enable bidirectional level translation. They feature two data input-output ports (pins An and Bn), a direction control input (DIR), an output enable input ($\overline{\text{OE}}$) and dual supply pins ($V_{\text{CC(A)}}$ and $V_{\text{CC(B)}}$). Both $V_{\text{CC(A)}}$ and $V_{\text{CC(B)}}$ can be supplied at any voltage between 1.2V and 5.5V making the device suitable for translating between any of the low voltage nodes (1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5.0V). Pins An, $\overline{\text{OE}}$ and DIR are referenced to $V_{\text{CC(A)}}$ and pins Bn are referenced to $V_{\text{CC(B)}}$. A HIGH on DIR allows transmission from An to Bn and a LOW on DIR allows transmission from Bn to An. The output enable input ($\overline{\text{OE}}$) can be used to disable the outputs so the buses are effectively isolated.

The devices are fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{\text{CC(A)}}$ or $V_{\text{CC(B)}}$ are at GND level, both A port and B port are in the high-impedance OFF-state.

Active bus hold circuitry in the CJ74LVCH8T245 holds unused or floating data inputs at a valid logic level.

8.2 Functional Block Diagram

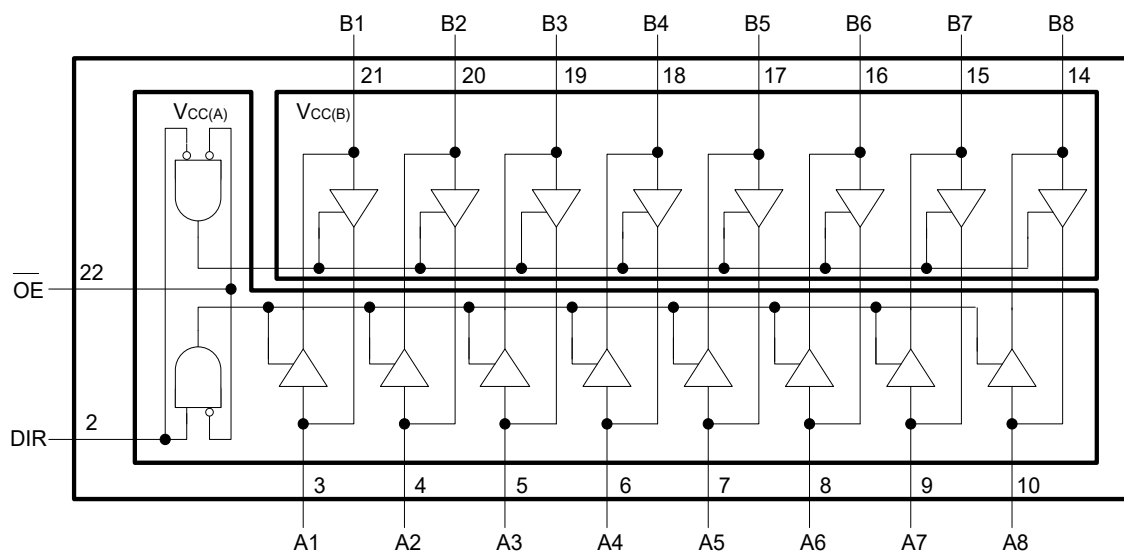


Figure 8-1 Logic symbol

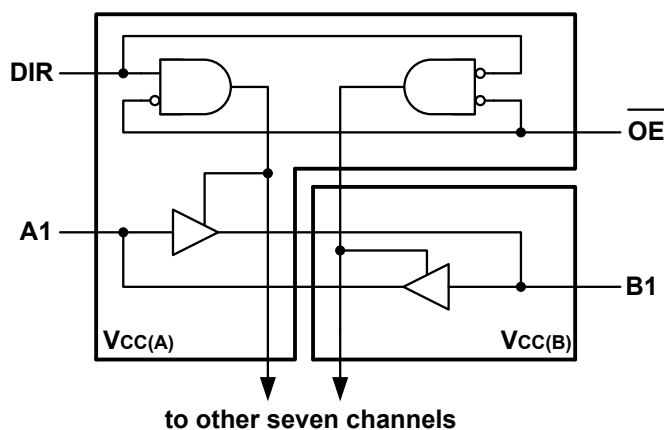


Figure 8-2 Logic diagram (one channel)

8.3 Function Table

SUPPLY VOLTAGE	INPUT		INPUT/OUTPUT	
$V_{CC(A)}, V_{CC(B)}$	$\overline{OE}$	DIR	An	Bn
1.2V to 5.5V	L	L	An=Bn	input
1.2V to 5.5V	L	H	input	Bn=An
1.2V to 5.5V	H	X	Z	Z
GND	X	X	Z	Z

Note:

- (1) H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.
- (2) The An inputs/outputs, DIR and $\overline{OE}$ input circuit is referenced to $V_{CC(A)}$; The Bn inputs/outputs circuit is referenced to $V_{CC(B)}$.
- (3) If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

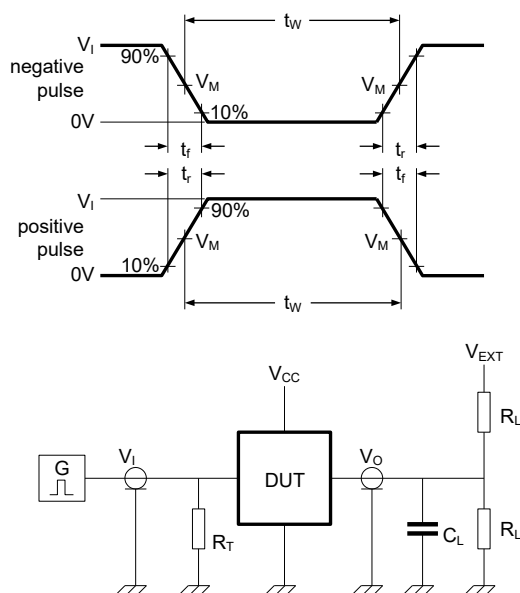


Figure 8-3 Load circuitry for switching times

Definitions for test circuit:

R_L =Load resistance.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance.

V_{EXT} =External voltage for measuring switching times.

8.4.2 AC Testing Waveforms

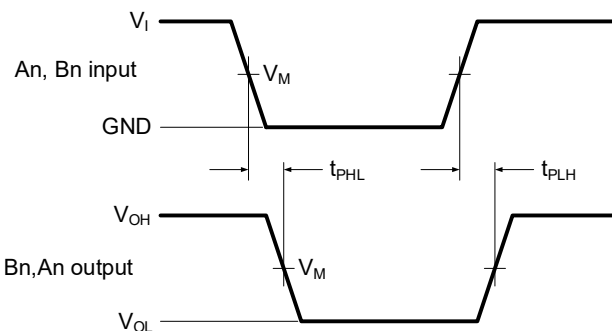


Figure 8-4 The data input (An, Bn) to output (Bn, An) propagation delay times
(V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.)

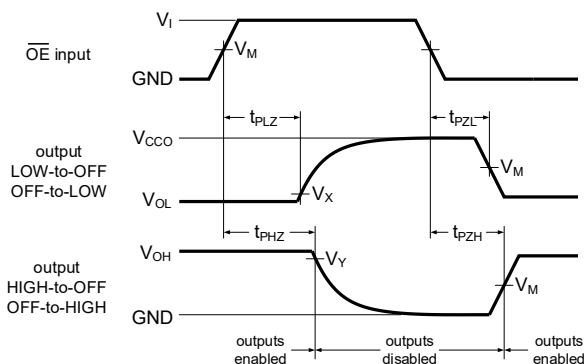


Figure 8-5 Enable and disable times
(V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.)

8.4.3 Measurement Points

SUPPLY VOLTAGE	INPUT ⁽¹⁾	OUTPUT ⁽²⁾		
$V_{CC(A)}, V_{CC(B)}$	V_M	V_M	V_X	V_Y
1.2V to 1.6V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.1V$	$V_{OH}-0.1V$
1.65V to 2.7V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.15V$	$V_{OH}-0.15V$
3.0V to 5.5V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL}+0.3V$	$V_{OH}-0.3V$

(1) V_{CCI} is the supply voltage associated with the data input port.

(2) V_{CCO} is the supply voltage associated with the output port.

8.4.4 Test Data

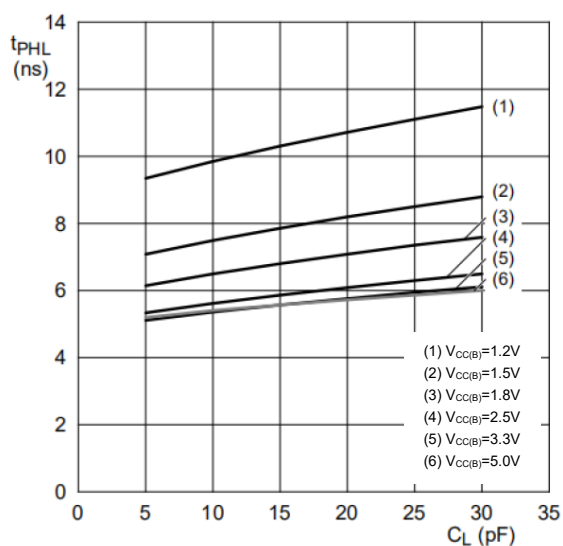
SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}		
$V_{CC(A)}, V_{CC(B)}$	$V_I^{(1)}$	$\Delta t/\Delta V^{(2)}$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	$t_{PZL}, t_{PLZ}^{(3)}$
1.2V to 5.5V	V_{CCI}	$\leq 1.0ns/V$	15pF	2k Ω	Open	GND	$2V_{CCO}$

(1) V_{CCI} is the supply voltage associated with the data input port.

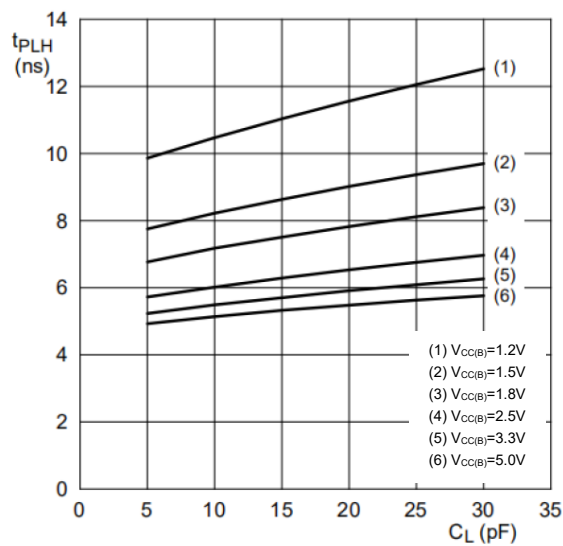
(2) $dV/dt \geq 1.0V/ns$.

(3) V_{CCO} is the supply voltage associated with the output port.

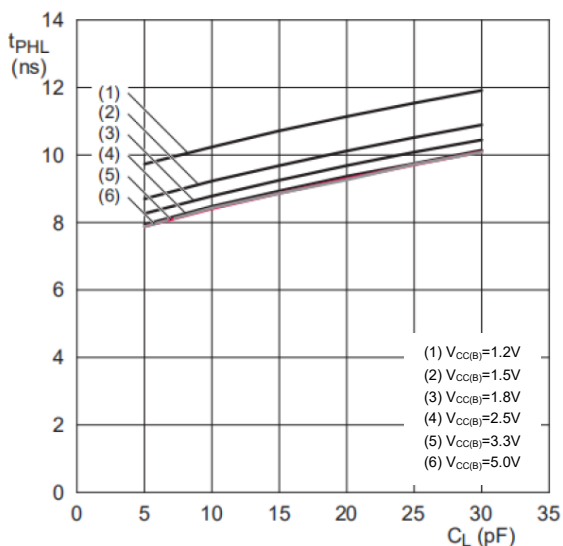
9 Characteristic Curve



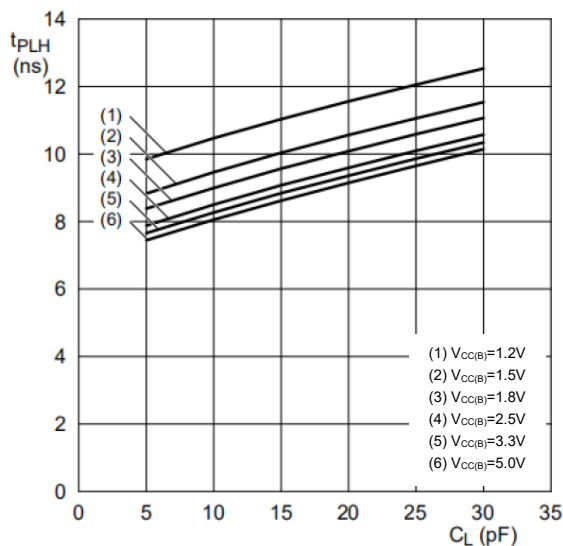
a. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)} = 1.2V$



b. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)} = 1.2V$

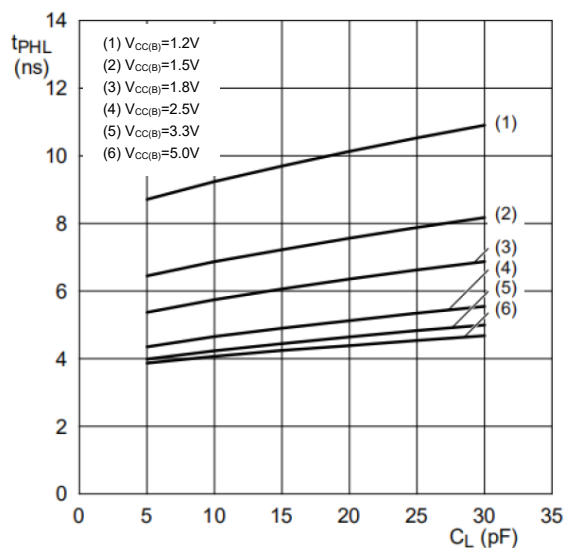


c. HIGH to LOW propagation delay (B to A);
 $V_{CC(A)} = 1.2V$

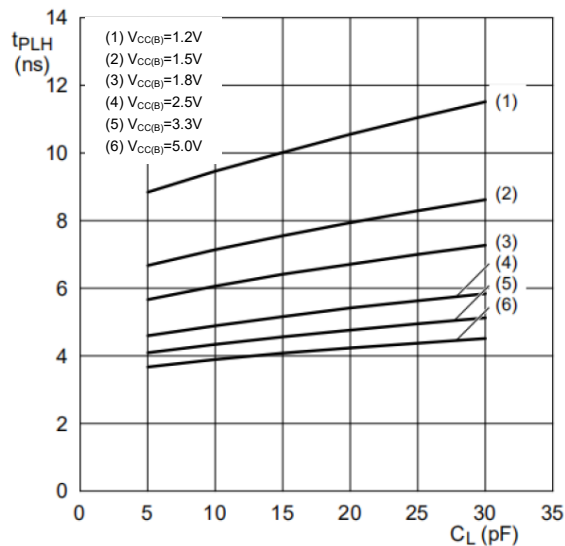


d. LOW to HIGH propagation delay (B to A);
 $V_{CC(A)} = 1.2V$

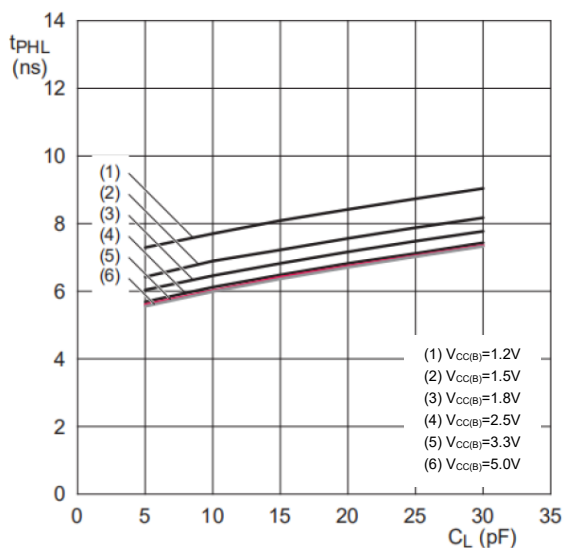
Figure 9-1 Typical propagation delay versus load capacitance; $T_{amb} = 25^\circ C$



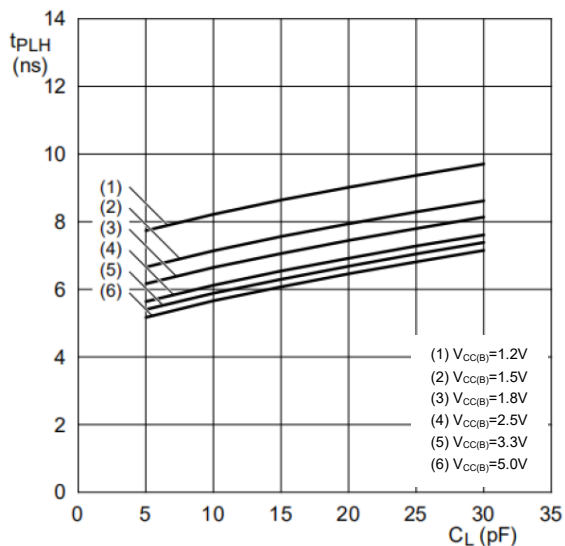
a. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)}=1.5V$



b. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)}=1.5V$

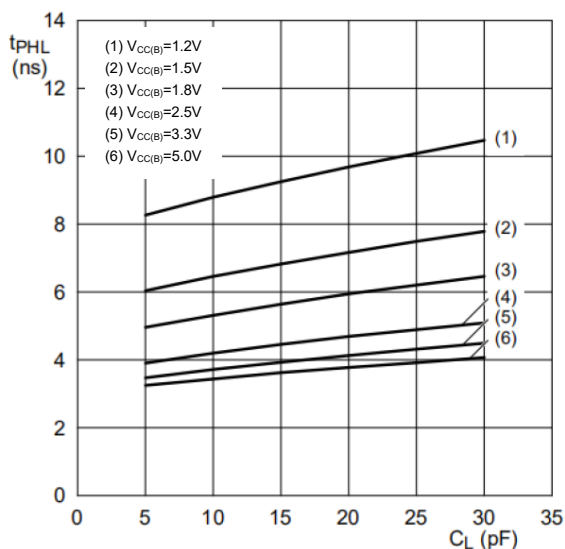


c. HIGH to LOW propagation delay (B to A);
 $V_{CC(A)}=1.5V$

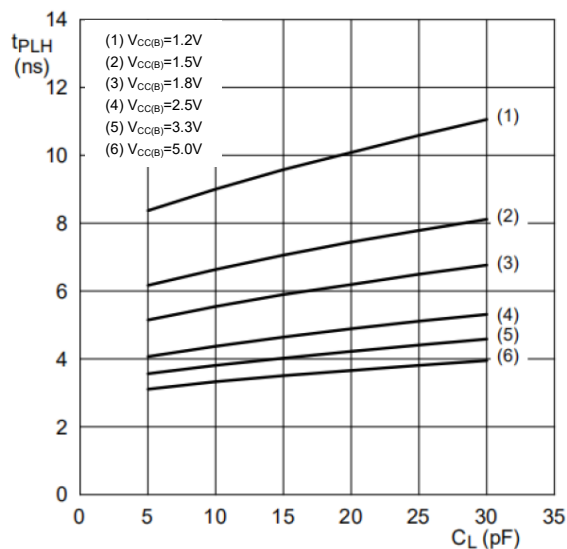


d. LOW to HIGH propagation delay (B to A);
 $V_{CC(A)}=1.5V$

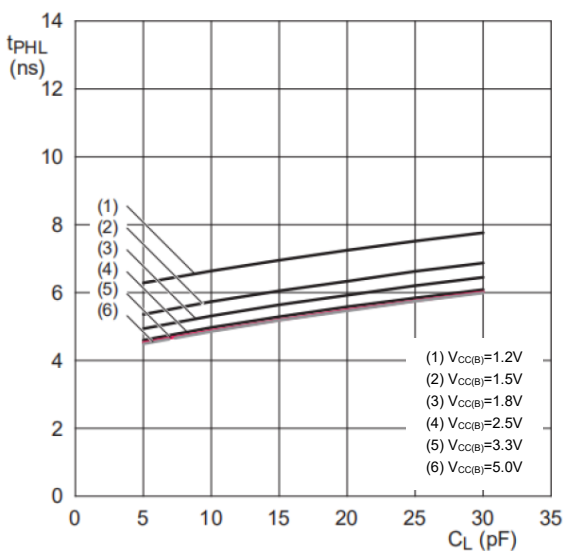
Figure 9-2 Typical propagation delay versus load capacitance; $T_{amb}=25^{\circ}C$



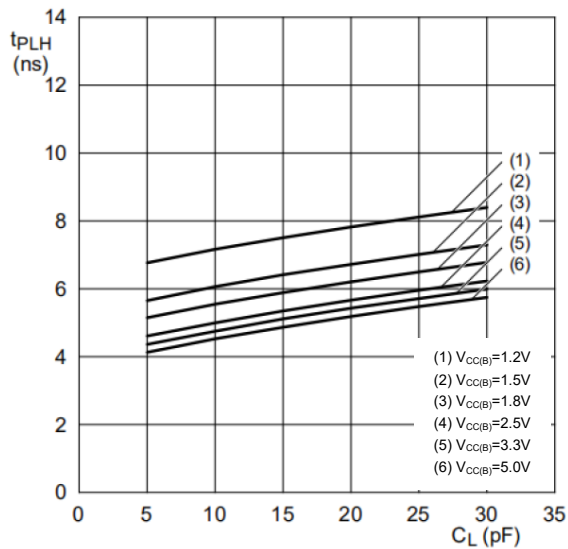
a. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)}=1.8V$



b. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)}=1.8V$

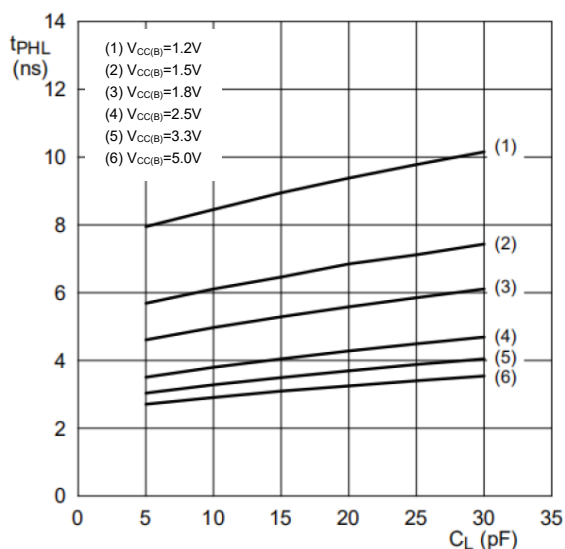


c. HIGH to LOW propagation delay (B to A);
 $V_{CC(A)}=1.8V$

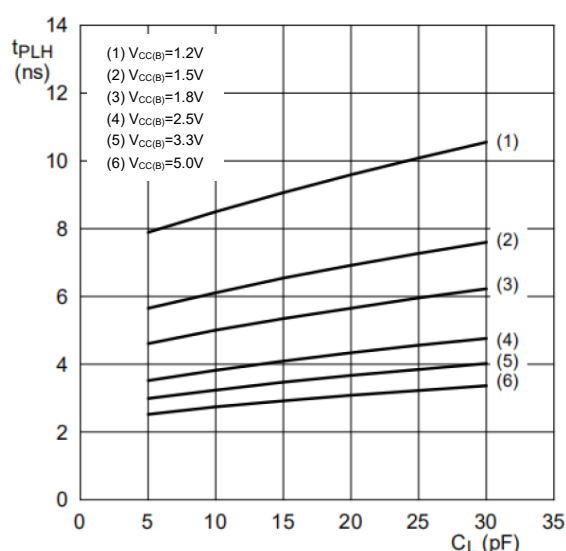


d. LOW to HIGH propagation delay (B to A);
 $V_{CC(A)}=1.8V$

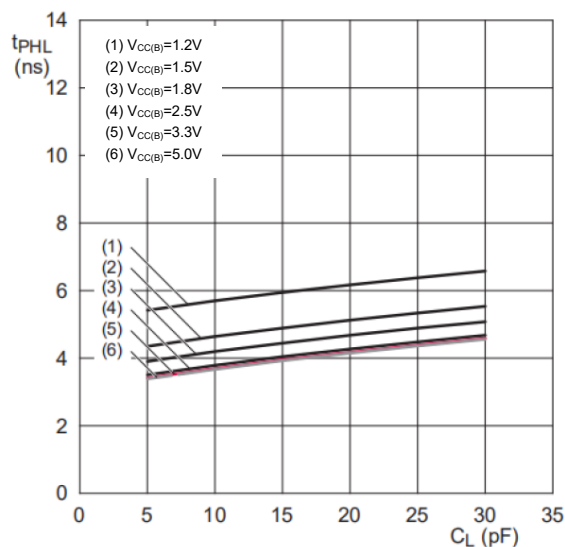
Figure 9-3 Typical propagation delay versus load capacitance; $T_{amb}=25^{\circ}C$



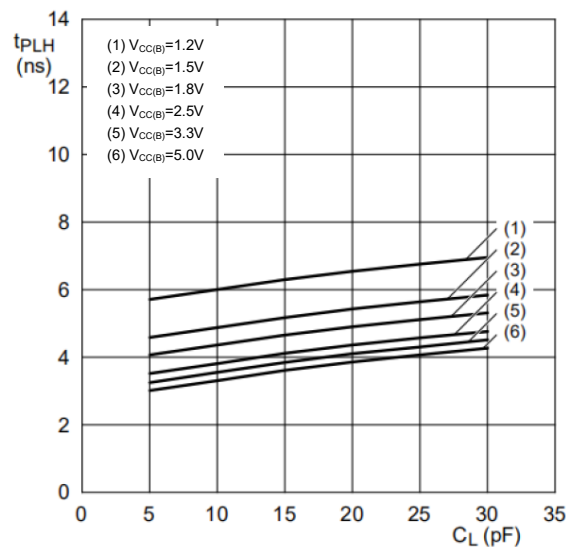
a. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)}=2.5V$



b. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)}=2.5V$

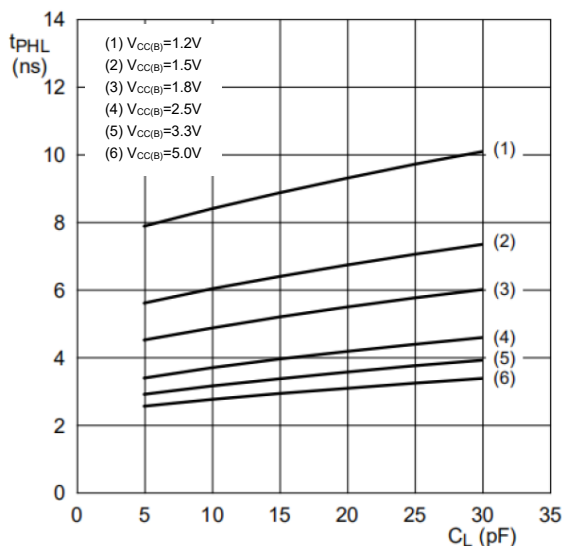


c. HIGH to LOW propagation delay (B to A);
 $V_{CC(A)}=2.5V$

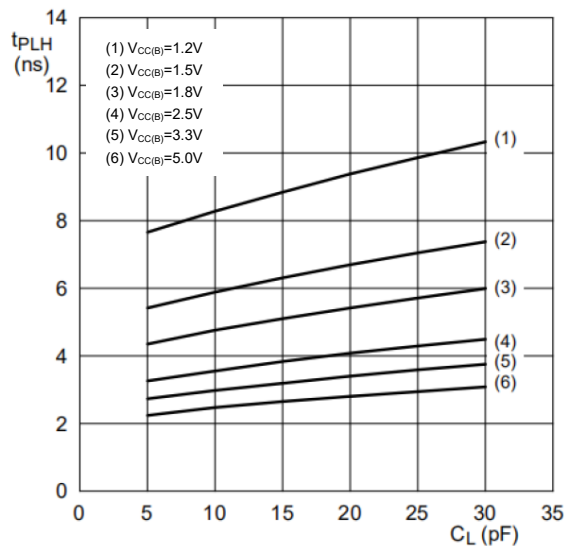


d. LOW to HIGH propagation delay (B to A);
 $V_{CC(A)}=2.5V$

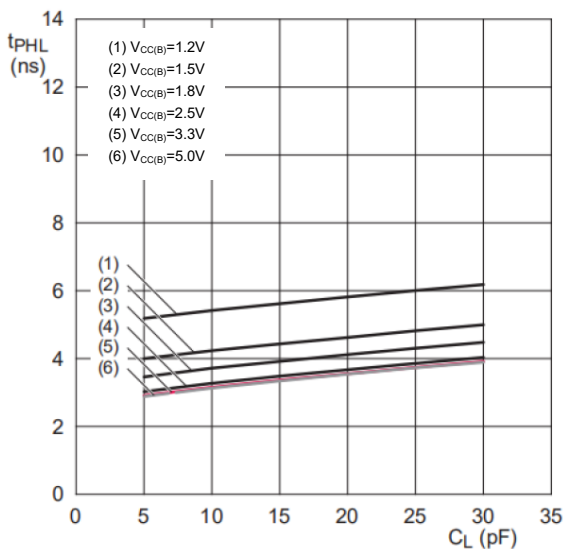
Figure 9-4 Typical propagation delay versus load capacitance; $T_{amb}=25^{\circ}C$



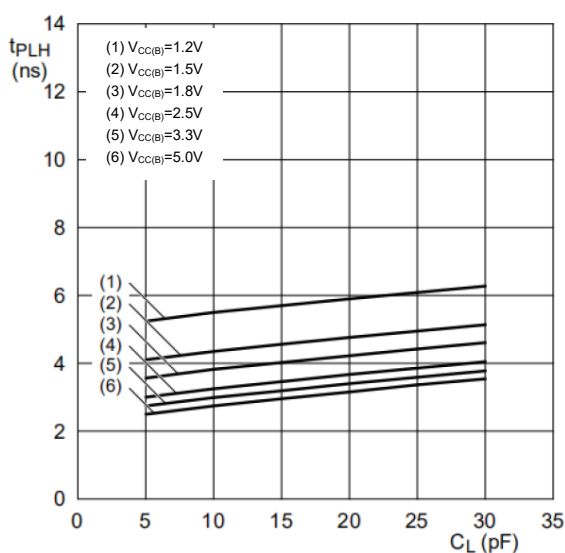
a. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)}=3.3V$



b. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)}=3.3V$

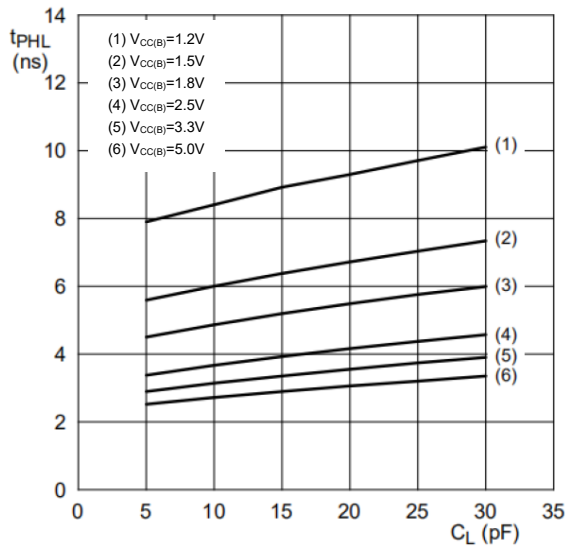


c. HIGH to LOW propagation delay (B to A);
 $V_{CC(A)}=3.3V$

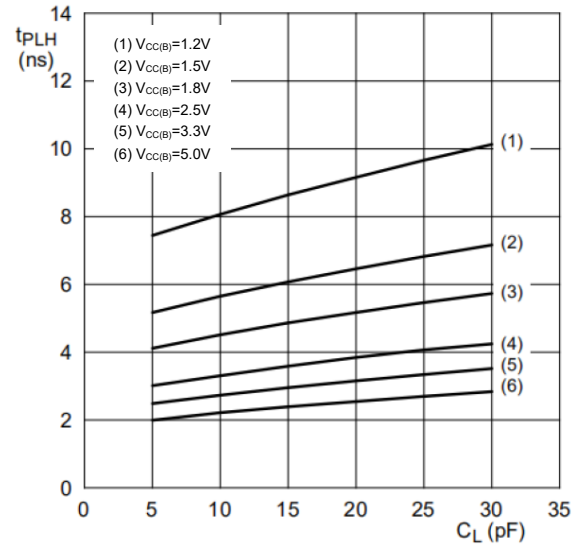


d. LOW to HIGH propagation delay (B to A);
 $V_{CC(A)}=3.3V$

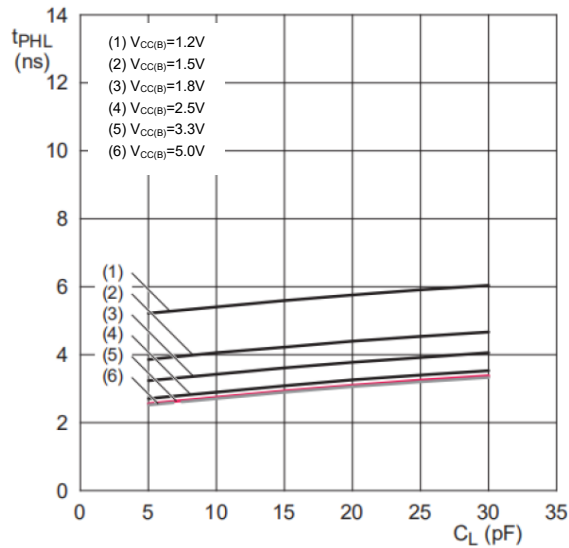
Figure 9-5 Typical propagation delay versus load capacitance; $T_{amb}=25^{\circ}C$



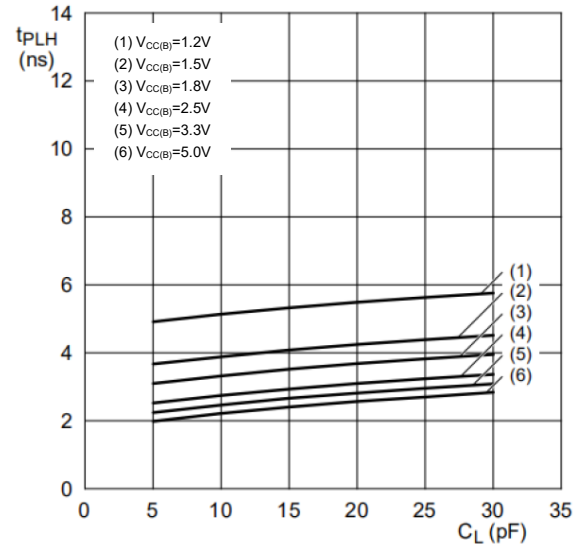
a. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)}=5.0V$



b. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)}=5.0V$



c. HIGH to LOW propagation delay (B to A);
 $V_{CC(A)}=5.0V$



d. LOW to HIGH propagation delay (B to A);
 $V_{CC(A)}=5.0V$

Figure 9-6 Typical propagation delay versus load capacitance; $T_{amb}=25^{\circ}C$

10 Typical Application Circuit and Application Note

10.1 Application Circuit 1

The circuit given in Figure 10-1 is an example of the CJ74LVC8T245; CJ74LVCH8T245 being used in an unidirectional logic level-shifting application.

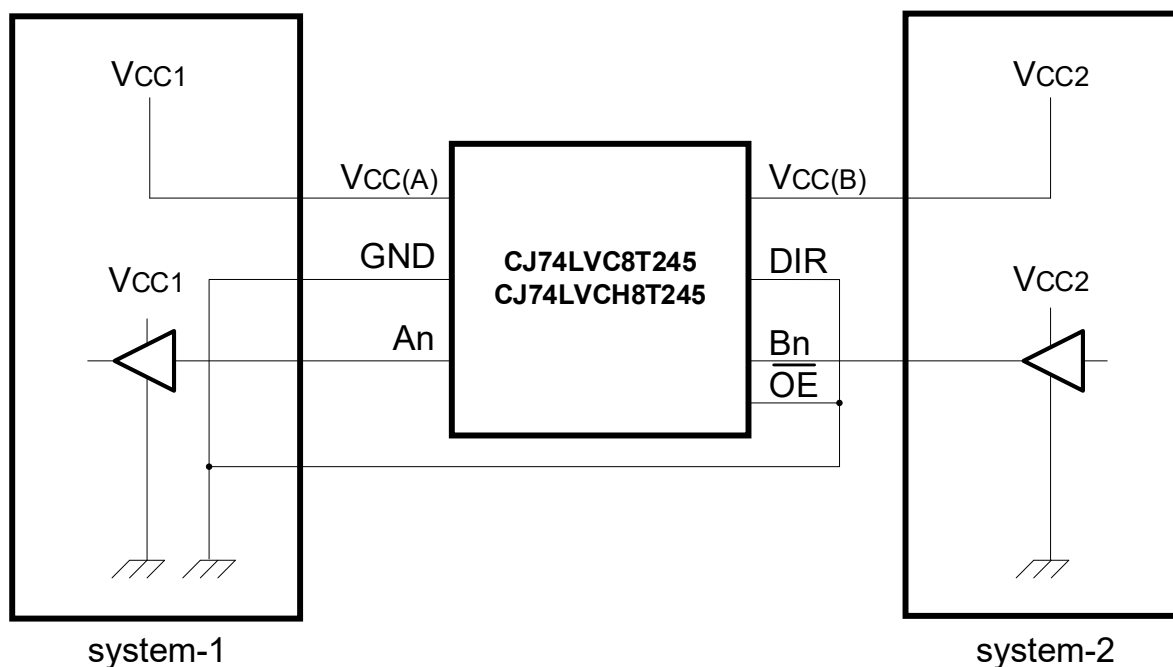


Figure 10-1 Unidirectional logic level-shifting application

NOTE: Schematic given for one channel.

Description unidirectional logic level-shifting application

PIN	NAME	FUNCTION	DESCRIPTION
1	V _{CC(A)}	V _{CC1}	Supply voltage of system-1 (1.2V to 5.5V)
2	GND	GND	Device GND
3	A	OUT	Output level depends on V _{CC1} voltage
4	B	IN	Input threshold value depends on V _{CC2} voltage
5	DIR	DIR	The GND (LOW level) determines B port to A port direction
6	V _{CC(B)}	V _{CC2}	Supply voltage of system-2 (1.2V to 5.5V)
7	$\overline{\text{OE}}$	$\overline{\text{OE}}$	The GND (LOW level) enables the output ports

10.2 Application Circuit 2

Figure 10-2 shows the CJ74LVC8T245; CJ74LVCH8T245 being used in a bidirectional logic level-shifting application.

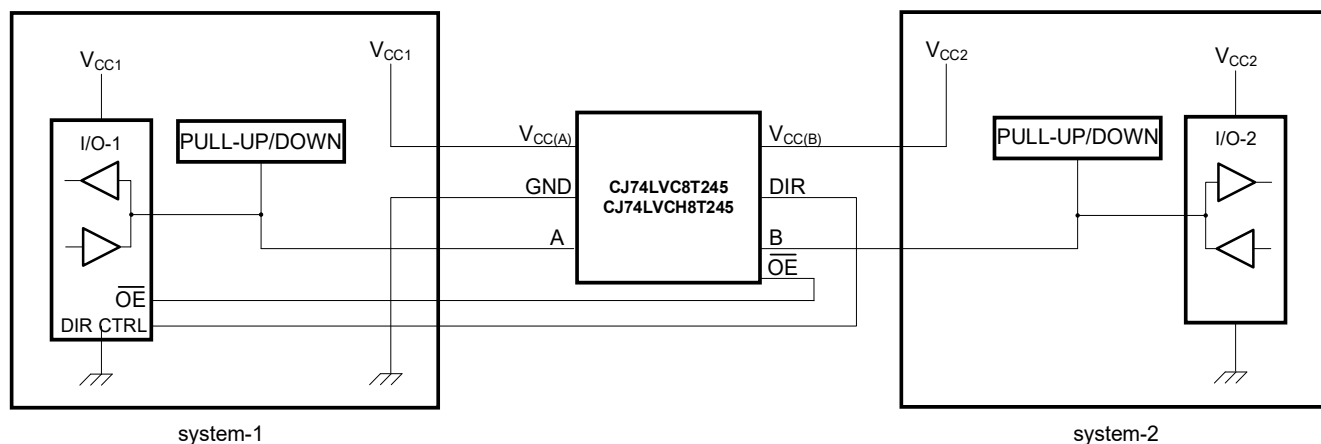


Figure 10-2 Bidirectional logic level-shifting application

NOTE: Schematic given for one channel. Pull-up or pull-down only needed for CJ74LVC8T245.

The following table gives a sequence that will illustrate data transmission from system-1 to system-2 and then from system-2 to system-1.

STATE	DIR CTRL	OE	I/O-1	I/O-2	DESCRIPTION
1	H	L	output	input	System-1 data to system-2
2	H	H	Z	Z	System-2 is getting ready to send data to system-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on bus hold.
3	L	H	Z	Z	DIR bit is set LOW. I/O-1 and I/O-2 still are disabled. The bus-line state depends on bus hold.
4	L	L	input	output	System-2 data to system-1

Note: H=HIGH voltage level; L=LOW voltage level; Z=high-impedance OFF-state.

10.3 Power-up Considerations

The device is designed such that no special power-up sequence is required other than GND being applied first.

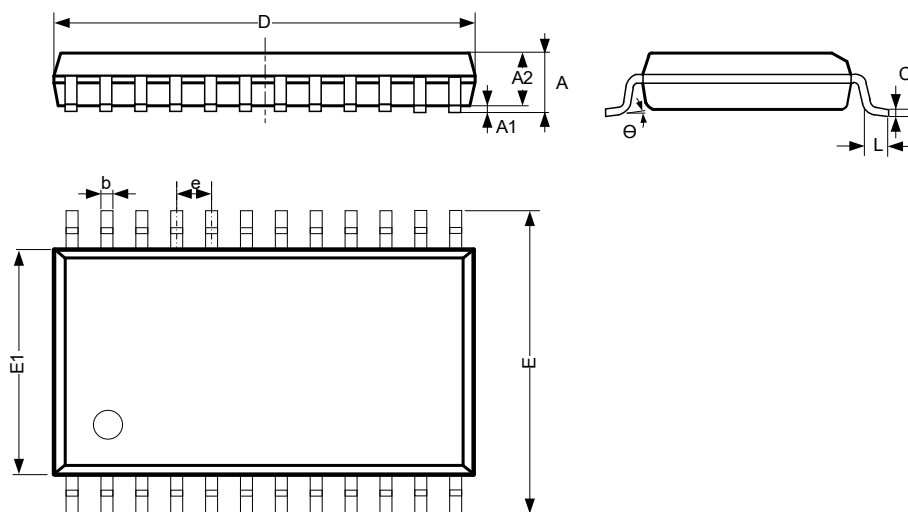
Typical total supply current ($I_{CC(A)} + I_{CC(B)}$)

$V_{CC(A)}$	$V_{CC(B)}$					UNIT
	0V	1.8V	2.5V	3.3V	5.0V	
0V	0	<1	<1	<1	<1	uA
1.8V	<1	<2	<2	<2	2	uA
2.5V	<1	<2	<2	<2	<2	uA
3.3V	<1	<2	<2	<2	<2	uA
5.0V	<1	2	<2	<2	<2	uA

11 Mechanical Information

11.1 TSSOP24 Mechanical Information

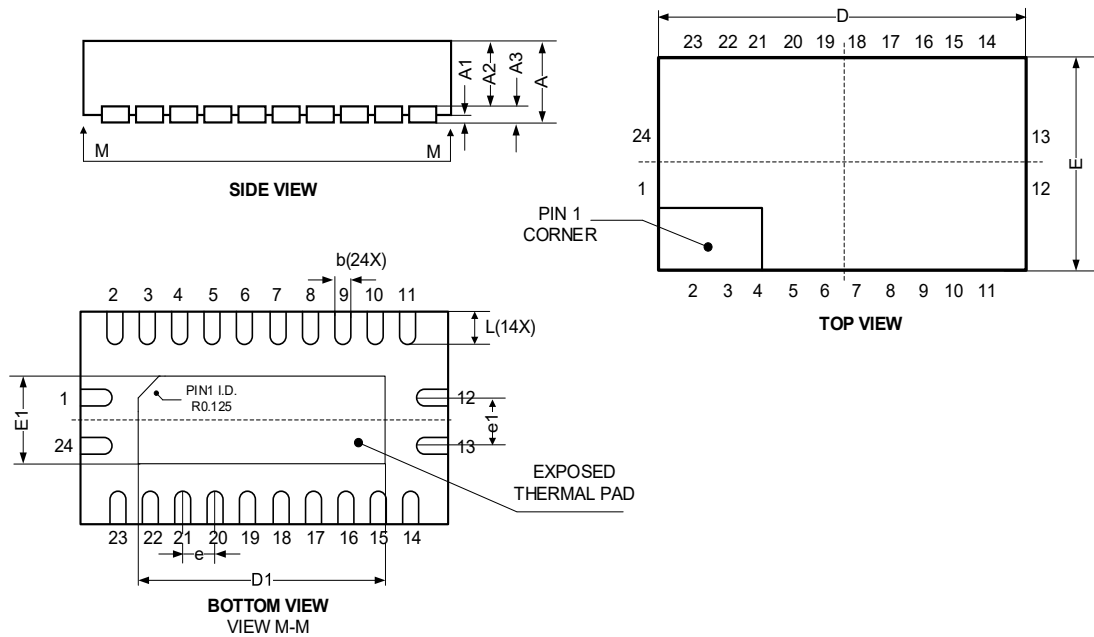
11.1.1 TSSOP24 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	7.70	-	7.90
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
θ	0°	-	8°
Unit: mm			

11.2 QFN5.5x3.5-24L Mechanical Information

11.2.1 QFN5.5x3.5-24L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.80	-	1.00
A1	0.00	-	0.05
A2	0.60	-	0.70
A3	-	0.20	-
D	5.40	-	5.60
E	3.40	-	3.60
e	0.50 BSC		
e1	-	1.50	-
b	0.18	-	0.30
L	0.30	-	0.50
D1	3.95	-	4.25
E1	1.95	-	2.25
Unit: mm			

12 Notes and Revision History

12.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- <https://www.jscj-elec.com> for more details.

12.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

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