Quad single-pole single-throw analog switch

CD4066H Logic

1 Introduction

The CD4066H provides four single-pole, single-throw analog switch functions.

It operates over a recommended V_{DD} power supply range of 3V to 18V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2 Available Packages

PART NUMBER	PACKAGE
CD4066H	SOP14
	TSSOP14

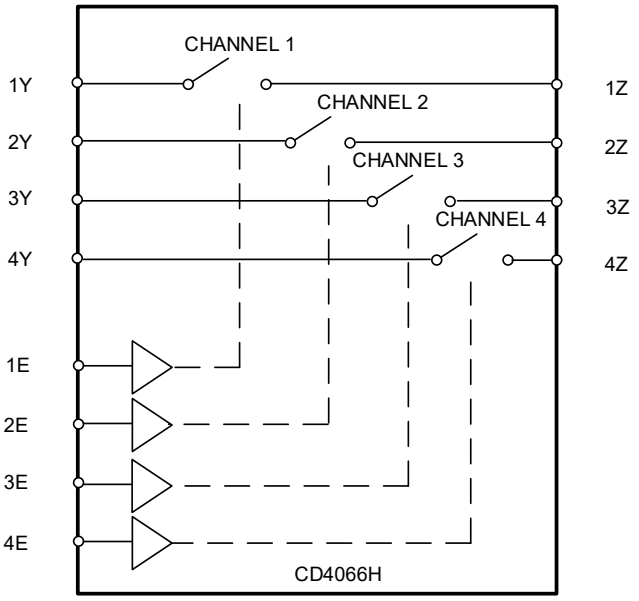
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Supply voltage range: 3V to 18V
- Temperature range: -40°C to +125°C

4 Applications

- Analog signal switching and multiplexing:
  - Signal gating, modulators, squelch controls
  - Demodulators, choppers, commutating switches
- Digital signal switching and multiplexing
- Analog-to-digital and digital-to-analog conversions
- Digital control of frequency, impedance, phase, and analog-signal gain
- Building automation



Function diagram

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CD4066HADN	SOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active
CD4066HBDN	TSSOP14	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

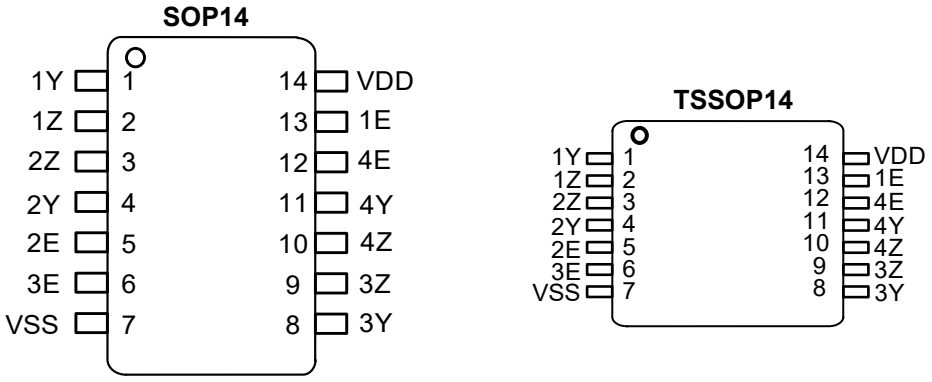


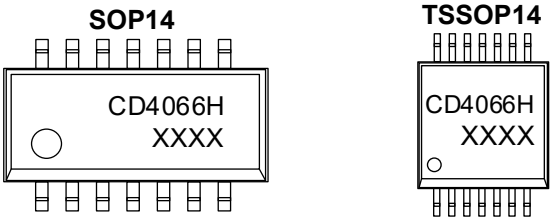
Figure 6-1 Pin Configuration

6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	1Y	I/O	Independent input or output
2	1Z	I/O	Independent input or output
3	2Z	I/O	Independent input or output
4	2Y	I/O	Independent input or output
5	2E	I	Enable input (active HIGH)
6	3E	I	Enable input (active HIGH)
7	VSS	G	Ground (0V)
8	3Y	I/O	Independent input or output
9	3Z	I/O	Independent input or output
10	4Z	I/O	Independent input or output
11	4Y	I/O	Independent input or output
12	4E	I	Enable input (active HIGH)
13	1E	I	Enable input (active HIGH)
14	VDD	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



CD4066H: Device number.
XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{DD}	Supply voltage	-		-0.5	+21	V
V_I	Input voltage	All inputs		-0.5	V_{DD}+0.5	V
I_{IK}	DC input current	Any one input		-	±10	mA
T_{stg}	Storage temperature	-		-65	+150	°C
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	°C

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	-	3	-	18	V
T_{amb}	Ambient temperature	In free air	-40	-	+125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM)(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

T_{amb}=-40°C to +85°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	V_{DD}	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	5V	-	3.5	-	-	V
		10V	-	7	-	-	V
		18V	-	12.6	-	-	V
V_{IL}	LOW-level input voltage	5V	-	-	-	1.5	V
		10V	-	-	-	3	V
		18V	-	-	-	5.4	V
I_I	Input leakage current	18V	V_I=18V or GND	-	-	±1.0	uA
$I_{S(OFF)}$	OFF-state leakage current	18V	Per channel	-	-	±1.0	uA
I_{DD}	Supply current	5V	V_I=5V or GND; I_O=0A	-	-	150	uA
		10V	V_I=10V or GND; I_O=0A	-	-	300	uA
		18V	V_I=18V or GND; I_O=0A	-	-	600	uA
$R_{ON(peak)}$	ON resistance(peak)	5V	V_I=0V~V_{DD}	-	117	836	Ω

		10V		-	58	178	Ω
		15V		-	41	120	Ω
		20V		-	36	105	Ω
$R_{ON(rail)}$	ON resistance(rail)	5V	V_I=0V	-	44	130	Ω
		10V		-	29	93	Ω
		15V		-	24	69	Ω
		20V		-	22	63	Ω
		5V	V_I=V_{DD}	-	82	249	Ω
		10V		-	51	157	Ω
		15V		-	41	127	Ω
		20V		-	36	112	Ω
ΔR_{ON}	ON resistance Mismatch between channels	5V	V_I=0V~V_{DD}	-	25	-	Ω
		10V		-	10	-	Ω
		15V		-	5	-	Ω
		20V		-	5	-	Ω

7.4.2 DC Characteristics 2

T_{amb}=-40°C to +125°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	CHARACTERISTIC	V_{DD}	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	HIGH-level input voltage	5V	-	3.5	-	-	V
		10V	-	7	-	-	V
		18V	-	12.6	-	-	V
V_{IL}	LOW-level input voltage	5V	-	-	-	1.5	V
		10V	-	-	-	3	V
		18V	-	-	-	5.4	V
I_I	Input leakage current	18V	V_I=18V or GND	-	-	±1.0	uA
$I_{S(OFF)}$	OFF-state leakage current	18V	Per channel	-	-	±1.0	uA
I_{DD}	Supply current	5V	V_I=5V or GND; I_O=0A	-	-	150	uA
		10V	V_I=10V or GND; I_O=0A	-	-	300	uA
		18V	V_I=18V or GND; I_O=0A	-	-	600	uA
$R_{ON(peak)}$	ON resistance(peak)	5V	V_I=0V~V_{DD}	-	-	836	Ω
		10V		-	-	178	Ω
		15V		-	-	120	Ω
		20V		-	-	105	Ω
$R_{ON(rail)}$	ON resistance(rail)	5V	V_I=0V	-	-	130	Ω
		10V		-	-	93	Ω
		15V		-	-	69	Ω
		20V		-	-	63	Ω

		5V	$V_I=V_{DD}$	-	-	249	Ω
		10V		-	-	157	Ω
		15V		-	-	127	Ω
		20V		-	-	112	Ω

7.4.3 AC Characteristics 3

T_{amb}=-40°C to +85°C, V_{SS}=0V, unless otherwise specified.

SYMBOL	CHARACTERISTIC	V_{DD}	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PHL}	HIGH to LOW propagation delay time	5V	nY to nZ;nZ to nY See Figure 8-3	-	10	20	ns
		10V		-	5	10	ns
		18V		-	5	10	ns
t_{PLH}	LOW to HIGH propagation delay time	5V	nY to nZ;nZ to nY See Figure 8-3	-	10	20	ns
		10V		-	5	10	ns
		18V		-	5	10	ns
t_{PHZ}	HIGH to OFF-state propagation delay time	5V	nE to nY;nZ See Figure 8-4	-	80	160	ns
		10V		-	65	130	ns
		18V		-	60	120	ns
t_{PLZ}	LOW to OFF-state propagation delay time	5V	nE to nY;nZ See Figure 8-4	-	80	160	ns
		10V		-	70	140	ns
		18V		-	70	140	ns
t_{PZH}	OFF-state to HIGH propagation delay time	5V	nE to nY;nZ See Figure 8-4	-	40	80	ns
		10V		-	20	40	ns
		18V		-	15	30	ns
t_{PZL}	OFF-state to LOW propagation delay time	5V	nE to nY;nZ See Figure 8-4	-	45	90	ns
		10V		-	20	40	ns
		18V		-	15	30	ns
THD	Total harmonic distortion	5V	R_L=10K, C_L=15pF Channel ON; V_I=0.55V_{DD}(p-p) f_i=1kHz; See Figure 8-3	-	0.25	-	%
		10V		-	0.04	-	%
		18V		-	0.04	-	%
V_{ct}	Crosstalk voltage(nE to nY to nZ	10V	R_L=10K, C_L=15pF nE=V_{DD}（square-wave） See Figure 8-4	-	50	-	mV
Xtalk	Crosstalk	10V	Between switches; f_i=1MHz; R_L=1kΩ; V_I=0.5V_{DD} (p-p) See Figure 8-5	-	-50	-	dB
αiso	OFF frequency	10V	f_i=1MHz; R_L=1kΩ; C_L=5pF; V_I=0.5V_{DD} (p-p) See Figure 8-6	-	-50	-	dB
$f_{(-3dB)}$	-3 dB frequency response	10V	R_L=1kΩ; C_L=5pF; V_I=0.5V_{DD} (p-p) See Figure 8-7	-	90	-	MHz

7.4.4 AC Characteristics 4

T_{amb} =-40°C to +125°C, V_{SS}=0V, unless otherwise specified.

SYMBOL	CHARACTERISTIC	V_{DD}	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{PHL}	HIGH to LOW propagation delay time	5V	nY to nZ;nZ to nY See Figure 8-8	-	-	24	ns
		10V		-	-	12	ns
		18V		-	-	12	ns
t_{PLH}	LOW to HIGH propagation delay time	5V	nY to nZ;nZ to nY See Figure 8-8	-	-	24	ns
		10V		-	-	12	ns
		18V		-	-	12	ns
t_{PHZ}	HIGH to OFF-state propagation delay time	5V	nE to nY;nZ See Figure 8-9	-	-	192	ns
		10V		-	-	156	ns
		18V		-	-	144	ns
t_{PLZ}	LOW to OFF-state propagation delay time	5V	nE to nY;nZ See Figure 8-9	-	-	192	ns
		10V		-	-	156	ns
		18V		-	-	156	ns
t_{PZH}	OFF-state to HIGH propagation delay time	5V	nE to nY;nZ See Figure 8-9	-	-	96	ns
		10V		-	-	48	ns
		18V		-	-	36	ns
t_{PZL}	OFF-state to LOW propagation delay time	5V	nE to nY;nZ See Figure 8-9	-	-	108	ns
		10V		-	-	48	ns
		18V		-	-	36	ns
THD	Total harmonic distortion	5V	R_L=10K, C_L=15pF Channel ON; V_I=0.55V_{DD}(p-p) f_i=1kHz; See Figure 8-3	-	0.25	-	%
		10V		-	0.04	-	%
		18V		-	0.04	-	%
V_{ct}	Crosstalk voltage(nE to nY to nZ)	10V	R_L=10K, C_L=15pF nE=V_{DD}（square-wave） See Figure 8-4	-	50	-	mV
Xtalk	Crosstalk	10V	Between switches; f_i=1MHz; R_L=1kΩ; V_I=0.5V_{DD} (p-p) See Figure 8-5	-	-50	-	dB
αiso	OFF frequency	10V	f_i=1MHz; R_L=1kΩ; C_L=5pF; V_I=0.5V_{DD} (p-p) See Figure 8-6	-	-50	-	dB
$f_{(-3dB)}$	-3 dB frequency response	10V	R_L=1kΩ; C_L=5pF; V_I=0.5V_{DD} (p-p) See Figure 8-7	-	90	-	MHz

8 Detailed Description

8.1 Overview

The CD4066H provides four single-pole, single-throw analog switch functions.

It operates over a recommended V_{DD} power supply range of 3V to 18V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

8.2 Functional Block Diagram

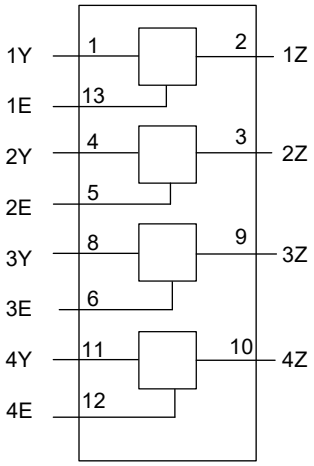


Figure 8-1 Functional diagram

8.3 Function Table(1)

INPUT	SWITCH
nE	
H	ON
L	OFF

(1) H=HIGH voltage level; L=LOW voltage level.

8.4 Testing Circuit

8.4.1 AC Testing Circuit

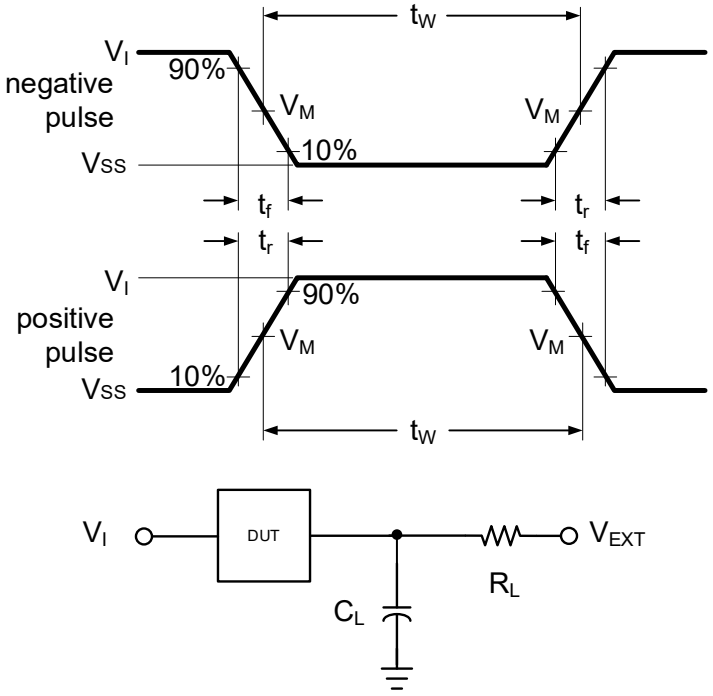


Figure 8-2 Load circuit

C_L= Includes probe and jig capacitance.

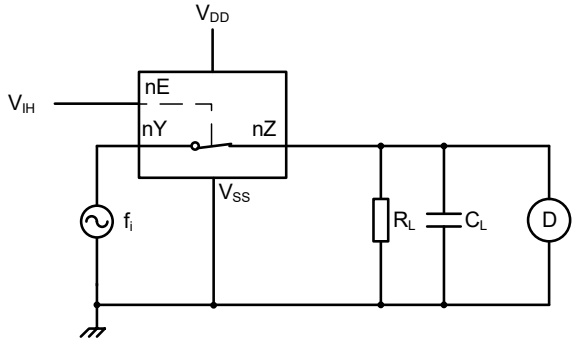
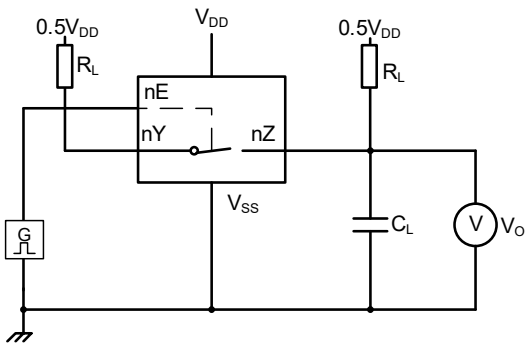


Figure 8-3 Test circuit for measuring total harmonic distortion



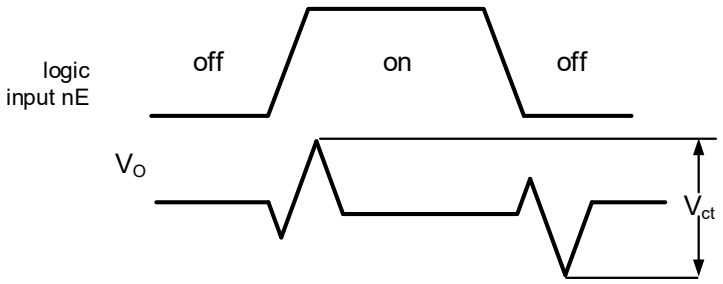


Figure 8-4 Test circuit for measuring crosstalk voltage between digital input and switch

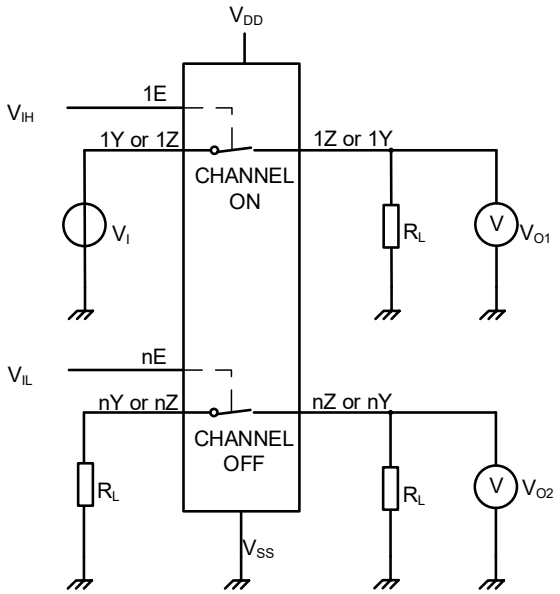


Figure 8-5 Test circuit for measuring crosstalk voltage between switches

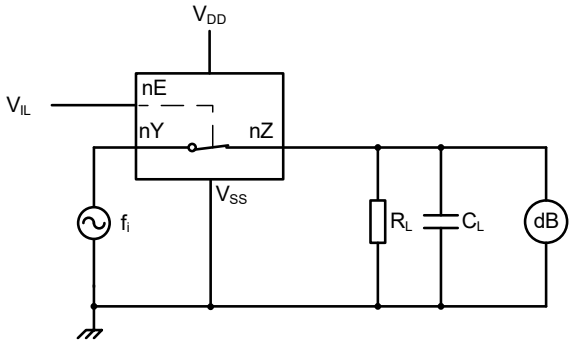


Figure 8-6 Test circuit for measuring isolation (OFF-state)

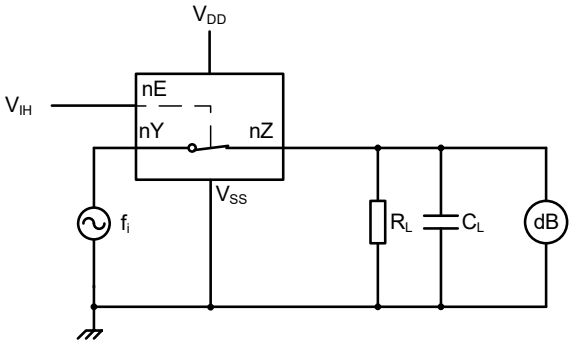


Figure 8-7 Test circuit for measuring frequency response

8.4.2 AC Testing Waveforms

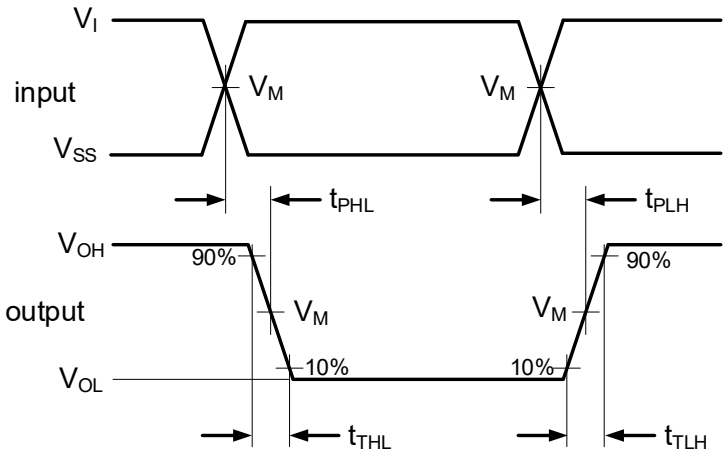


Figure 8-8 Propagation delay, output transition time

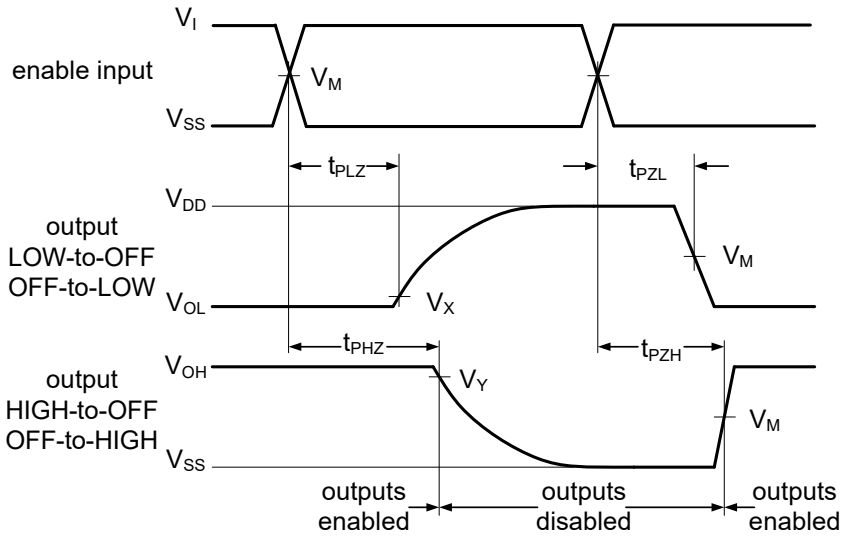


Figure 8-9 3-state enable and disable times

8.4.3 Measurement Points

Supply voltage	INPUT	OUTPUT
V_{DD}	V_M	V_M
5V to 18V	$0.5xV_{DD}$	$0.5xV_{DD}$

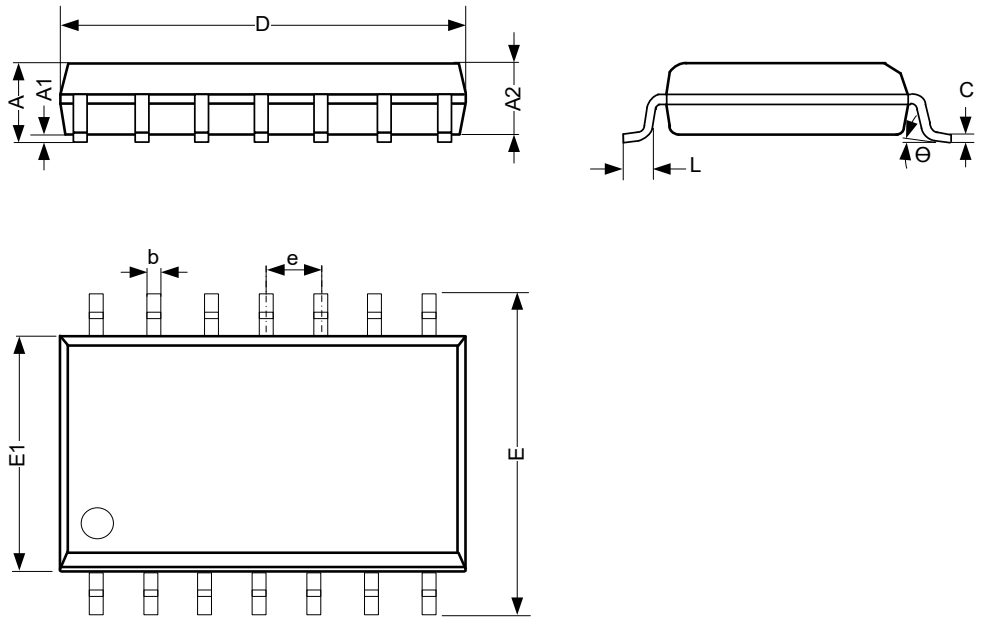
8.4.4 Test Data

SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}		
V_{DD}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}/t_{PHL}	t_{PLZ}/t_{PZL}	t_{PHZ}/t_{PZH}
5V to 18V	V_{CC}	≤ 20ns	50pF	10kΩ	Open	V_{DD}	V_{SS}

9 Mechanical Information

9.1 SOP14 Mechanical Information

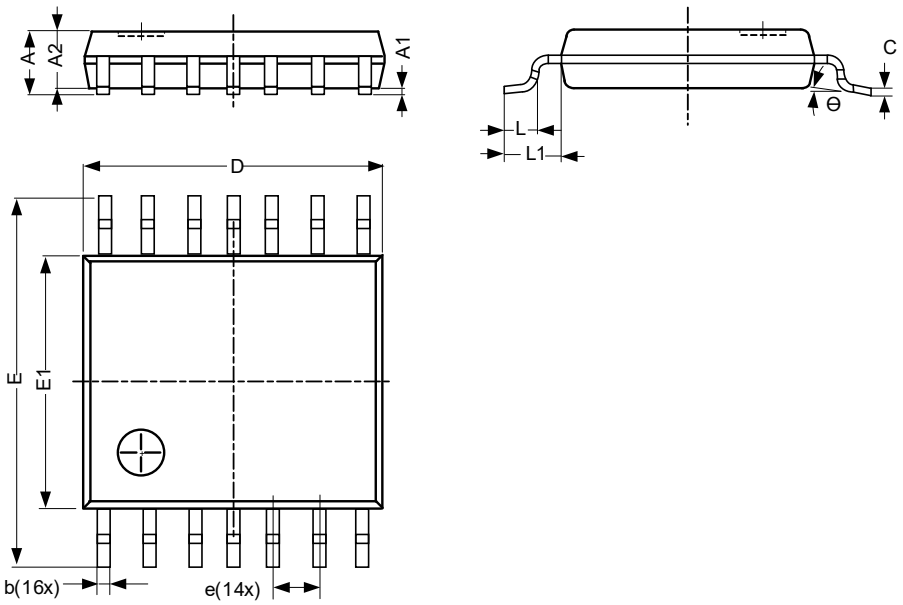
9.1.1 SOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.50	-	1.75
A1	0.05	-	0.25
A2	1.30	-	-
b	0.33	-	0.50
c	0.19	-	0.25
D	8.43	-	8.76
E	5.80	-	6.25
E1	3.75	-	4.00
e	1.27 BSC		
L	0.40	-	0.89
Θ	0°	-	8°
Unit: mm			

9.2 TSSOP14 Mechanical Information

9.2.1 TSSOP14 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
L1	-	1.00	-
Θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

June, 2025: rev - 1.1, Make pin name consistent as nY/nZ/nE .

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

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