

Triple 2-channel Analog Multiplexer/Demultiplexer

CD4053H

Logic

1 Introduction

The CD4053H is a triple single-pole double-throw (SPDT) analog switch, suitable for use as an analog or digital multiplexer/demultiplexer. Each switch has a digital select input (S_n), two independent inputs/outputs (nY_0 and nY_1) and a common input/output (nZ). All three switches share an enable input ($/E$). A HIGH on $/E$ causes all switches into the high-impedance OFF-state, independent of S_n .

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S_n and $/E$). The V_{DD} to V_{SS} range is 3V to 18V. The analog inputs/outputs (nY_0 , nY_1 , and nZ) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD}-V_{EE}$ may not exceed 18V. Unused inputs must be connected to V_{DD} , V_{SS} , or another input. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground). V_{EE} and V_{SS} are the supply voltage connections for the switches.

2 Available Packages

PART NUMBER	PACKAGE
CD4053H	SOP16
	TSSOP16

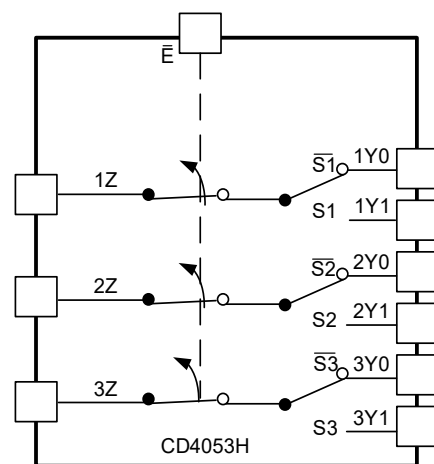
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- Wide supply voltage range from 3V to 18V
- Fully static operation
- 5V, 10V and 18V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to $+125^{\circ}\text{C}$

4 Applications

- Analog and digital multiplexing and demultiplexing
- Analog to digital and digital to analog conversion
- Signal gating
- Factory automation
- Televisions
- Appliances
- Consumer audio
- Programmable logic circuits
- Sensors



Functional diagrams

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CD4053HAEN	SOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units/Reel	Active
CD4053HBEN	TSSOP16	-40~125°C	RoHS & Green	Level 3 168HR	Tape and Reel 5000 Units/Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

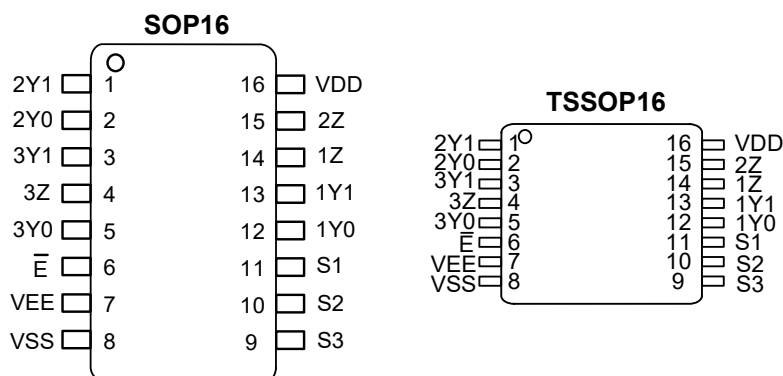


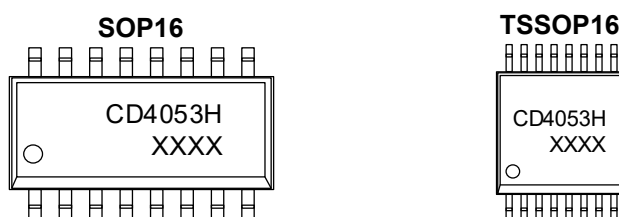
Figure 6-1 Pin configuration

6.2 Pin Function

PIN		I/O ⁽¹⁾	DESCRIPTION
No.	NAME		
1	2Y1	I/O	Independent input or output
2	2Y0	I/O	Independent input or output
3	3Y1	I/O	Independent input or output
4	3Z	I/O	Independent output or input
5	3Y0	I/O	Independent input or output
6	$\bar{E}$	I	Enable input (active LOW)
7	VEE	P	Supply voltage
8	VSS	G	Ground (0V)
9	S3	I	Select input
10	S2	I	Select input
11	S1	I	Select input
12	1Y0	I/O	Independent input or output
13	1Y1	I/O	Independent input or output
14	1Z	I/O	Independent output or input
15	2Z	I/O	Independent output or input
16	VDD	P	Supply voltage

(1) I-Input, O-Output, P-Power, G-Ground.

6.3 Marking Information



XXXX: Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

$T_{amb}=25^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{DD}	Supply voltage	-		-0.5	+21	V
V_{EE}	Supply voltage	Referenced to V_{DD}		-21	+0.5	V
V_I	Input voltage	-		-0.5	$V_{DD}+0.5$	V
I_{IK}	Input clamping current	$V_I < -0.5\text{V}$ or $V_I > V_{DD}+0.5\text{V}$		-	± 10	mA
I_{IO}	Input/output current	-		-	± 10	mA
I_{DD}	Supply current	-		-	50	mA
T_{stg}	Storage temperature	-		-65	+150	$^{\circ}\text{C}$
T_{amb}	Ambient temperature	-		-40	+125	$^{\circ}\text{C}$
P_{tot}	Total power dissipation	-		-	500	mW
P	Device dissipation	Per output transistor		-	100	mW
T_L	Soldering temperature	10s	SOP/TSSOP	-	260	$^{\circ}\text{C}$

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

7.2 Recommended Operating Conditions

$T_{amb}=25^{\circ}\text{C}$; $R_L=10\text{k}\Omega$; $C_L=50\text{pF}$; $/E=V_{DD}$; $V_{IS}=V_{DD}=5\text{V}$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	-	3	-	18	V
V_{EE}	Supply voltage	-	-15	-	0	V
$V_{DD}-V_{EE}$	Supply voltage	-	3	-	18	V
V_I	Input voltage	-	0	-	V_{DD}	V
T_{amb}	Ambient temperature	In free air	-40	-	+125	$^{\circ}\text{C}$
$\Delta t/\Delta V$	Input transition rise and fall rate	$V_{DD}=5\text{V}$	-	-	3.75	us/V
		$V_{DD}=10\text{V}$	-	-	0.5	us/V
		$V_{DD}=18\text{V}$	-	-	0.08	us/V

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) ⁽¹⁾	± 2000	V

(1) JEDEC document JEP155 states that 500-V H1BM allows safe manufacturing with a standard ESD control process.

7.4 Electrical Characteristics

7.4.1 DC Characteristics 1

$T_{amb}=25^{\circ}\text{C}$, $V_{SS}=V_{EE}=0\text{V}$; $V_I=V_{SS}$ or V_{DD} , $I_{SW}=200\mu\text{A}$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		T _{amb} =25°C			UNIT
				MIN.	TYP.	MAX.	
V _{IH}	HIGH-level input voltage	I _O <1uA	V _{DD} =5V	3.5	-	-	V
			V _{DD} =10V	7.0	-	-	V
			V _{DD} =18V	12.6	-	-	V
V _{IL}	LOW-level input voltage	I _O <1uA	V _{DD} =5V	-	-	1.5	V
			V _{DD} =10V	-	-	3.0	V
			V _{DD} =18V	-	-	5.4	V
I _{DD}	Supply current	I _O =0A	V _{DD} =5V	-	-	5	uA
			V _{DD} =10V	-	-	10	uA
			V _{DD} =18V	-	-	20	uA
I _I	Input leakage current	V _{DD} =18V		-	-	±1.0	uA
I _{S(OFF)}	OFF-state leakage current	V _{DD} =18V	Z port; All channels OFF; See Figure 8-6	-	-	±1.0	uA
			Y port; Per channel; See Figure 8-7	-	-	±1.0	uA
R _{ON(peak)}	ON resistance (peak)	V _I =0V to V _{DD} -V _{EE} ; See Figure 8-8 and Figure 8-9	V _{DD} -V _{EE} =5V	-	117	836	Ω
			V _{DD} -V _{EE} =10V	-	58	178	Ω
			V _{DD} -V _{EE} =15V	-	41	120	Ω
			V _{DD} -V _{EE} =20V	-	36	105	Ω
R _{ON(rail)}	ON resistance (rail)	V _I =0V; See Figure 8-8 and Figure 8-9	V _{DD} -V _{EE} =5V	-	44	130	Ω
			V _{DD} -V _{EE} =10V	-	29	93	Ω
			V _{DD} -V _{EE} =15V	-	24	69	Ω
			V _{DD} -V _{EE} =20V	-	22	63	Ω
		V _I =V _{DD} -V _{EE} ; See Figure 8-8 and Figure 8-9	V _{DD} -V _{EE} =5V	-	82	249	Ω
			V _{DD} -V _{EE} =10V	-	51	157	Ω
			V _{DD} -V _{EE} =15V	-	41	127	Ω
			V _{DD} -V _{EE} =20V	-	36	112	Ω
ΔR _{ON}	ON resistance mismatch between channels	V _I =0V to V _{DD} -V _{EE} ; See Figure 8-8	V _{DD} -V _{EE} =5V	-	25	-	Ω
			V _{DD} -V _{EE} =10V	-	10	-	Ω
			V _{DD} -V _{EE} =15V	-	5	-	Ω
			V _{DD} -V _{EE} =20V	-	5	-	Ω
C _I	Input capacitance	Sn, $\bar{E}$ inputs		-	-	7.5	pF

7.4.2 DC Characteristics 2

$T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{SS} = V_{EE} = 0\text{V}$; $V_I = V_{SS}$ or V_{DD} , unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		T _{amb} =-40°C		T _{amb} =+85°C		T _{amb} =+125°C		UNIT
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V _{IH}	HIGH-level input voltage	I _o <1uA	V _{DD} =5V	3.5	-	3.5	-	3.5	-	V
			V _{DD} =10V	7.0	-	7.0	-	7.0	-	V
			V _{DD} =18V	12.6	-	12.6	-	12.6	-	V
V _{IL}	LOW-level input voltage	I _o <1uA	V _{DD} =5V	-	1.5	-	1.5	-	1.5	V
			V _{DD} =10V	-	3.0	-	3.0	-	3.0	V
			V _{DD} =18V	-	5.4	-	5.4	-	5.4	V
I _{DD}	Supply current	I _o =0A	V _{DD} =5V	-	5	-	150	-	150	uA
			V _{DD} =10V	-	10	-	300	-	300	uA
			V _{DD} =18V	-	20	-	600	-	600	uA
I _I	Input leakage current	V _{DD} =18V		-	±1.0	-	±1.0	-	±1.0	uA

7.4.3 AC Characteristics 1

$T_{amb} = 25^{\circ}\text{C}$, $V_{EE} = V_{SS} = 0\text{V}$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
t _{PHL}	HIGH to LOW propagation delay time	nYn, nZ to nZ, nYn; See Figure 8-11	V _{DD} =5V	-	10	20	ns
			V _{DD} =10V	-	5	10	ns
			V _{DD} =18V	-	5	10	ns
		Sn to nYn, nZ; See figure 8-12	V _{DD} =5V	-	200	400	ns
			V _{DD} =10V	-	85	170	ns
			V _{DD} =18V	-	65	130	ns
t _{PLH}	LOW to HIGH propagation delay	nYn, nZ to nZ, nYn; See Figure 8-11	V _{DD} =5V	-	15	30	ns
			V _{DD} =10V	-	5	10	ns
			V _{DD} =18V	-	5	10	ns
		Sn to nYn, nZ; See Figure 8-12	V _{DD} =5V	-	275	555	ns
			V _{DD} =10V	-	100	200	ns
			V _{DD} =18V	-	65	130	ns
t _{PHZ}	HIGH to OFF-state propagation delay	$\bar{E}$ to nYn, nZ; See Figure 8-13	V _{DD} =5V	-	200	400	ns
			V _{DD} =10V	-	115	230	ns
			V _{DD} =18V	-	110	220	ns
t _{PLZ}	LOW to OFF-state propagation delay	$\bar{E}$ to nYn, nZ; See Figure 8-13	V _{DD} =5V	-	200	400	ns
			V _{DD} =10V	-	120	245	ns
			V _{DD} =18V	-	110	215	ns
t _{PZH}	OFF-state to HIGH propagation delay	$\bar{E}$ to nYn, nZ; See Figure 8-13	V _{DD} =5V	-	260	525	ns
			V _{DD} =10V	-	95	190	ns

			$V_{DD}=18V$	-	65	130	ns
t_{PZL}	OFF-state to LOW propagation delay	$\bar{E}$ to nYn, nZ; See Figure 8-13	$V_{DD}=5V$	-	280	565	ns
			$V_{DD}=10V$	-	105	205	ns
			$V_{DD}=18V$	-	70	140	ns

7.4.4 AC Characteristics 2

$T_{amb}=25^{\circ}C$, $V_{EE}=V_{SS}=0V$, $V_I=0.5V_{DD}$ (p-p), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
THD	Total harmonic distortion	See Figure 8-14; R _L =10kΩ; C _L =15pF; Channel ON; f _i =1kHz	V _{DD} =5V	-	0.25	-	%
			V _{DD} =10V	-	0.04	-	%
			V _{DD} =18V	-	0.04	-	%
f _(-3dB)	-3dB frequency response	See Figure 8-15; R _L =1kΩ; C _L =5pF; Channel ON;	V _{DD} =5V	-	13	-	MHz
			V _{DD} =10V	-	40	-	MHz
			V _{DD} =18V	-	70	-	MHz
α _{iso}	Isolation (OFF-state)	See Figure 8-16; f _i =1MHz; R _L =1kΩ; C _L =5pF; Channel OFF; V _{DD} =10V	-	-50	-	dB	
V _{ct}	Crosstalk voltage	Digital inputs to switch; See Figure 8-17; R _L =10kΩ; C _L =15pF; $\bar{E}$ or Sn=V _{DD} (square-wave); V _{DD} =10V	-	50	-	mV	
Xtalk	Crosstalk	Between switches; See Figure 8-18; f _i =1MHz; R _L =1kΩ; V _{DD} =10V	-	-50	-	dB	

(1) f_i is biased at $0.5V_{DD}$; $V_I=0.5V_{DD}$ (p-p).

8 Detailed Description

8.1 Overview

The CD4053H is a triple single-pole double-throw (SPDT) analog switch, suitable for use as an analog or digital multiplexer/demultiplexer. Each switch has a digital select input (S_n), two independent inputs/outputs (nY_0 and nY_1) and a common input/output (nZ). All three switches share an enable input ($/E$). A HIGH on $/E$ causes all switches into the high-impedance OFF-state, independent of S_n .

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S_n and $/E$). The V_{DD} to V_{SS} range is 3V to 18V. The analog inputs/outputs (nY_0 , nY_1 , and nZ) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD}-V_{EE}$ may not exceed 18V. Unused inputs must be connected to V_{DD} , V_{SS} , or another input. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground). V_{EE} and V_{SS} are the supply voltage connections for the switches.

8.2 Functional Block Diagram

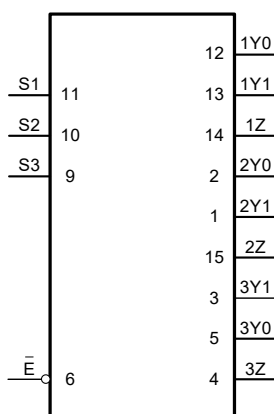


Figure 8-1 Logic symbol

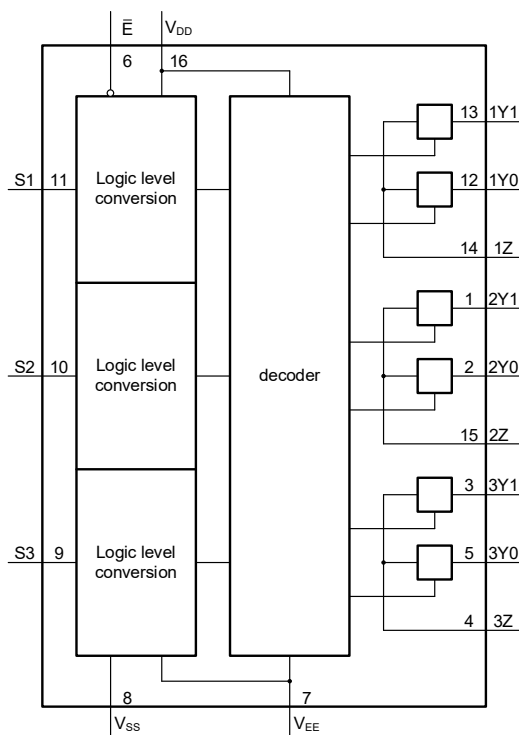


Figure 8-2 Functional diagram

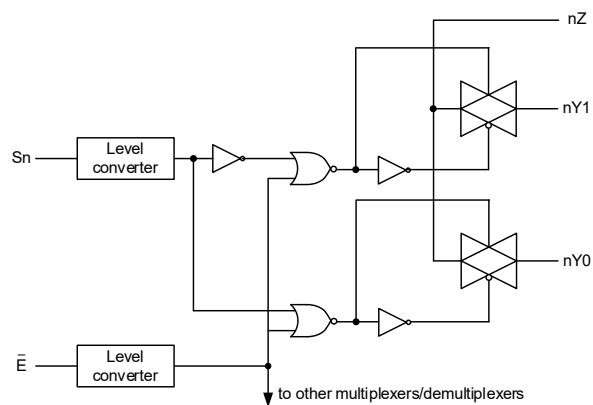


Figure 8-3 Logic diagram (one multiplexer/demultiplexer)

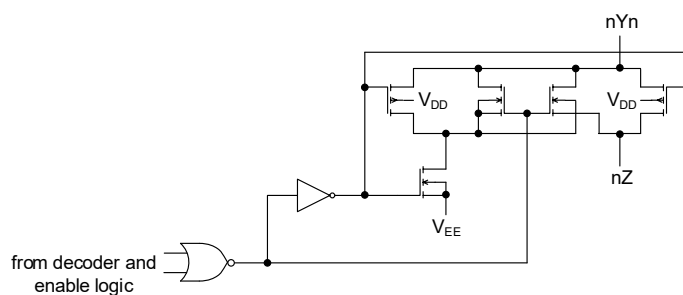


Figure 8-4 Schematic diagram (one switch)

8.3 Function Table⁽¹⁾

INPUT		CHANNEL ON
$\bar{E}$	S_n	
L	L	nY0 to nZ
L	H	nY1 to nZ
H	X	Switches off

(1) H=HIGH voltage level; L=LOW voltage level; X=don't care.

8.4 Testing Circuit

8.4.1 DC Testing Circuit

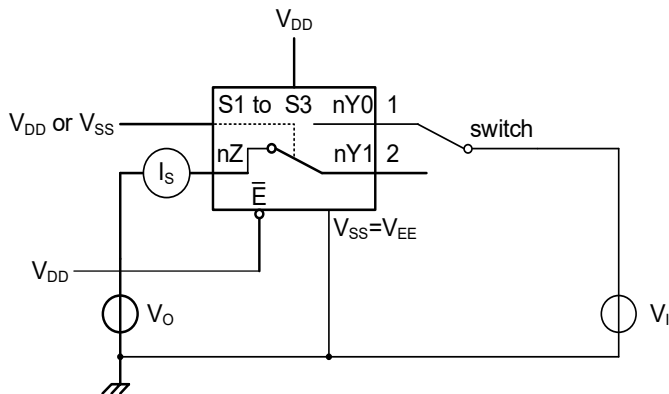


Figure 8-6 Test circuit for measuring OFF-state leakage current Z port

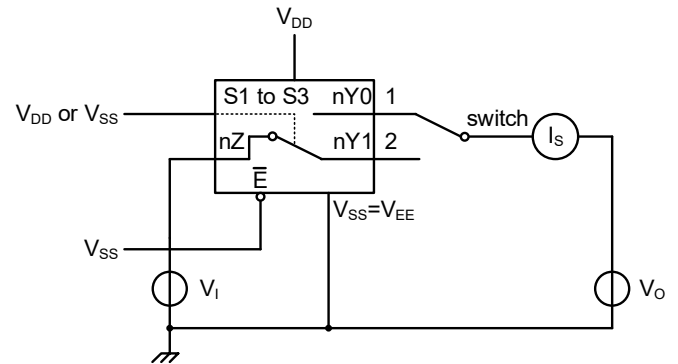


Figure 8-7 Test circuit for measuring OFF-state leakage current nYn port

8.4.2 ON Resistance Testing Circuit

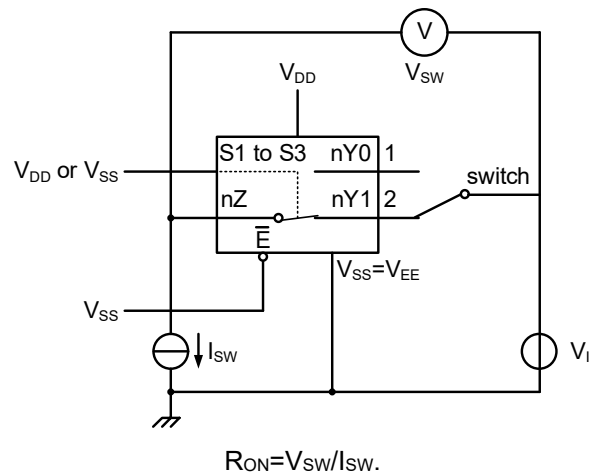


Figure 8-8 Test circuit for measuring R_{ON}

8.4.3 ON Resistance Waveforms

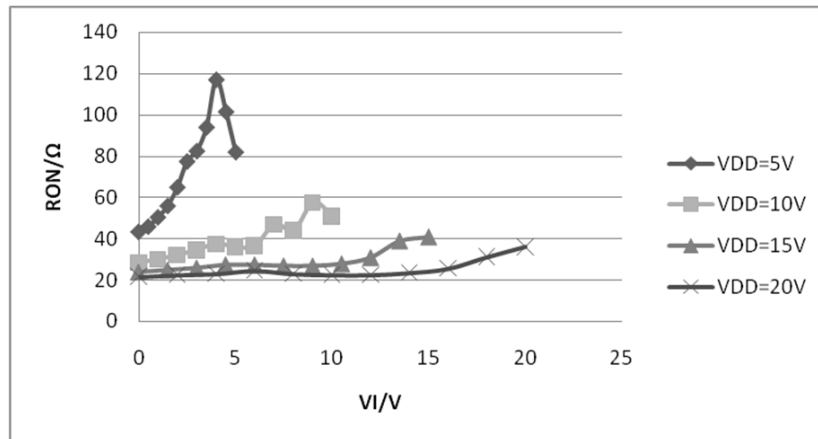


Figure 8-9 Typical R_{ON} as a function of input voltage

8.4.4 AC Testing Circuit 1

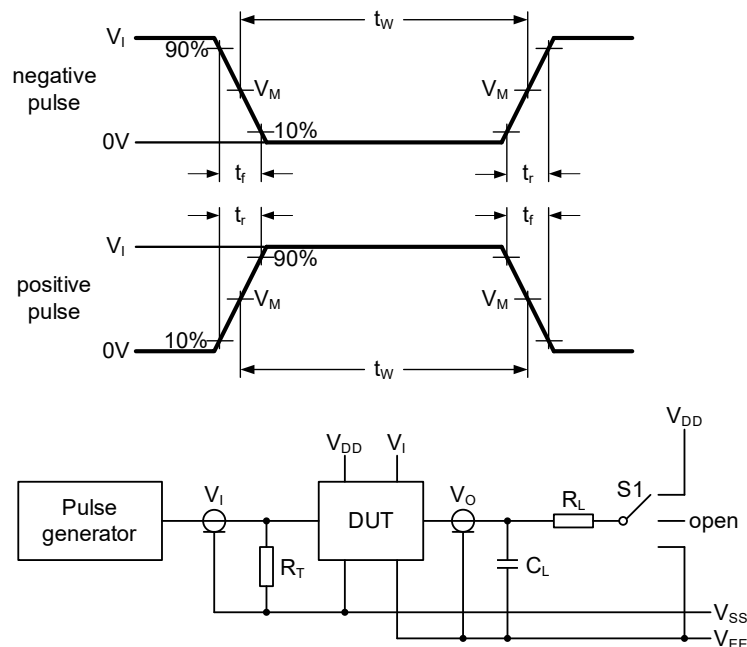


Figure 8-10 Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L =Load resistance.

8.4.5 AC Testing Waveforms

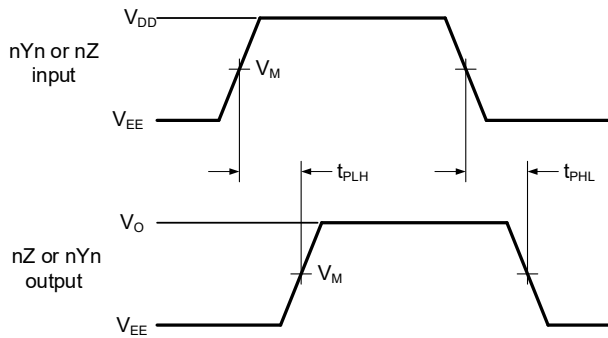


Figure 8-11 nYn, nZ to nZ, nYn propagation delays

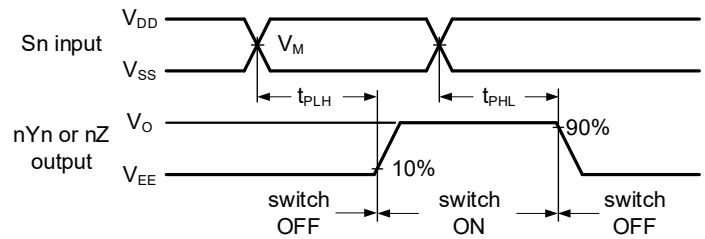


Figure 8-12 Sn to nYn, nZ propagation delays

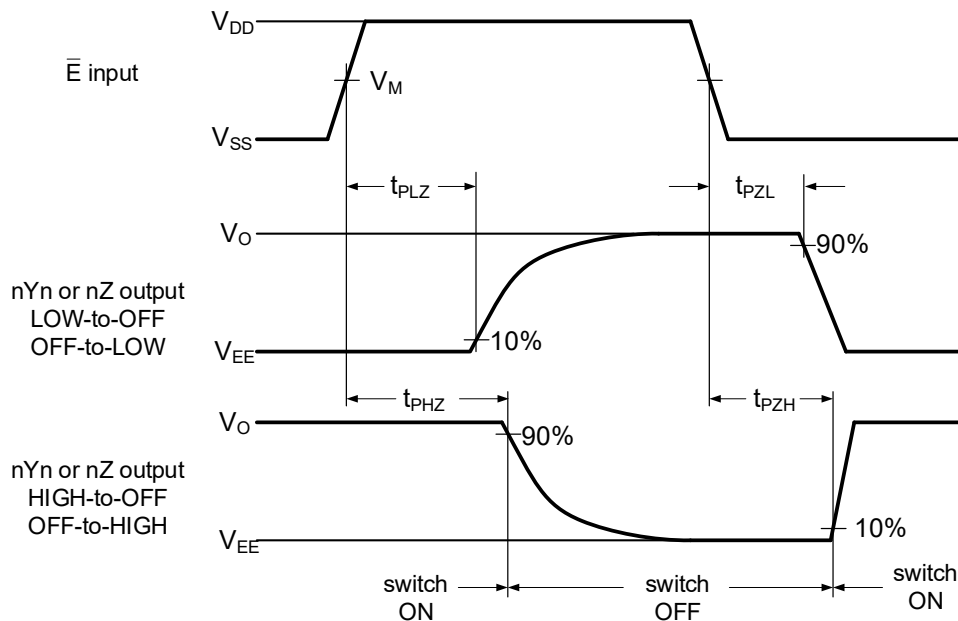


Figure 8-13 Enable and disable times

8.4.6 AC Testing Circuit 2

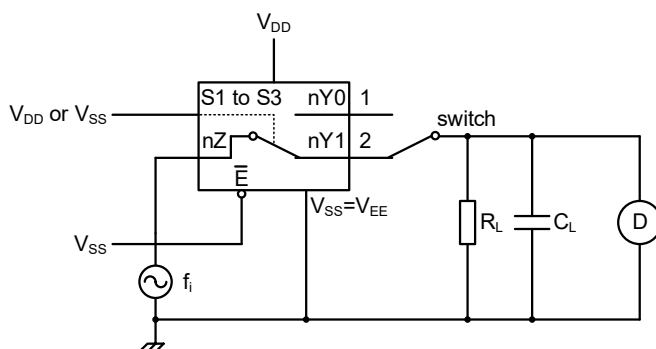


Figure 8-14 Test circuit for measuring total harmonic distortion

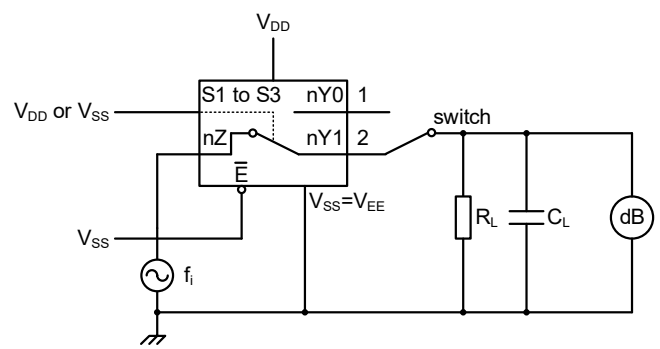


Figure 8-15 Test circuit for measuring frequency response

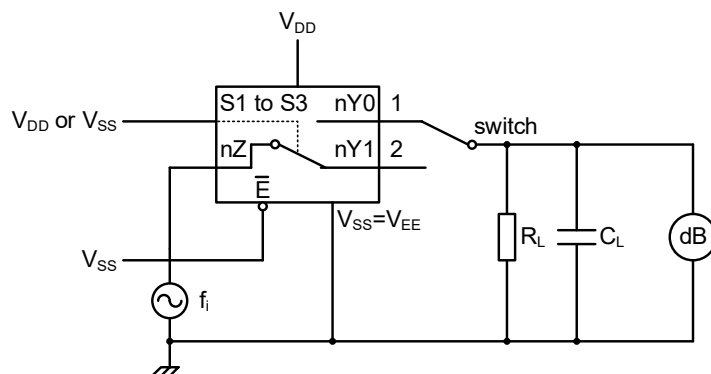
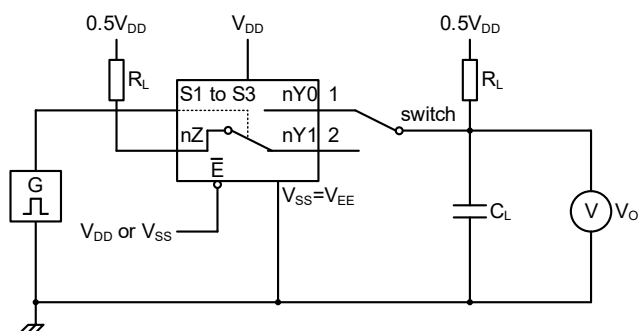
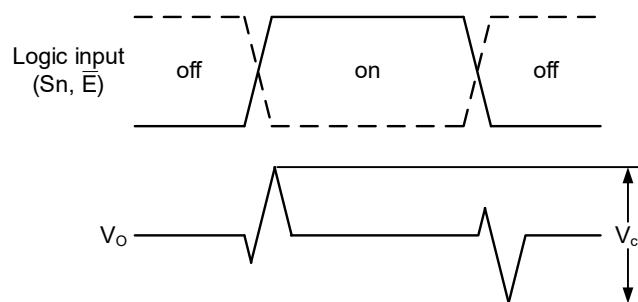


Figure 8-16 Test circuit for measuring isolation (OFF-state)

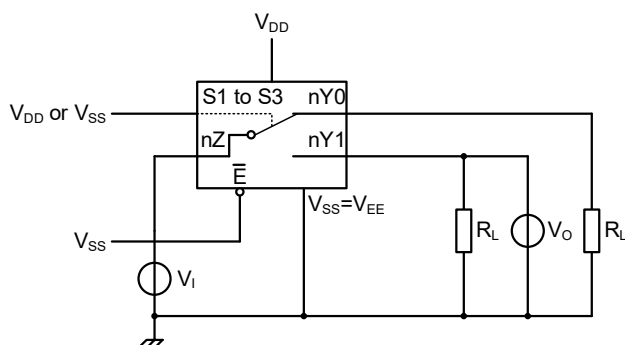


a. Test circuit

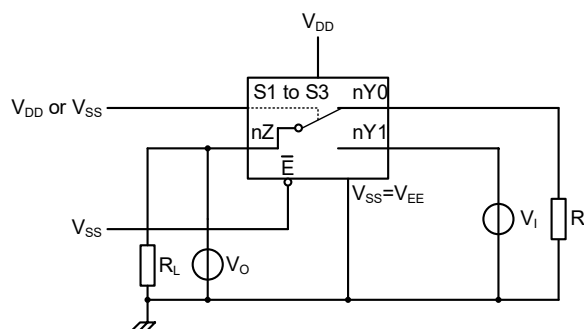


b. Input and output pulse definitions

Figure 8-17 Test circuit for measuring crosstalk voltage between digital inputs and switch



a. Switch closed condition



b. Switch open condition

Figure 8-18 Test circuit for measuring crosstalk between switches

8.4.7 Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{DD}	V_M	V_M
5V to 18V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

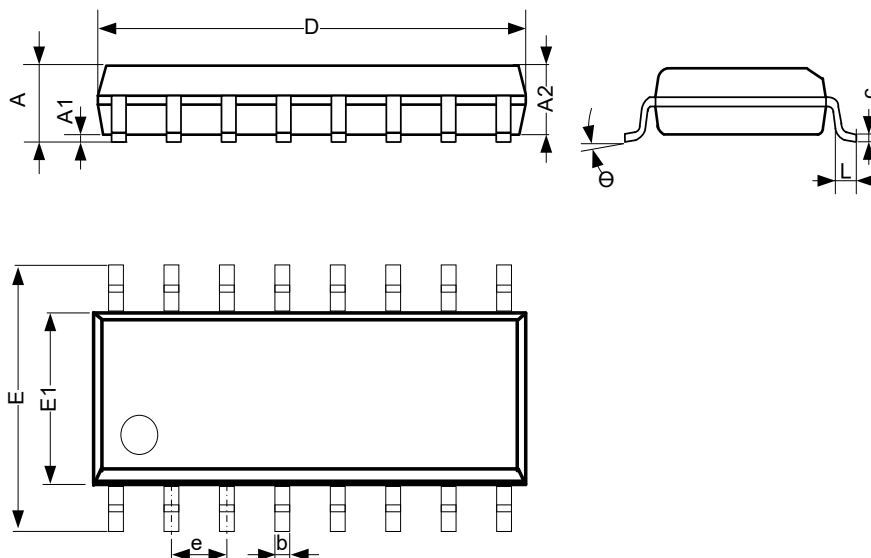
8.4.8 Test Data

INPUT				LOAD		S1 POSITION				
nYn, nZ	Sn and $\bar{E}$	t_r, t_f	V_M	C_L	R_L	t_{PHL}	t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}	Other
V_{DD} or V_{EE}	V_{DD} or V_{SS}	$\leq 20\text{ns}$	$0.5 \times V_{DD}$	50pF	10k Ω	V_{DD} or V_{EE}	V_{EE}	V_{EE}	V_{DD}	V_{EE}

9 Mechanical Information

9.1 SOP16 Mechanical Information

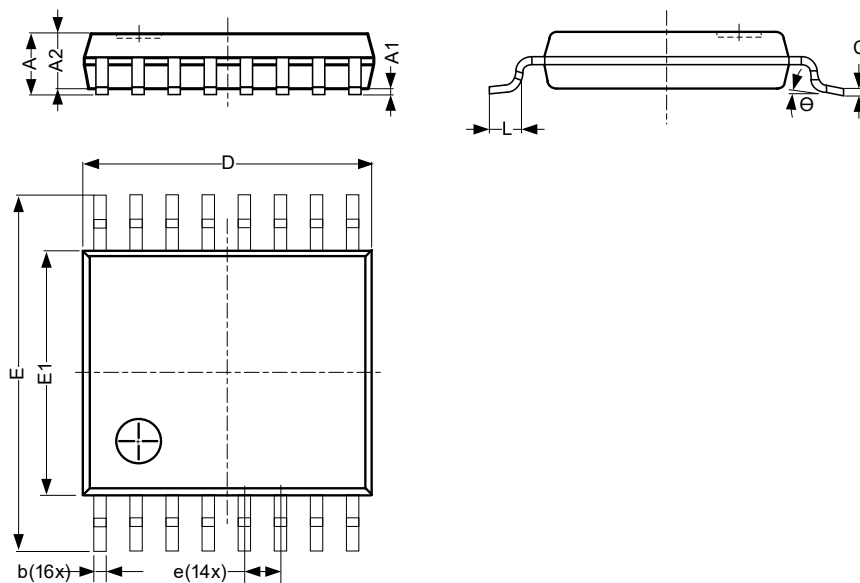
9.1.1 SOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.35	-	1.80
A1	0.10	-	0.25
A2	1.25	-	1.55
b	0.33	-	0.51
c	0.19	-	0.25
D	9.50	-	10.10
E	5.80	-	6.30
E1	3.70	-	4.10
e	1.27 BSC		
L	0.35	-	0.89
θ	0°	-	8°
Unit: mm			

9.2 TSSOP16 Mechanical Information

9.2.1 TSSOP16 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	-	5.10
E	6.20	-	6.60
E1	4.30	-	4.50
e	0.65 BSC		
L	0.45	-	0.75
θ	0°	-	8°
Unit: mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- <https://www.jscj-elec.com> for more details.

10.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

July, 2025: rev - 1.1, Change marking information.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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