## General Description

The SI8400AB-B-IS devices are low-power bidirectional isolators compatible with the I²C interface. These devices have logic input and output buffers that are separated by using a silicon dioxide ($SiO_2$) barrier. These devices block high voltages and prevent noise currents from entering the control side ground, avoiding circuit interference, and damaging sensitive components.

The SI8400AB-B-IS device is based on **iDivider®** technology with functional, performance, size, and power consumption advantages as compared to optocouplers.

The SI8400AB-B-IS provide two bidirectional channels, supporting a complete isolated I²C interface. The SI8400AB-B-IS is used in applications that have a single master. This device feature independent 3.0V supplies on each side of the isolator. These devices operate from DC to 2MHzat ambient temperatures of -40°C to +125°C.

## Features

Bidirectional I²C communication
Ultra-low power consumption
Supports up to 2MHz operation
Open-drain interfaces
  Side 1 outputs with 3.5mA sink current
  Side 2 outputs with 35mA sink current
3.0V to 5.5V supply/logic levels
High common-mode transient immunity: 120kV/μs
typical RoHS-compliant, SOP-8

## Applications

Isolated I²C, SMBus, PMBus
interfaces Multilevel I²C interfaces
Electric and Hybrid-Electric
Vehicles Open-Drain Networks
I²C Level Shifting
Power supplies

## Ordering Guide

Table 1. Ordering guide

| Model Name [1] | Temperature Range | Total signal channel amount | No. of Bi-directional channels | Isolation Rating (kV rms) | Package | MSL Peak Temp [2] | Quantity per reel |
|---|---|---|---|---|---|---|---|
| SI8400AB-B-IS | −40 ~125°C | 2 | 2 | 3 | SOP-8 | Level-2-260C-1 YEAR | 4000 |

1. Pai2xxxxx is equals to π2xxxxx in the customer BOM. Devices with Q suffix are AEC-Q100 qualified.
2. MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## Functional Block Diagrams

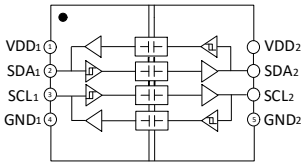
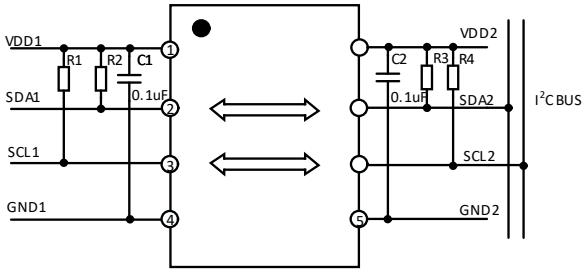



*Figure 1. Functional Block Diagram*



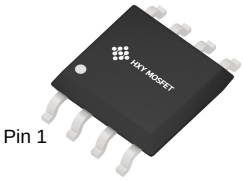




*Figure 2. Typical Application Circuit*

## Pin Configrations And Functions

Table 2. Pin Function Descriptions

| Pin No. | Name | Description |
|---|---|---|
| 1 | $V_{DD1}$ | Supply Voltage for Isolator Side 1. |
| 2 | $SDA_1$ | Serial data input / output, side 1. |
| 3 | $SCL_1$ | Serial clock input / output, side 1. |
| 4 | $GND_1$ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 5 | $GND_2$ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 6 | $SCL_2$ | Serial clock input / output, side 2. |
| 7 | $SDA_2$ | Serial data input / output, side 2. |
| 8 | $V_{DD2}$ | Supply Voltage for Isolator Side 2. |

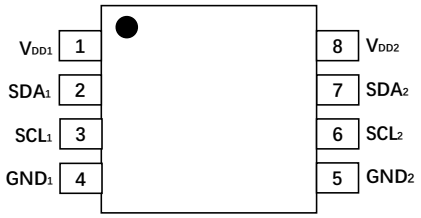



*Figure 3. P in Configuration*

## Absolute Maximum Ratings

$T_A$ = 25°C, unless otherwise noted.

Table 3.Absolute Maximum Ratings[4]

| Parameter | Rating |
|---|---|
| Supply Voltages ($V_{DD1}$-$GND_1$, $V_{DD2}$-$GND_2$) | −0.5 V to +7.0 V |
| Signal Voltage SDA1/SCL1 | −0.5 V to $V_{DDx}$ + 0.5 V |
| Signal Voltage SDA2/SCL2 | −0.5 V to $V_{DDx}$ + 0.5 V |
| Average Output Current SDA1/SCL1 ($I_{O1}$) | −20 mA to +20 mA |
| Average Output Current SDA2/SCL2 ($I_{O2}$) | −100 mA to +100 mA |
| Storage Temperature ($T_{ST}$) Range | −65°C to +150°C |
| Maximum junction temperature $T_{J(MAX)}$ | +150°C |

Notes:

1. All voltage values here within are with respect to the local ground pin (GND1 or GND2) and are peak voltage values.
2. Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## Recommended Operating Conditions

Table 4. Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DDx}$ [1] | 3 | | 5.5 | V |
| Input/Output Signal Voltage ($V_{SDA1}$, $V_{SCL1}$, $V_{SDA2}$, $V_{SCL2}$) | | 0 | | $V_{DDx}$[1] | V |
| Low-level input voltage, side 1 | $V_{IL1}$ | 0 | | 0.47 | V |
| High-level input voltage, side 1 | $V_{IH1}$ | 0.7*$V_{DD1}$ | | $V_{DD1}$ | V |
| Low-level input voltage, side 2 | $V_{IL2}$ | 0 | | 0.3*$V_{DD2}$ | V |
| High-level input voltage, side 2 | $V_{IH2}$ | 0.7*$V_{DD2}$ | | $V_{DD2}$ | V |
| Output current, side 1 | $I_{OL1}$ | 0.5 | | 3.5 | mA |
| Output current, side 2 | $I_{OL2}$ | 0.5 | | 35 | mA |
| Capacitive load, side 1 | C1 | | | 40 | pF |
| Capacitive load, side 2 | C2 | | | 400 | pF |
| Operating frequency | $f_{MAX}$ | | | 2 | MHz |
| Ambient Operating Temperature | $T_A$ | -40 | | 125 | °C |

Notes:

[1] $V_{DDx}$ is the side voltage power supply $V_{DD}$, where x = 1 or 2.

## Truth Tables

Table 5. Truth Table

| $V_{Ix}$ Input[1] | $V_{DDI}$ State[1] | $V_{DDO}$ State[1] | $V_{Ox}$ Output[1] |
|---|---|---|---|
| Low | Powered[2] | Powered[2] | Low |
| High | Powered[2] | Powered[2] | High Impedance |
| Open[4] | Powered[2] | Powered[2] | High Impedance |
| Don't Care | Unpowered[3] | Powered[2] | High Impedance |
| Don't Care | Powered[2] | Unpowered[3] | High Impedance |

Notes:

[1] $V_{Ix}/V_{Ox}$ are the input/output signals of a given channel (SDA or SCL). $V_{DDI}/V_{DDO}$ are the supply voltages on the input/output signal sides of this given channel. [2] Powered means $V_{DDx} \geq 2.95V$

[3] Unpowered means $V_{DDx} < 2.30V$

[4] Invalid input condition as an I²C system requires that a pullup resistor to $V_{DD}$ is connected.

## Specifications

### Electrical Characteristics

Table 6. DC Specifications

$V_{DD1}$ - $V_{GND1}$ = $V_{DD2}$ - $V_{GND2}$ =3.0V ~ 5.5V, typical value is measured at $T_A$=25°C, unless otherwise noted.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| **Side 1 Logic Levels** | | | | | | |
| Voltage input threshold low, $SDA_1$ and $SCL_1$ | $V_{ILT1}$ | 470 | 510 | 570 | mV | |
| Voltage input threshold high, $SDA_1$ and $SCL_1$ | $V_{IHT1}$ | 540 | 580 | 630 | mV | |
| Voltage input hysteresis | $V_{HYST1}$ | 30 | 70 | | mV | $V_{IHT1} - V_{ILT1}$ |
| Low-level output voltage, SDA1 and SCL1 | $V_{OL1}$ | 650 | 720 | 800 | mV | 0.5 mA ≤ ($I_{SDA1}$ and $I_{SCL1}$) ≤ 3.5 mA |
| Low-level output voltage to high-level input voltage threshold difference, SDA1 and SCL1 | $\Delta V_{OIT1}$[1] | 60 | 120 | | mV | 0.5 mA ≤ ($I_{SDA1}$ and $I_{SCL1}$) ≤ 3.5 mA |
| **Side 2 Logic Levels** | | | | | | |
| Voltage input threshold low, SDA2 and SCL2 | $V_{ILT2}$ | 0.30* $V_{DD2}$ | | 0.42*$V_{DD2}$ | V | |
| Voltage input threshold high, SDA2 and SCL2 | $V_{IHT2}$ | 0.58* $V_{DD2}$ | | 0.69*$V_{DD2}$ | V | |
| Voltage input hysteresis | $V_{HYST2}$ | 0.15* $V_{DD2}$ | 0.28* $V_{DD2}$ | | V | $V_{IHT2} - V_{ILT2}$ |
| Low-level output voltage, SDA2 and SCL2 | $V_{OL2}$ | | | 0.4 | V | 0.5 mA ≤ ($I_{SDA2}$ and $I_{SCL2}$) ≤ 35 mA |
| **Both Sides** | | | | | | |
| Input leakage currents, SDA1, SCL1, SDA2, and SCL2 | $\|I_{IN}\|$ | | 0.01 | 10 | µA | $V_{SDA1}$, $V_{SCL1}$ = $V_{DD1}$; $V_{SDA2}$, $V_{SCL2}$ = $V_{DD2}$ |
| $V_{DDx}$[3]Undervoltage Rising Threshold | $V_{DDxUV+}$ | 2.45 | 2.75 | 2.95 | V | |
| $V_{DDx}$[3]Undervoltage Falling Threshold | $V_{DDxUV-}$ | 2.30 | 2.60 | 2.80 | V | |
| $V_{DDx}$[3]Hysteresis | $V_{DDxUVH}$ | | 0.15 | | V | |

Notes:

1. $\Delta V_{OIT1} = V_{OL1} - V_{IHT1}$. This is the minimum difference between the output logic low level and the input logic threshold within a given component. This ensures that there is no possibility of the part latching up the bus to which it is connected.
2. $V_{DDx}$ is the side voltage power supply VDD, where x = 1 or 2.

Table 7. Quiescent Supply Current

$V_{DD1}$ - $V_{GND1}$ = $V_{DD2}$ - $V_{GND2}$ =3.0V ~ 5.5V, typical value is measured at $T_A$=25°C, unless otherwise noted.

| Part | Symbol | Min | Typ | Max | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|
| | | | | | | Supply voltage | Input signal |
| SI8400AB-B-IS | $I_{DD1 (Q)}$ | | 1.7 | 2.4 | mA | $5V_{DC}$ | All IO = $0V_{DC}$ |
| | $I_{DD2 (Q)}$ | | 1.4 | 2.1 | mA | | |
| | $I_{DD1 (Q)}$ | | 1.5 | 2.3 | mA | | All IO = $5V_{DC}$ |
| | $I_{DD2 (Q)}$ | | 1.2 | 1.8 | mA | | |
| | $I_{DD1 (Q)}$ | | 1.5 | 2.3 | mA | $3.3V_{DC}$ | All IO = $0V_{DC}$ |
| | $I_{DD2 (Q)}$ | | 1.2 | 1.8 | mA | | |
| | $I_{DD1 (Q)}$ | | 1.5 | 2.3 | mA | | All IO = $3.3V_{DC}$ |
| | $I_{DD2 (Q)}$ | | 1.2 | 1.8 | mA | | |

Table 8. Switching Specifications

$V_{DD1}$ - $V_{GND1}$ = $V_{DD2}$ - $V_{GND2}$ =3.0V ~ 5.5V, typical value is measured at $T_A$=25°C, unless otherwise noted.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| Output Signal Fall Time SDA1, SCL1 | $t_{f1}$ | 10 | 18 | 32 | ns | 0.9 × $V_{DD1}$ to 0.9V; R1 = 1500Ω, C1 = 40pF, @ $5V_{DC}$ supply |
| | | 8 | 16 | 30 | ns | R1 = 1000Ω, C1 = 40pF; @ $3.3V_{DC}$ supply |
| Output Signal Fall Time SDA2, SCL2 | $t_{f2}$ | 20 | 36 | 60 | ns | 0.9 × $V_{DD2}$ to 0.4V; R2 = 150Ω, C2 = 400pF, @ $5V_{DC}$ supply |
| | | 18 | 31 | 57 | ns | R2 = 100Ω, C2 = 400pF; @ $3.3V_{DC}$ supply |
| Low-to-High Propagation Delay, Side 1 to Side 2 | $t_{pLH1-2}$ | | 45 | 68 | ns | 0.55V to 0.7 × $V_{DD2}$; R1 = 1500Ω, R2 = 150Ω, C1, C2 = 10 pF; @ $5V_{DC}$ supply |
| | | | 38 | 63 | ns | R1 = 1000Ω, R2 = 100Ω, C1, C2 = 10pF; @ $3.3V_{DC}$ supply |
| High-to-Low Propagation Delay, Side 1 to Side 2 | $t_{PHL1-2}$ | | 67 | 130 | ns | 0.7V to 0.4V; R1 = 1500Ω, R2 = 150Ω, C1, C2 = 10pF; @ $5V_{DC}$ supply |
| | | | 64 | 130 | ns | R1 = 1000Ω, R2 = 100Ω, C1, C2 = 10pF; @ $3.3V_{DC}$ supply |
| Pulse Width Distortion $\lvert t_{pHL1-2} - t_{pLH1-2} \rvert$ | $PWD_{1-2}$ | | 22 | 60 | ns | R1 = 1500Ω, R2 = 150Ω, C1, C2 = 10pF; @ $5V_{DC}$ supply |
| | | | 26 | 65 | ns | R1 = 1000Ω, R2 = 100Ω, C1, C2 = 10pF; @ $3.3V_{DC}$ supply |
| Low-to-High Propagation Delay, Side 2 to Side 1 | $t_{PLH2-1}$ | | 62 | 80 | ns | 0.4 × $V_{DD2}$ to 0.7 × VDD1; R1 = 1500Ω, R2 = 150Ω, C1, C2 = 10pF; @ $5V_{DC}$ supply |
| | | | 50 | 70 | ns | R1 = 1000Ω, R2 = 100Ω, C1, C2 = 10pF; @ $3.3V_{DC}$ supply |
| High-to-Low Propagation Delay, Side 2 to Side 1 | $t_{PHL2-1}$ | | 54 | 84 | ns | 0.4 × $V_{DD2}$ to 0.9V; R1 = 1500Ω, R2 = 150Ω, C1, C2 = 10pF; @ $5V_{DC}$ supply |
| | | | 56 | 86 | ns | R1 = 1000Ω, R2 = 100Ω, C1, C2 = 10pF; @ $3.3V_{DC}$ supply |
| Pulse Width Distortion $\lvert t_{pHL2-1} - t_{pLH2-1} \rvert$ | $PWD_{2-1}$ | | 12 | 25 | ns | R1 = 1500Ω, R2 = 150Ω, C1,2 = 10 pF; @ $5V_{DC}$ supply |
| | | | 15 | 35 | ns | R1 = 1000Ω, R2 = 100Ω, C1, C2 = 10 pF; @ $3.3V_{DC}$ supply |
| Round-trip propagation delay on Side 1 | $t_{LOOP1}$ | | 116 | 180 | ns | 0.4 V to 0.3 × $V_{DD1}$; R1 = 1500Ω, R2 = 150Ω, C1, C2 = 10 pF; @ $5V_{DC}$ supply |
| | | | 98 | 162 | ns | R1 = 1000Ω, R2 = 100Ω, C1, C2 = 10 pF; @ $3.3V_{DC}$ supply |
| Common-Mode Transient Immunity[2] | CMTI | | 120 | | kV/μs | $V_{IN}$ = $V_{DDx}$[1] or 0V, $V_{CM}$ = 1000 V. |
| ESD（HBM - Human body model） | ESD | | ±6 | | kV | |

## Insulation And Safety Related Specifications

Table 9. Insulation Specifications

| Parameter | Symbol | Value | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| Rated Dielectric Insulation Voltage | $V_{ISO}$ | 3000 | $V_{RMS}$ | 1-minute duration, certificated |
| Minimum External Air Gap (Clearance) | CLR | ≥4.0 | mm | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | CRP | ≥4.0 | mm | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | DTI | ≥21 | μm | Insulation distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | ≥400 | V | DIN EN 60112 (VDE 0303-11):2010-05 |
| Material Group | | II | | IEC 60112:2003 + A1:2009 |

## Package Characteristics

Table 10.Package Characteristics

| Parameter | Symbol | Value | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| Resistance (Input to Output)[1] | $R_{I-O}$ | $\geq 10^{12}$ | Ω | $V_{IO}$=500V, $T_A$ = 25°C |
| Resistance (Input to Output)[1] | $R_{I-O}$ | $\geq 10^{11}$ | Ω | $V_{IO}$=500V, $T_A$ = 125°C |
| Resistance (Input to Output)[1] | $R_{I-O}$ | $\geq 10^{9}$ | Ω | $V_{IO}$=500V, $T_A$ = 150℃ |
| Capacitance (Input to Output)[1] | $C_{I-O}$ | 1.5 | pF | @300kHz |
| Input Capacitance[2] | $C_I$ | 3 | pF | @1MHz, ensured by design |
| IC Junction to Ambient Thermal Resistance | $\theta_{JA}$ | 100 | °C/W | |

Notes:

1. The device is considered a 2-terminal device. Short-circuit all terminals on the $VDD_1$ side as one terminal and short-circuit all terminals on the $VDD_2$ side as the other terminal.
2. Testing from the input signal pin to ground.

## DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 Insulation Characteristics

Table 11.VDE Insulation Characteristics

| Description | Test Conditions/ Comments | Symbol | Characteristic | Unit |
|---|---|---|---|---|
| Installation Classification per DIN VDE 0110 | | | | |
| For Rated Mains Voltage ≤ 150 $V_{RMS}$ | | | I to IV | |
| For Rated Mains Voltage ≤ 300 $V_{RMS}$ | | | I to III | |
| For Rated Mains Voltage ≤ 400 $V_{RMS}$ | | | I to III | |
| Climatic Classification | | | 40/125/21 | |
| Pollution Degree per DIN VDE 0110, Table 1 | | | 2 | |
| Maximum repetitive peak isolation voltage | Time dependent dielectric breakdown test | $V_{IORM}$ | 707 | $V_{peak}$ |
| Maximum isolation working voltage | AC voltage (sine wave) | $V_{IOWM}$ | 500 | $V_{RMS}$ |
| | DC Voltage | | 707 | $V_{peak}$ |
| Input to Output Test Voltage, Method B1 | | | | |
| 100% production test, no pre-condition tests | $V_{IORM}$ × 1.5 = $V_{pd\ (m)}$, $t_{ini}$ = $t_m$ = 1 sec, partial discharge < 5pC | $V_{pd\ (m)}$ | 1061 | $V_{peak}$ |
| Input to Output Test Voltage, Method A | | | | |
| After Environmental Tests Subgroup 1 | $V_{IORM}$ × 1.3 = $V_{pd\ (m)}$, $t_{ini}$ = 60 sec, $t_m$ = 10 sec, partial discharge < 5pC | $V_{pd\ (m)}$ | 919 | $V_{peak}$ |
| After Input and/or Safety Test Subgroup 2 and Subgroup 3 | $V_{IORM}$ × 1.2 = $V_{pd\ (m)}$, $t_{ini}$ = 60 sec, $t_m$ = 10 sec, partial discharge < 5pC | $V_{pd\ (m)}$ | 848 | $V_{peak}$ |
| Highest Allowable Overvoltage | $V_{TEST}$ = $V_{IOTM}$ t = 60s (qualification); $V_{TEST}$ =1.2 × $V_{IOTM}$ t= 1s (100% production) | $V_{IOTM}$ | 4200 | $V_{peak}$ |
| Maximum Surge Isolation Voltage | Basic insulation, 1.2/50 µs combination wave, $V_{TEST}$ = 1.3 × $V_{IOSM}$ (qualification)[1] | $V_{IOSM}$ | 5000 | $V_{peak}$ |
| Safety Limiting Values | Maximum value allowed in the event of a failure (see Figure 4) | | | |
| Maximum Safety Temperature | | $T_S$ | 150 | ℃ |
| Maximum Power Dissipation at 25°C | | $P_S$ | 1.25 | W |
| Insulation Resistance | $V_{IO}$ = 500V, $T_A$= 25°C | $R_{I-O}$ | $\geq 10^{12}$ | Ω |
| Insulation Resistance | $V_{IO}$ = 500V, 100°C ≤ $T_A$ ≤ 125°C | $R_{I-O}$ | $\geq 10^{11}$ | Ω |
| Insulation Resistance at $T_S$ | $V_{IO}$ = 500V, $T_S$ = 150℃ | $R_{I-O}$ | $\geq 10^{9}$ | Ω |

Notes:

[1]In accordance with DIN V VDE V 0884-17, SI8400AB-B-IS is proof tested by applying a surge isolation voltage of 6500V.

## Typical Thermal Characteristics

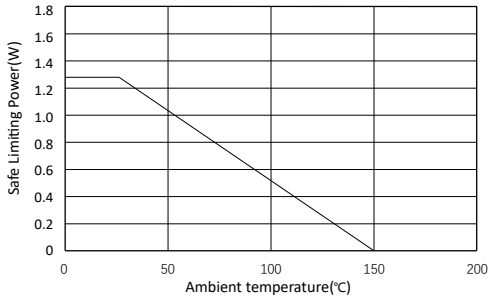



*Figure 4.Thermal Derating Curve, Dependence Of Safety Limiting Values with Ambient Temperature per VDE*

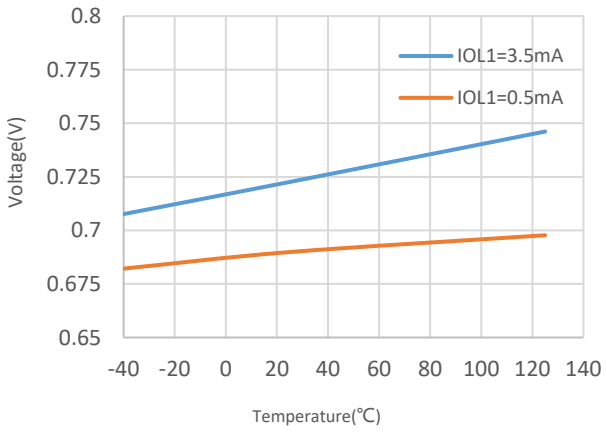



*Figure 5. Side 1: Output Low Voltage vs Free-Air Temperature*

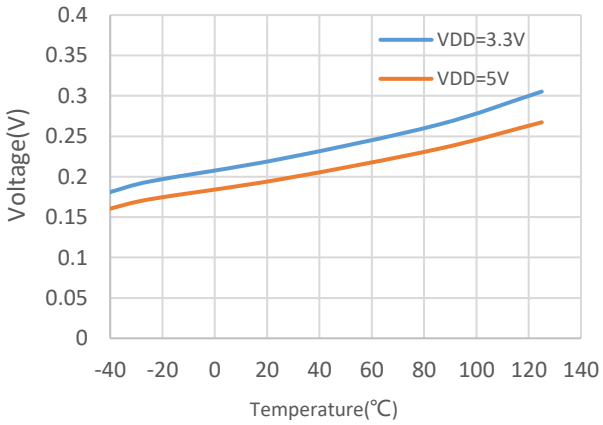



*Figure 6. Side 2: Output Low Voltage vs Free-Air Temperature, Sink 35mA*

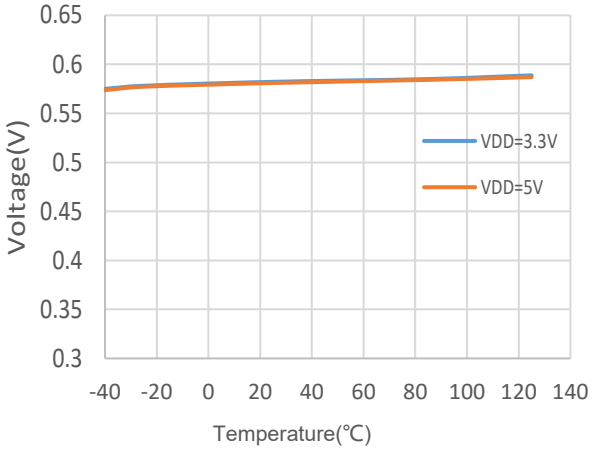



*Figure 7. Side 1: Input Threshold High vs Free-Air Temperature*

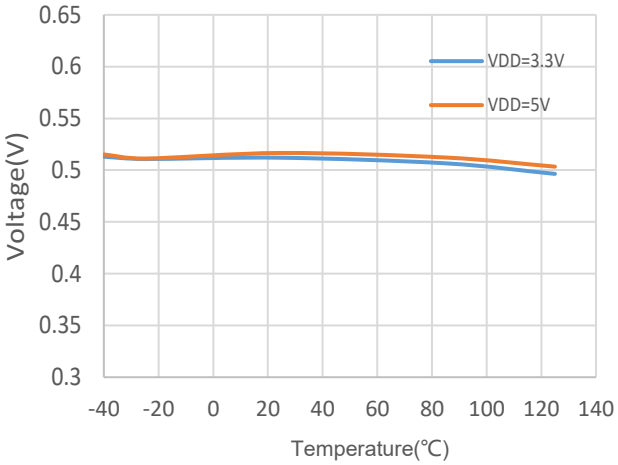



*Figure 8. Side 1: Input Threshold Low vs Free-Air Temperature*

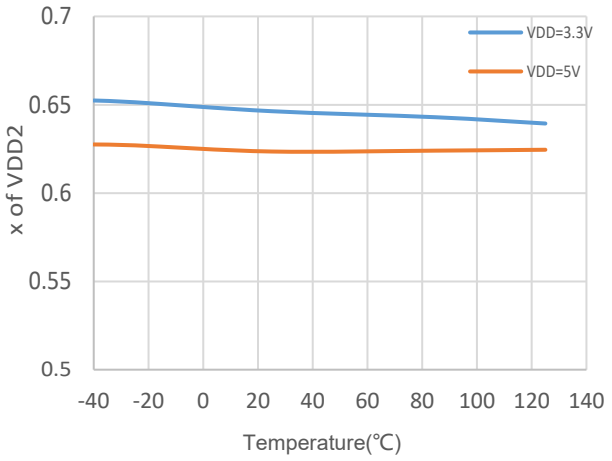



*Figure 9 . Side 2: Input Threshold High vs Free-Air Temperature*

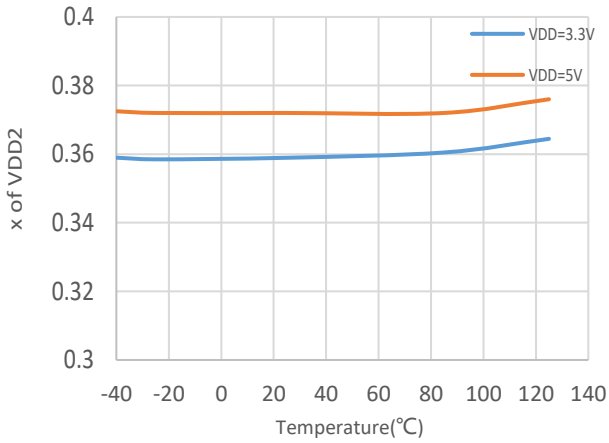



*Figure 10. Side 2: Input Threshold Low vs Free-Air Temperature*

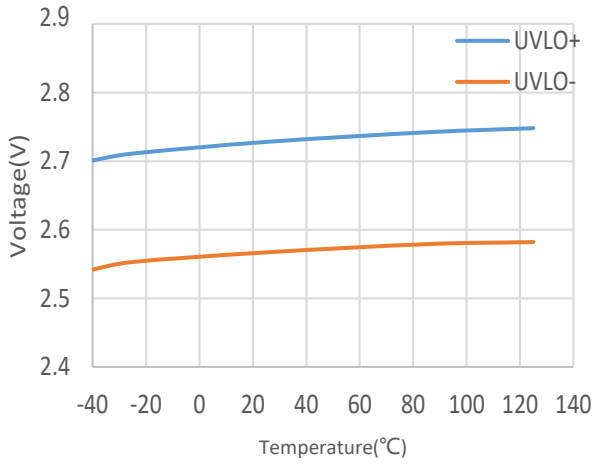



*Figure 11 UVLO vs Free-Air Temperature*

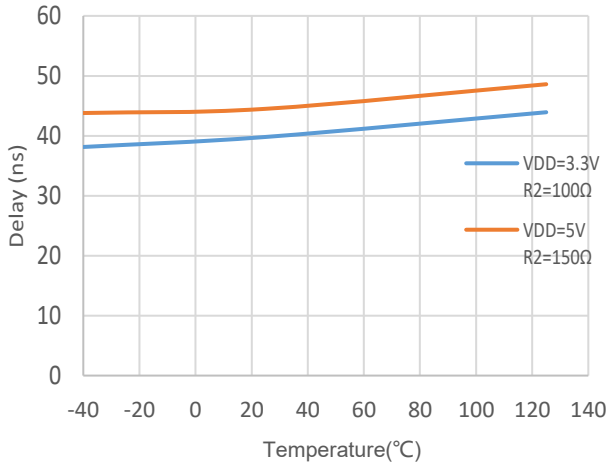



*Figure 12. $t_{PLH1-2}$ Propagation Delay vs Free-Air Temperature*

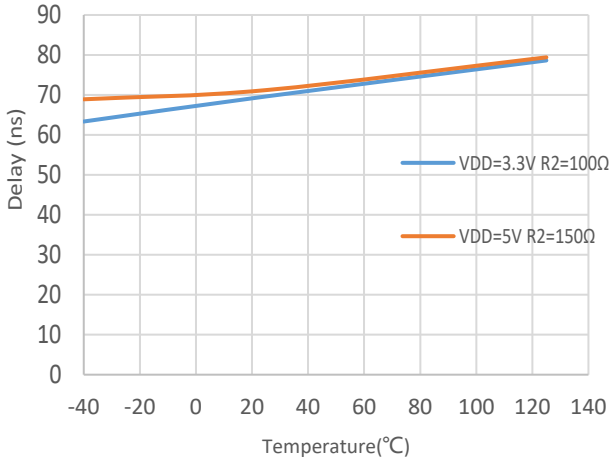



*Figure 13. $t_{PHL1-2}$ Propagation Delay vs Free-Air Temperature*

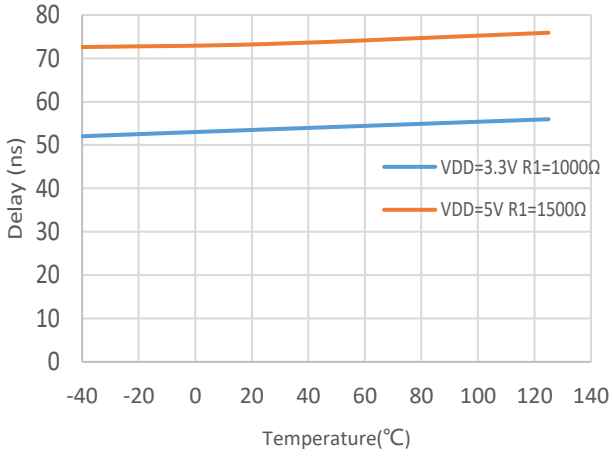



*Figure 14. $t_{PLH2-1}$ Propagation Delay vs Free-Air Temperature*

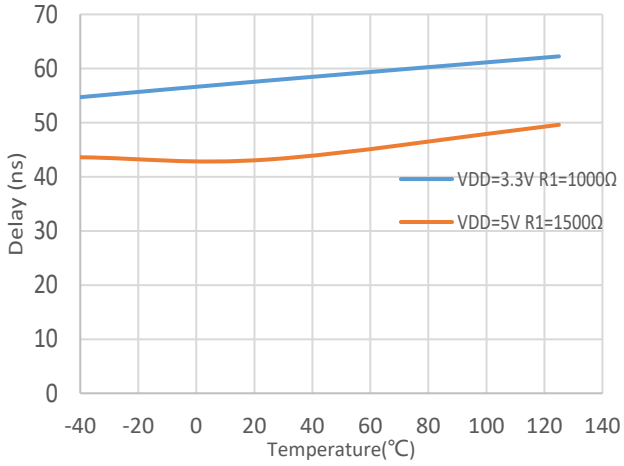



*Figure 15. $t_{PHL2-1}$ Propagation Delay vs Free-Air Temperature*

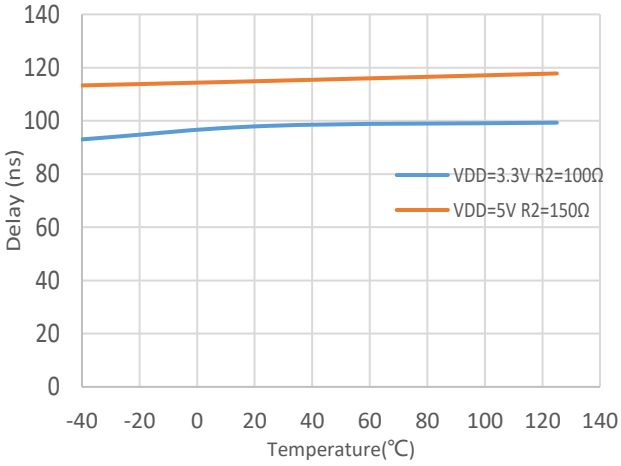



*Figure 16. $t_{LOOP1}$ vs Free-Air Temperature*

## Timing Test Information

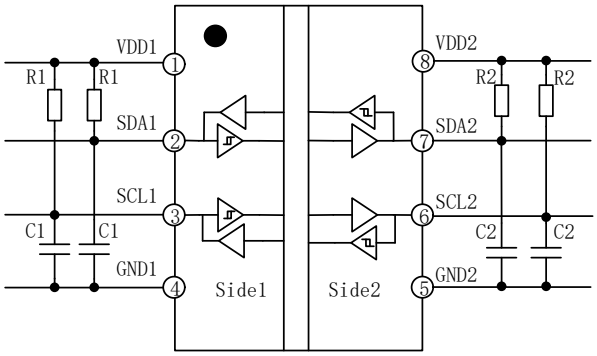



*Figure 17. Test Diagram*

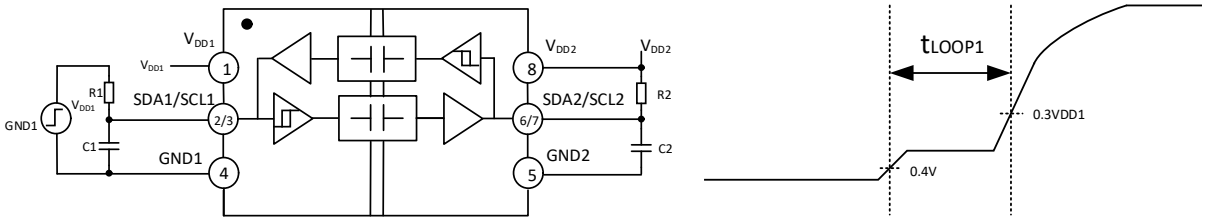



*Figure 18. $t_{Loop1}$ Setup and Timing Diagram*

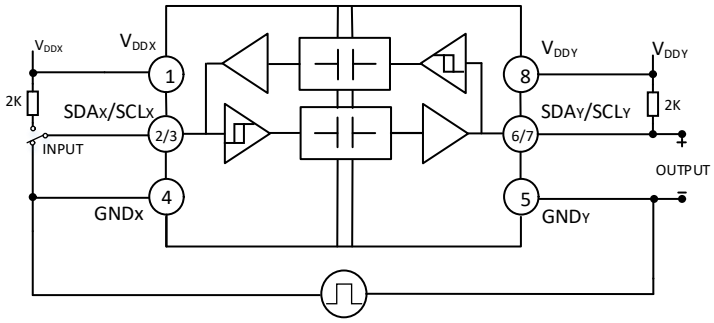



*Figure 19. Common-Mode Transient Immunity Test Circuit*

# Applications Information

## Overview

The inter-integrated circuit (I²C) bus is a single-ended, two wire bus for efficient inter-IC communication and is used in a wide range of applications. The I²C bus is used for communication between multiple masters or a single master and slaves. The master device controls the serial clock line (SCL), and data is bidirectional transferred on the serial data line (SDA) between master and slaves. The I²C bus can theoretically add up to 112 communication nodes, however, the number of nodes will increase the load capacitance on the bus, thereby limiting the communication distances and communication speeds. In applications, tradeoffs are often made between communication speeds, bus length, and number of nodes based on actual conditions.

The I²C bus supports data transmission in four speeds: standard mode (up to 100Kbps), fast mode (up to 400Kbps), fast mode plus (up to 1Mbps), and high-speed mode (up to 3.4Mbps). The SI8400AB-B-IS device support all the above four communication modes.

## Functional Description

The SI8400AB-B-IS device is low-power bidirectional isolators compatible with the I²C interface.

This device have logic input and output buffers that are separated by using a silicon dioxide ($SiO_2$) barrier. This device block high voltages and prevent noise currents from entering the control side ground, avoiding circuit interference, and damaging sensitive components.

Each channel output of the SI8400AB-B-IS device is made open-drain to comply with the open-drain technology of I²C. Serial data line (SDA)and serial clock line (SCL) need to add pull-up resistors to ensure normal operation of the system. It is recommended that side 1 of the I²C isolator be connected to the processor and sides 2 to the bus when there are multiple nodes on the I2C bus as side 2 support up to 400pF capacitance load.

The SI8400AB-B-ISdevice feature two bidirectional channels that have open-drain outputs, As shown in Figure 20. As a logic low on one side causes the corresponding pin on the other side to be pulled low, to avoid data-latching within the device, The output logic low ($V_{OL1}$) voltages of $SDA_1$ and $SCL_1$ are at least 60mV higher than the input threshold high ($V_{IHT1}$) of $SDA_1$ and $SCL_1$, As shown in Figure 21.

Because the Side 2 logic levels/thresholds are standard I²C values, multiple SI8400AB-B-IS devices connected to a bus by their Side 2 pins can communicate with each other and with other I2C compatible devices. However, because the Side 1 pin has a modified output level/ input threshold, this side of the SI8400AB-B-IS can communicate only with devices that conform to the I2C standard.

The output low voltages of SI8400AB-B-IS device is guaranteed for sink currents of up to 35mA for side 2, and 3. 5mA
for side 1.

To enhance system reliability, it is recommended to connect the node with larger load capacitance and longer wires on side 2 for point-to-point communication.

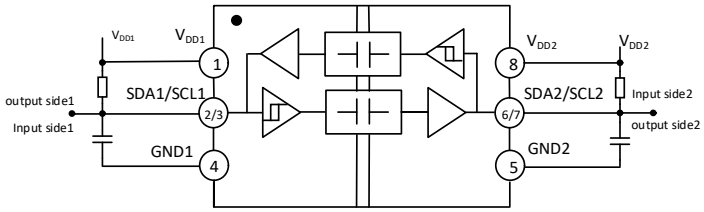



*Figure 20. system operation diagram*

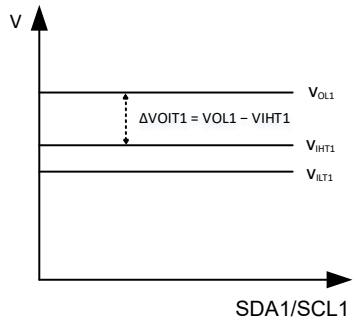



*Figure 21. side 1 voltage Diagram*

## Typical Application Diagram

Figure 22 shows a typical application circuit including the pull-up resistors required for both Side 1 and Side 2. Bypass capacitors with values from 0.1μF to 10μF are required between VDD1 and GND1 and between VDD2 and GND2. To enhance the robustness of a design, the user may connect a resistor (50-200Ω) in series between R2 and C1 and between R3 and C2 if the system is excessively noisy.

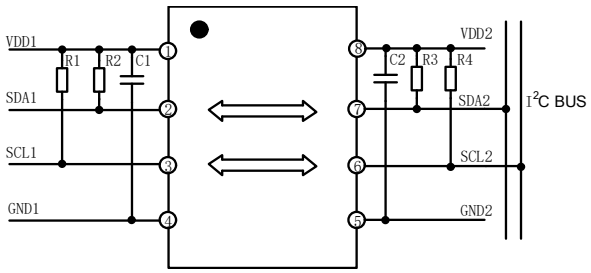



*Figure 22. Typical Isolated I²C Interface Using the* SI8400AB-B-IS

## Outline Dimensions

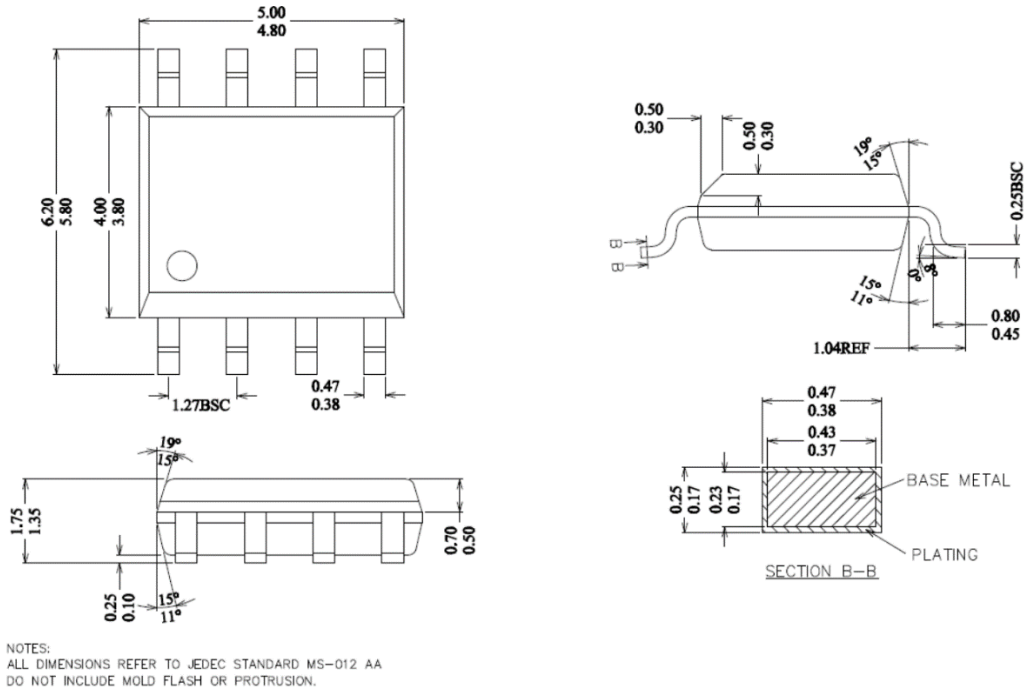



*Figure 23. 8-Lead SOP Outline Package–dimension unit(mm)*

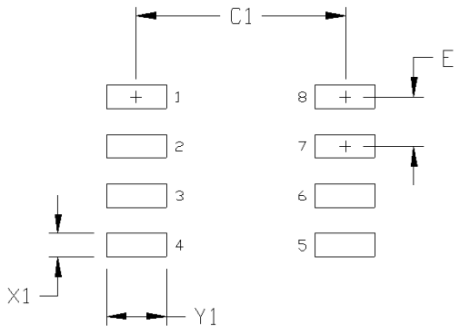



*Figure 24.*8-Lead SOP Land Pattern

Table 12.8-Lead SOP Land Pattern Dimensions

| Dimension | Feature | Parameter | Unit |
|---|---|---|---|
| C1 | Pad column spacing | 5.40 | mm |
| E | Pad row pitch | 1.27 | mm |
| X1 | Pad width | 0.60 | mm |
| Y1 | Pad length | 1.55 | mm |

Note：

1.This land pattern design is based on IPC -7351.

2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

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