2MHz, Super Chopper-Stabilized Operational Amplifier

Features

- Guaranteed Max Input Offset Voltage for All Temperature Ranges
- Low Long-Term and Temperature Drifts of Input Offset Voltage
- Guaranteed Max Input Bias Current :10pA
- Extremely Wide Common Mode Voltage Range : +3.5V to -5V
- Reduced Supply Current : 2mA
- Guaranteed Minimum Output Source/Sink Current
- Extremely High Gain :150dB
- Extremely High CMRR and PSRR :140dB
- High Slew Rate :2.5V/μs
- Wide Bandwidth :2MHz
- Unity-Gain Compensated
- Clamp Circuit to Avoid Overload Recovery Problems and Allow Comparator Use
- Extremely Low Chopping Spikes at Input and Output
- Pb-Free Plus Anneal Available (RoHS Compliant)

DIP-14

DIP-8

SOP-8

Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
ICL7650N	DIP-8	ICL7650	TUBE	2000 pcs/box
ICL7650M/TR	SOP-8	ICL7650	REEL	2500 pcs/reel
ICL7650N-14	DIP-14	ICL7650-14	TUBE	1000 pcs/box

General Description

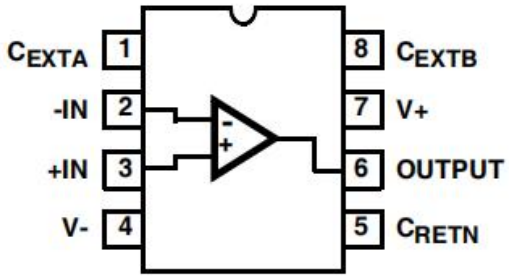
The ICL7650 Super Chopper-Stabilized Amplifier offers exceptionally low input offset voltage and is extremely stable with respect to time and temperature. It is a direct replacement for the industry-standard ICL7650 offering improved input offset voltage, lower input offset voltage temperature coefficient, reduced input bias current, and wider common mode voltage range.Critical parameters are guaranteed over the entire commercial temperature range.

ICL7650 unique CMOS chopper-stabilized amplifier circuitry is user-transparent, virtually eliminating the traditional chopper amplifier problems of intermodulation effects, chopping spikes, and overrange lockup.

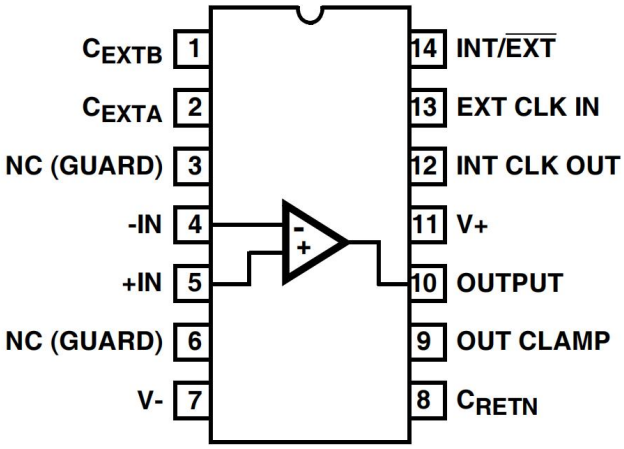
The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained. However the 14 pin lead version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7650 is internally compensated for unity-gain operation.

Pin Configurations

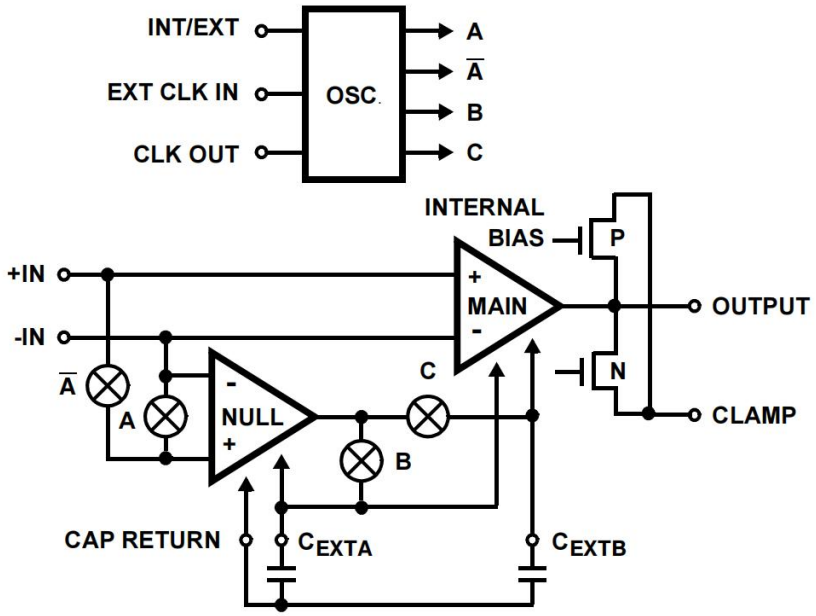


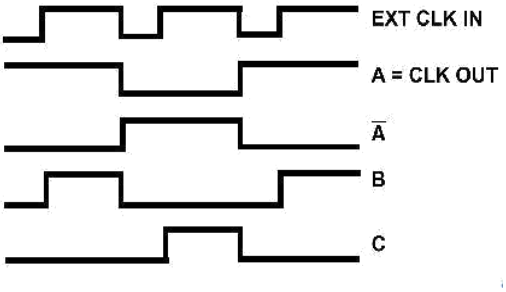
DIP-8/SOP-8



DIP-14

Functional Diagram





Absolute Maximum Ratings

Condition	Min	Max
Supply Voltage (V+ to V-)	-	18V
Input Voltage	(V++0.3)	(V--0.3)
Voltage on Oscillator Control Pins	V+	V-
Duration of Output Short Circuit	Indefinite	
Current to Any Pin	-	10mA
While Operating (Note 1)	-	100μA
Lead Temperature (Soldering, 10 seconds)	-	260℃

Note:Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.

Thermal Information

Condition		Min	Max
Thermal Resistance (Typical, Note 2) θ_{JA}(℃/W)	DIP-8 package	-	110℃/W
	DIP-14 package	-	90℃/W
	SOP-8 package	-	160℃/W
Maximum Junction Temperature (Plastic Package)		-	+150℃
Maximum Storage Temperature Range		-55℃	+150℃
Pb-free reflow profile		see link below	

*Pb-free DIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.
CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
NOTES:
1. Limiting input current to 100μA is recommended to avoid latchup problems. Typically 1mA is safe, however this is not guaranteed.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Operating Conditions

Condition	Min	Max
Temperature Range	0℃	70℃

Electrical Specifications

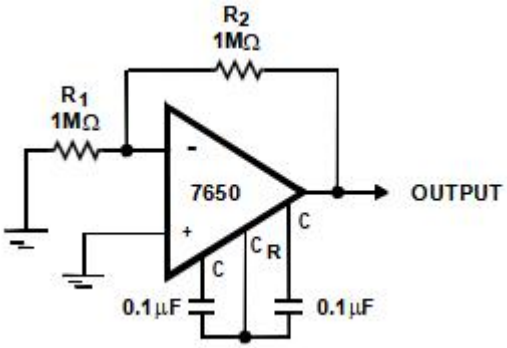
V_{SUPPLY} = ±5V. See Test Circuit, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 3)	V_{OS}		+25	-	±0.7	±5	μV
			0 to +70	-	±1	±8	μV
Average Temperature Coefficient of Input Offset Voltage (Note 3)	$\Delta V_{OS}/\Delta T$		0 to +70	-	0.02	-	μV/°C
Change in Input Offset with Time	$\Delta V_{OS}/\Delta T$		+25	-	100	-	$nV/\sqrt{month}$
Input Bias Current |I(+)|, |I(-)|	I_{BIAS}		+25	-	4	10	pA
			0 to +70	-	5	20	pA
Input Offset Current |I(-), |I(+)|	I_{OS}		+25	-	8	20	pA
			0 to +70	-	10	40	pA
Input Resistance	R_{IN}		+25	-	10^{12}	-	Ω
Large Signal Voltage Gain (Note 3)	A_{VOL}	RL=10kΩ, VO=±4V	+25	135	150	-	dB
			0 to +70	130	-	-	dB
Output Voltage Swing (Note 4)	V_{OUT}	RL = 10kΩ	+25	±4.7	±4.85	-	V
		RL = 100kΩ	+25	-	±4.95	-	V
Common Mode Voltage Range (Note 3)	CMVR		+25	-5	-5.2 to+4	3.5	V
			0 to +70	-5	-	3.5	V
Common Mode Rejection Ratio (Note 3)	CMRR	CMVR = -5V to +3.5V	+25	120	140	-	dB
			0 to +70	120	-	-	dB
Power Supply Rejection Ratio	PSRR	VS =±3V to±8V	+25	120	140	-	dB
Input Noise Voltage	eN	RS = 100Ω, f = DC to 10Hz	+25	-	2	-	μVP-P
Input Noise Current	iN	f = 10Hz	+25	-	0.01	-	$pA/\sqrt{Hz}$
Gain Bandwidth Product	GBWP		+25	-	2	-	MHz
Slew Rate	SR	CL=50pF,RL=10kΩ	+25	-	2.5	-	V/μs
Rise Time	t_R		+25	-	0.2	-	μs
Overshoot	OS		+25	-	20	-	%
Operating Supply Range	V+ to V-		+25	4.5	-	16	V
Supply Current	I_{SUPP}	No Load	+25	-	2	3	mA
			0 to +70	-	-	3.2	mA
Output Source Current	$I_{O\ SOURCE}$		+25	2.9	4.5	-	mA
			0 to +70	2.3	-	-	mA
Output Sink Current	$I_{O\ SINK}$		+25	25	30	-	mA
			0 to +70	20	-	-	mA
Internal Chopping Frequency	F_{CH}	Pins 13 and 14Open	+25	120	250	375	Hz
Clamp ON Current (Note 5)		RL=100KΩ	+25	25	70	-	μA
Clamp OFF Current (Note 5)		-4V≤V_{OUT}≤+4V	+25	-	0.001	5	nA
			0 to +70	-	-	10	nA

NOTES:

1. These parameters are guaranteed by design and characterization, but not tested at temperature extremes because thermocouple effects prevent precise measurement of these voltages in automatic test equipment.
2. OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs clamp current characteristics.
3. See OUTPUT CLAMP under detailed description.

Test Circuit



Application Information

Detailed Description

AMPLIFIER

The functional diagram shows the major elements of the ICL7650. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset-null capability. The main amplifier is connected continuously from the input to the output, while the nulling amplifier, under the control of the chopping oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET gates, are inherently high impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power supplyranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

Careful balancing of the input switches, and the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals, and also the feed forward-type injection into the compensation capacitor, which is the main cause of output spikes in this type of circuit.

INTERMODULATION

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs frequency characteristics near the chopping frequency.

These effects are substantially reduced in the ICL7650 by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7650, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

CAPACITOR CONNECTION

The null/storage capacitors should be connected to the CEXTA and CEXTB pins, with a common connection to the CRETN pin. This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to CRETN.

OUTPUT CLAMP

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled input differentials are avoided, together with the consequent charge buildup on the correction-storage capacitors. The output swing is slightly reduced.

COMPONENT SELECTION

The two required capacitors, CEXTA and CEXTB, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1μF, and to maintain the same relationship between the chopping frequency and the nulling time constant this value should be scaled approximately in proportion if an external clock is used. A high quality film type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1μV.

STATIC PROTECTION

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics, which may result in increased input-leakage currents.

LATCHUP AVOIDANCE

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (PNPN) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1mA to avoid latchup, even under fault conditions.

Output Stage/Load Driving

The output circuit is a high-impedance type (approximately 18kΩ), and therefore with loads less than this value, the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17dB lower with a 1kΩ load than with a 10kΩ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120dB even with a 1kΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10kΩ or higher. This will result in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.

THERMO-ELECTRIC EFFECTS

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1μV/°C, but up to tens of mV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-efficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7650. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

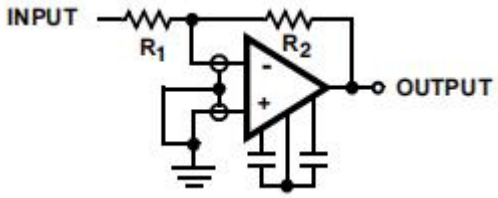


FIGURE 1A.INVERTING AMPLIFIER

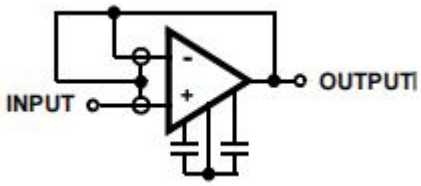
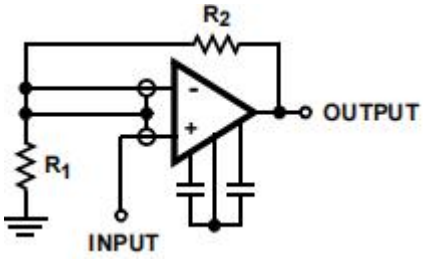


FIGURE 1B.FOLLOWER



NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ SHOULD BE LOW IMPEDANCE FOR OPTIMUM GUARDING

FIGURE 1C.NON-INVERTING AMPLIFIER

FIGURE 1.CONNECTION OF INPUT GUARDS

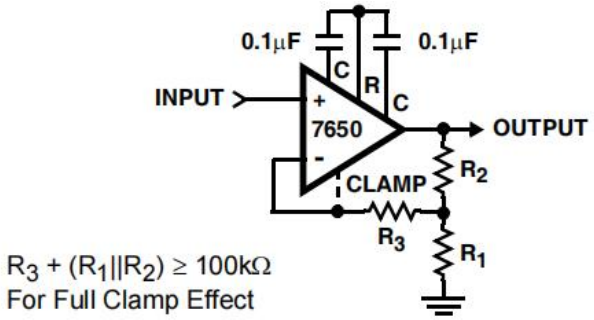
Pin Compatibility

The basic pinout of the 8-pin device corresponds, where possible, to that of the industry standard 8-pin devices, the 741 ,101, etc. The null-storing external capacitors are connected to pins 1 and 8, usually used for offset null or compensation capacitors, or simply not connected. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and V+, by two capacitors from those pins to pin 5, will provide easy compatibility. As for the 108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to pin 5 is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the 101 ,748 and similar parts.

The 14-pin device pinout corresponds most closely to that of the 108 device, owing to the provision of “NC” pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert it to the ICL7650.

Typical Applications

Clearly the applications of the ICL7650 will mirror those of other op amps. Anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7650 is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figures 2 and 3. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op amps by the ICL7650 are the supply voltage (±8V Max) and the output drive capability (10kΩ load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Figure 4, to enable the full output capabilities of the 741 (or any other standard device) to be combined with the input capabilities of the ICL7650. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.

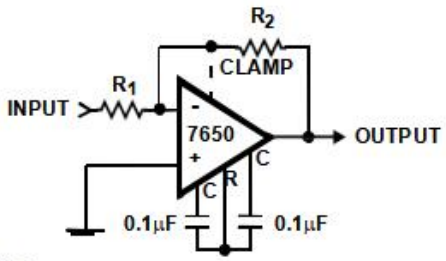


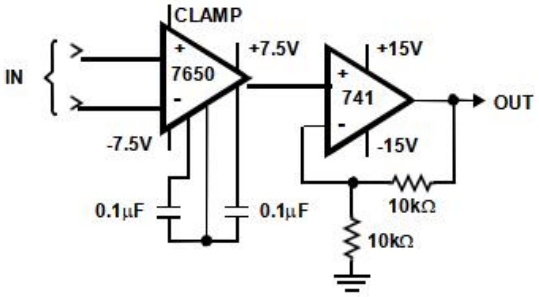
OTE: R1||R2 indicates the parallel combination of R_1 and R_2.

FIGURE 2. NON INVERTING AMPLIFIER WITH OPTIONAL CLAMP

Figure 5 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current ≈ VIN/R without disturbing other portions of the system.

The pin configuration of the 14 pin dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the 108).





NOTE: R1||R2 indicates the parallel combination of R1 and R2.

FIGURE 3. INVERTING AMPLIFIER WITH(OPTIONAL)CLAMP

FIGURE 4. USING 741 TO BOOST OUTPUT DRIVE CAPACITY

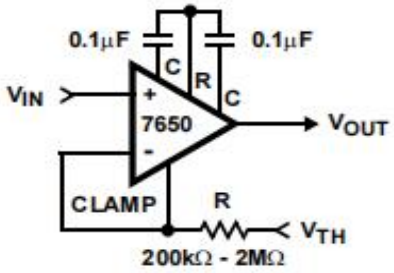


FIGURE 5. LOW OFFSET COMPARATOR

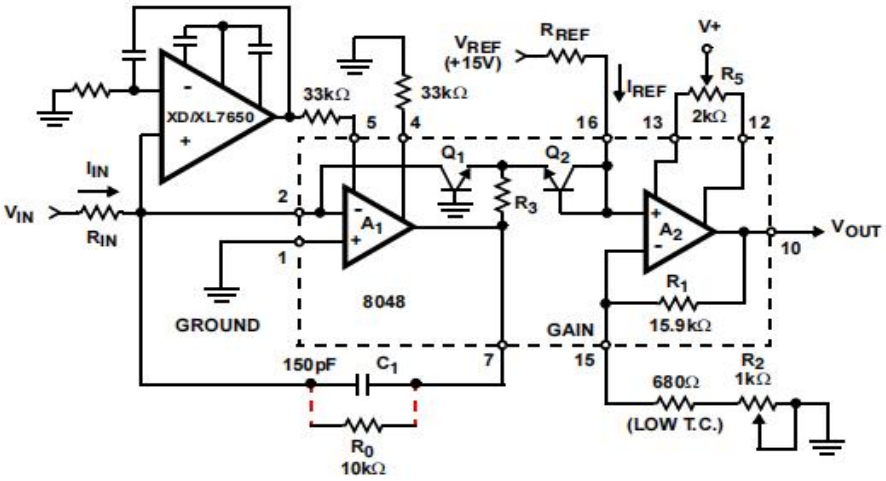


FIGURE 6.8048 OFFSET NULLED BY ICL7650

Normal logarithmic amplifiers are limited in dynamic range in the voltage-input mode by their input-offset voltage. The built-in temperature compensation and convenience features of the 8048 can be extended to a voltage-input dynamic range of close to 6 decades by using the ICL7650 to offset-null the 8048, as shown in Figure 6. The same concept can also be used with such devices as the 2500 or 2600 families of op amps to add very low offset voltage capability to their very high slew rates and bandwidths. Note that these circuits will also have their DC gains, CMRR, and PSRR enhanced.

Typical Performance Curves

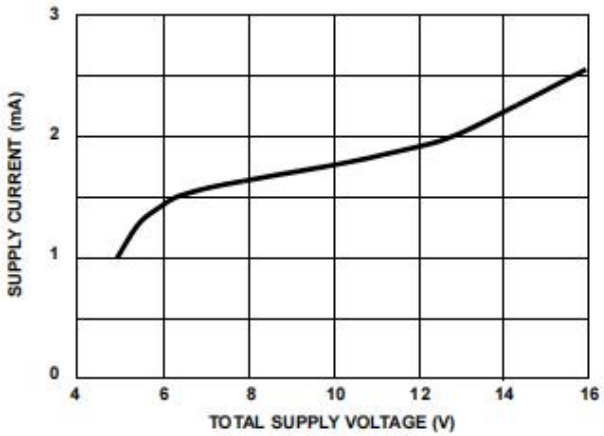


FIGURE 7. SUPPLY CURRENT vs SUPPLY VOLTAGE

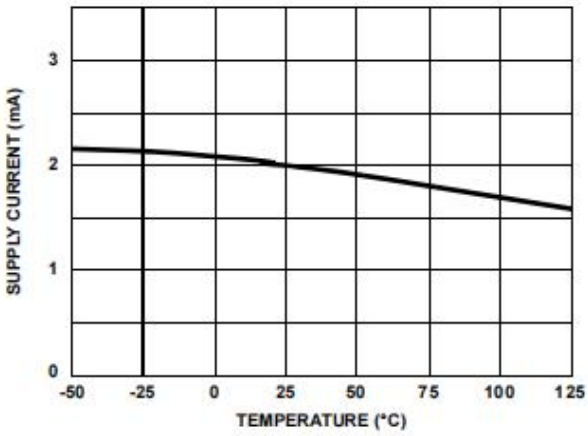


FIGURE 8. SUPPLY CURRENT vs AMBIENT TEMPERATURE

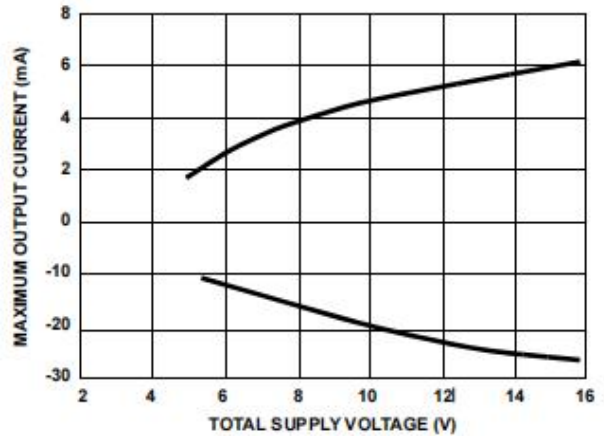


FIGURE 9. MAXIMUM OUTPUT CURRENT vs SUPPLY VOLTAGE

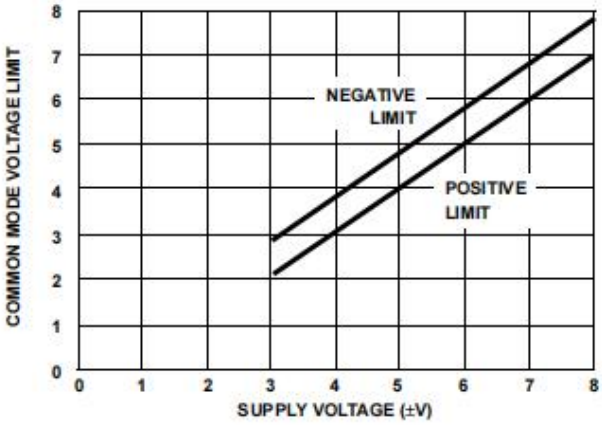


FIGURE 10. COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

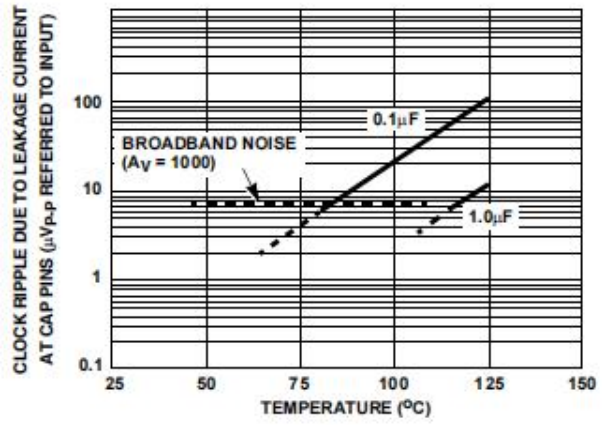


FIGURE 11. CLOCK RIPPLE REFERRED TO THE INPUT vs TEMPERATURE

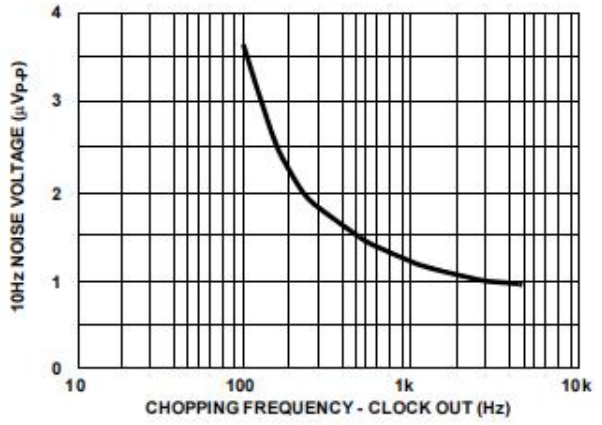


FIGURE 12. 10Hz NOISE VOLTAGE vs CHOPPING FREQUENCY

Typical Performance Curves (Continued)

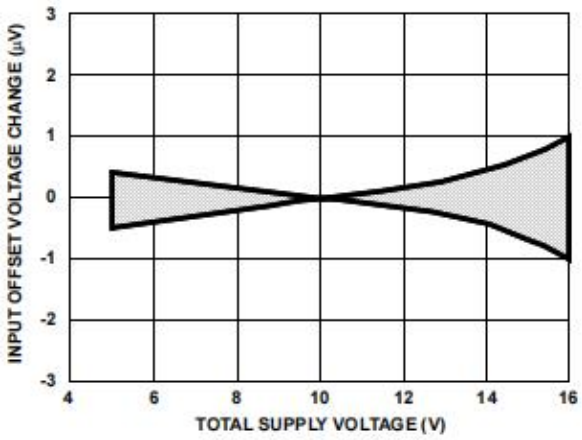


FIGURE 13. INPUT OFFSET VOLTAGE CHANGE vs SUPPLY VOLTAGE

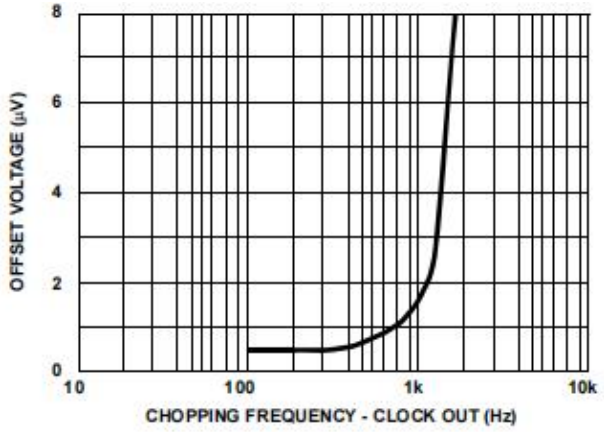


FIGURE 14. INPUT OFFSET VOLTAGE vs CHOPPING FREQUENCY

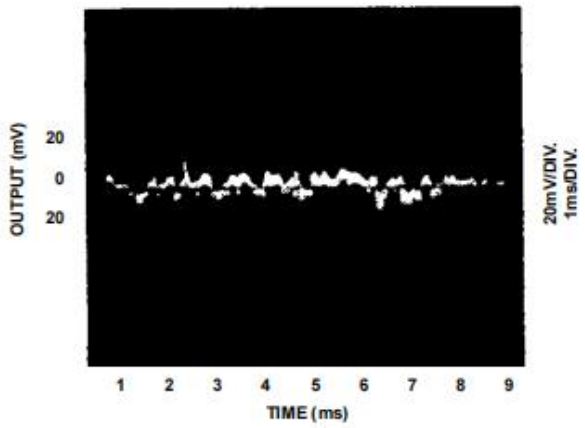


FIGURE 15. OUTPUT WITH ZERO INPUT; GAIN = 1000; BALANCED SOURCE IMPEDANCE = 10kΩ

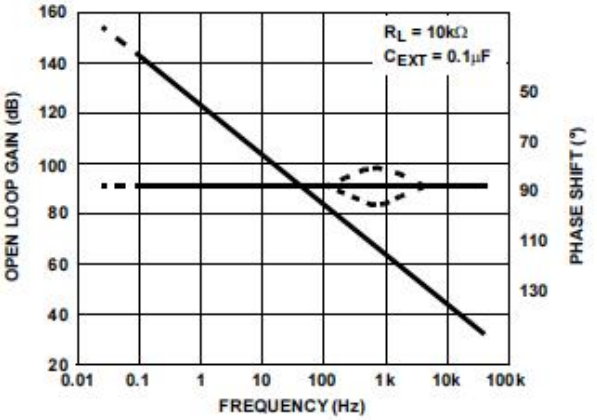


FIGURE 16. OPEN LOOP GAIN AND PHASE SHIFT vs FREQUENCY

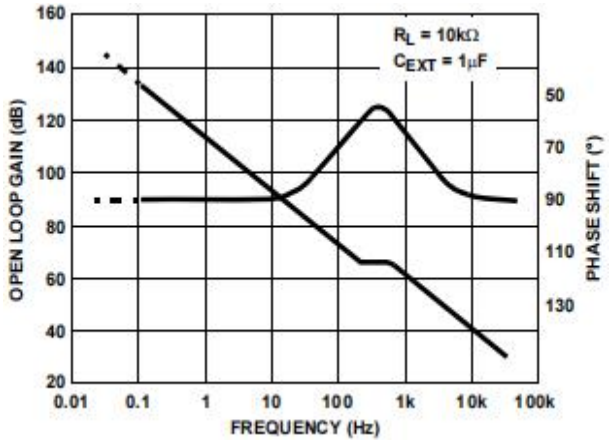
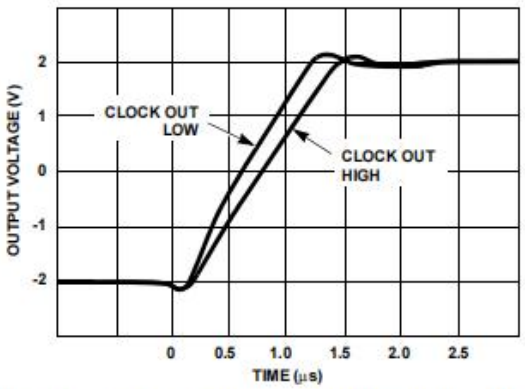


FIGURE 17. OPEN LOOP GAIN AND PHASE SHIFT vs FREQUENCY



NOTE: The two different responses correspond to the two phases of the clock.

FIGURE 18. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (NOTE)

Typical Performance Curves (Continued)

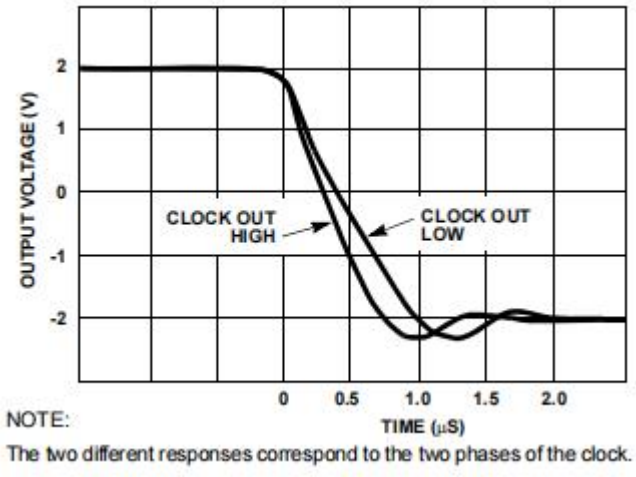


FIGURE 19. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (NOTE)

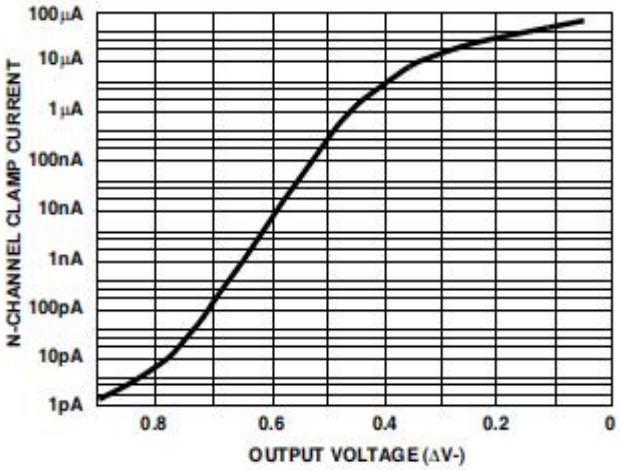


FIGURE 20. N-CHANNEL CLAMP CURRENT vs OUTPUT VOLTAGE

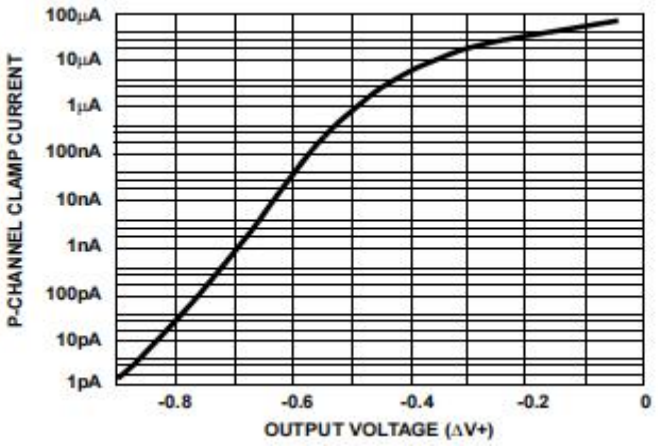
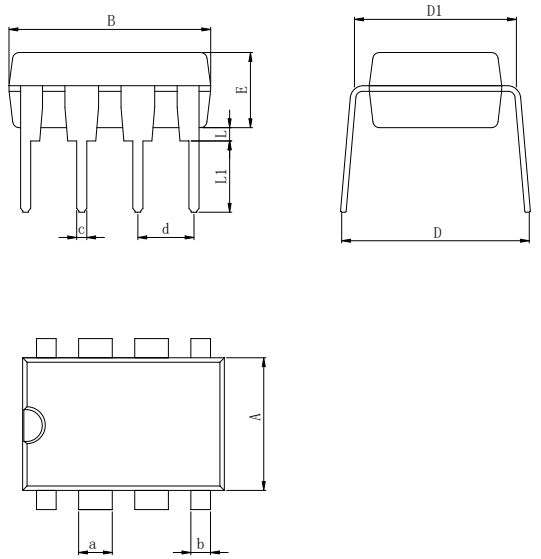


FIGURE 21. P-CHANNEL CLAMP CURRENT vs OUTPUT VOLTAGE

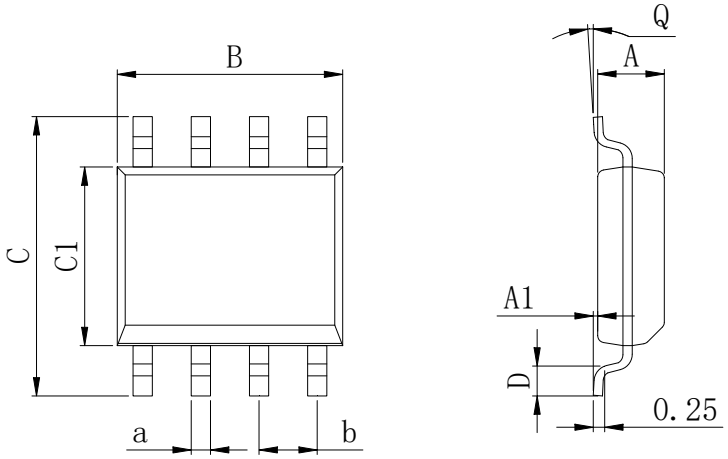
Physical Dimensions

DIP-8



Dimensions In Millimeters(DIP-8)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

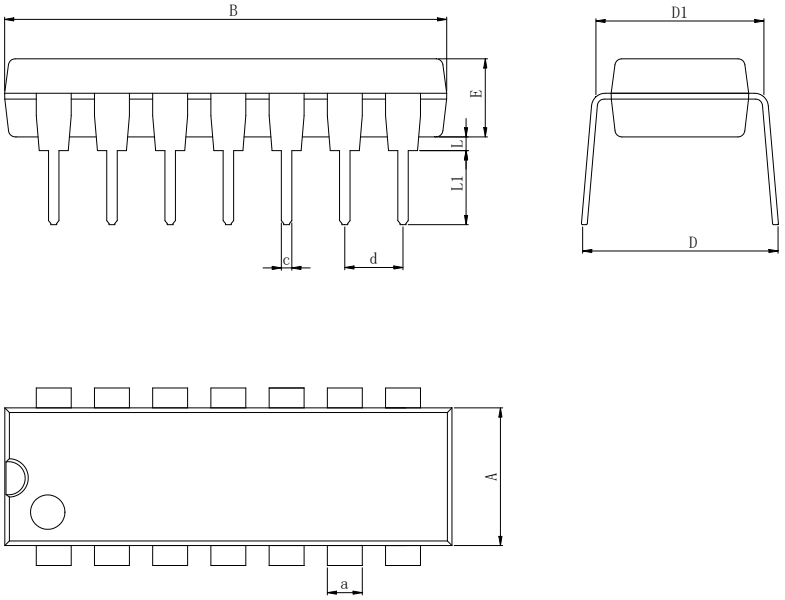
SOP-8



Dimensions In Millimeters(SOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

Physical Dimensions

DIP-14



Dimensions In Millimeters(DIP-14)										
Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.50	

Revision History

DATE	REVISION	PAGE
2014-6-8	New	1-16
2023-9-13	Update encapsulation type、 Updated DIP-8 dimension、 Add annotation for Maximum Ratings.Add DIP-14 package	1、3、14
2024-11-1	Update Lead Temperature	4

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