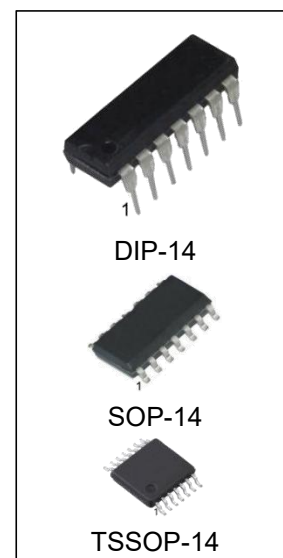


CD4066 Quad Bilateral Switches

Features:

- Wide supply voltage range from 3V to 15V
- Fully static operation
- 5V and 15V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from -40°C to +85°C
- Packaging information: DIP14/SOP14/TSSOP14



Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
CD4066BE/ CD4066BN	DIP-14	CD4066B	TUBE	1000pcs/box
CD4066BM/TR	SOP-14	CD4066B	REEL	2500pcs/reel
CD4066BMT/TR	TSSOP-14	CD4066B	REEL	2500pcs/reel

General Description

The CD4066B provides four single-pole, single-throw analog switch functions. Each switch has two input/output terminals (nY and nZ) and an active HIGH enable input (nE). When nE is LOW, the analog switch is turned off.

Block Diagram

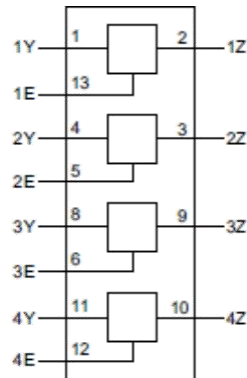


Figure 1. Functional diagram

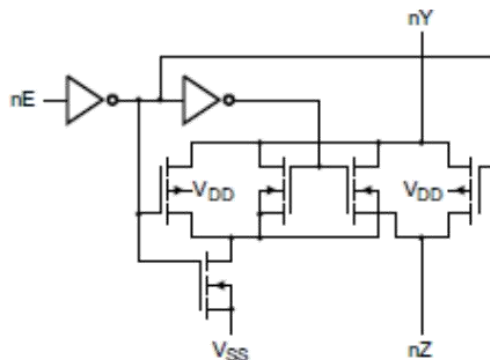


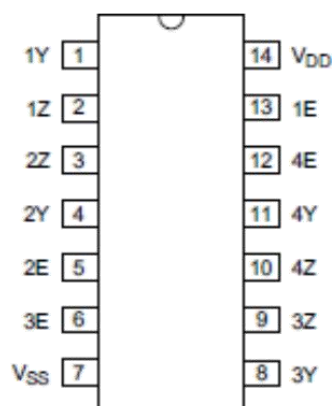
Figure 2. Logic diagram (one switch)

Function Table

Input	Switch
nE	
H	ON
L	OFF

Note: H=HIGH voltage level; L=LOW voltage level.

Pin Configurations



DIP-14/SOP-14/TSSOP-14

Pin Description

Pin No.	Pin Name	Description
1	1Y	independent input or output
2	1Z	independent input or output
3	2Z	independent input or output
4	2Y	independent input or output
5	2E	enable input (active HIGH)
6	3E	enable input (active HIGH)
7	V _{SS}	ground (0V)
8	3Y	independent input or output
9	3Z	independent input or output
10	4Z	independent input or output
11	4Y	independent input or output
12	4E	enable input (active HIGH)
13	1E	enable input (active HIGH)
14	V _{DD}	supply voltage

Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{DD}	-	-0.5	+15	V
input voltage	V_I	-	-0.5	$V_{DD}+0.5$	V
input clamping current	I_{IK}	$V_I < 0.5V$ or $V_I > V_{DD}+0.5V$	-	± 10	mA
input/output current	$I_{I/O}$	-	-	± 10	mA
storage temperature	T_{stg}	-	-65	+150	°C
total power dissipation	P_{tot}	-	-	500	mW
device dissipation	P	per output transistor	-	100	mW
Soldering temperature	T_L	10s	260		°C

Note: 1、Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.
2、For DIP14 packages: above 70°C the value of P_{tot} derates linearly with 12mW/K.
3、For SOP14 packages: above 70°C the value of P_{tot} derates linearly with 8mW/K.
4、For (T)SSOP14 packages: above 60°C the value of P_{tot} derates linearly with 5.5mW/K.

Recommended Operating Conditions

($T_{amb}=25^{\circ}C$; $R_L=10k\Omega$; $C_L=50pF$; $nE=V_{DD}$; $Vis=V_{DD}=5V$.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	-	12	V
ambient temperature	T_{amb}	in free air	-40	-	+85	°C
input voltage	V_I	-	0	-	V_{DD}	V
Disable output time (High level→turn off)	t_{PHZ}	nE to nZ or nE to nY	-	80	160	ns
Disable output time (Low level→turn off)	t_{PLZ}	nE to nZ or nE to nY	-	80	160	ns
Enable output time (turn off→high/low level)	t_{PZH}, t_{PZL}	-	-	45	90	ns
input capacitance	C_i	-	-	-	7.5	pF

Electrical Characteristics

DC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)		$T_{amb}=25^{\circ}\text{C}$			Unit
				Min.	Typ.	Max.	
supply current	I_{DD}	$V_I=V_{DD}$ or V_{SS} , $I_O=0\text{A}$	$V_{DD}=5\text{V}$	-	-	6	μA
			$V_{DD}=10\text{V}$	-	-	7	μA
			$V_{DD}=15\text{V}$	-	-	8	μA
HIGH-level input voltage	V_{IH}	$ I_O <1\mu\text{A}$	$V_{DD}=5\text{V}$ $V_O=0.5\text{V}$ or 5V	3.5	-	-	V
			$V_{DD}=10\text{V}$ $V_O=0.5\text{V}$ or 10V	7.0	-	-	V
			$V_{DD}=15\text{V}$ $V_O=0.5\text{V}$ or 15V	11	-	-	V
LOW-level input voltage	V_{IL}	$ I_O <1\mu\text{A}$	$V_{DD}=5\text{V}$ $V_O=0.5\text{V}$ or 5V	-	-	1.5	V
			$V_{DD}=10\text{V}$ $V_O=0.5\text{V}$ or 10V	-	-	3.0	V
			$V_{DD}=15\text{V}$ $V_O=0.5\text{V}$ or 15V	-	-	4	V
input leakage current	I_I	$V_I=0\text{V}$ or 15V , $V_{DD}=15\text{V}$		-	-	0.3	μA
ON resistance (rail)	R_{ON}	$V_I=0\text{V}$ to $V_{DD}-V_{EE}$	$V_{DD}-V_{EE}=5\text{V}$	-	350	2500	Ω
			$V_{DD}-V_{EE}=10\text{V}$	-	80	245	Ω
			$V_{DD}-V_{EE}=15\text{V}$	-	80	240	Ω
		$V_I=0\text{V}$	$V_{DD}-V_{EE}=5\text{V}$	-	115	340	Ω
			$V_{DD}-V_{EE}=10\text{V}$	-	50	160	Ω
			$V_{DD}-V_{EE}=15\text{V}$	-	50	140	Ω
		$V_I=V_{DD}-V_{EE}$	$V_{DD}-V_{EE}=5\text{V}$	-	120	365	Ω
			$V_{DD}-V_{EE}=10\text{V}$	-	65	200	Ω
			$V_{DD}-V_{EE}=15\text{V}$	-	45	170	Ω
ON resistance mismatch between channels	ΔR_{ON}	$V_I=0\text{V}$ to $V_{DD}-V_{EE}$	$V_{DD}-V_{EE}=5\text{V}$	-	25	-	Ω
			$V_{DD}-V_{EE}=10\text{V}$	-	10	-	Ω
			$V_{DD}-V_{EE}=15\text{V}$	-	5	-	Ω

Note: On resistance waveform and test circuit see Figure 9 and Figure 10.

DC Characteristics 2

($T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)		T _{amb} =-40℃		T _{amb} =+85℃		Unit
				Min.	Max.	Min.	Max.	
supply current	I _{DD}	V _I =V _{DD} or V _{SS} , I _O =0A	V _{DD} =5V	-	5	-	7	μA
			V _{DD} =10V	-	6	-	8	μA
			V _{DD} =15V	-	7.5	-	9	μA
HIGH-level input voltage	V _{IH}	I _O <1μA	V _{DD} =5V, V _O =0.5V or 5V	3.5	-	3.5	-	V
			V _{DD} =10V, V _O =0.5V or 10V	7.0	-	7.0	-	V
			V _{DD} =15V, V _O =0.5V or 15V	11	-	11	-	V
LOW-level input voltage	V _{IL}	I _O <1μA	V _{DD} =5V, V _O =0.5V or 5V	-	1.5	-	1.5	V
			V _{DD} =10V, V _O =0.5V or 10V	-	3.0	-	3.0	V
			V _{DD} =10V, V _O =0.5V or 10V	-	4.0	-	4.0	V
input leakage current	I _I	V _I =0V or 15V, V _{DD} =15V		-	-	-	1.0	μA

AC Characteristics 1

($T_{amb} = 25^{\circ}\text{C}$, $V_{EE} = V_{SS} = 0\text{V}$, $t_r, t_f \leq 20\text{ns}$, $C_L = 50\text{pF}$, $R_L = 10\text{k}\Omega$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
HIGH to LOW propagation delay time	t_{PHL}	nY to nZ; nZ to nY; see Figure 4	$V_{DD}=5V$	-	10	20	ns
			$V_{DD}=10V$	-	5	10	ns
			$V_{DD}=15V$	-	5	10	ns
LOW to HIGH propagation delay	t_{PLH}	nY to nZ; nZ to nY; see Figure 4	$V_{DD}=5V$	-	10	20	ns
			$V_{DD}=10V$	-	5	10	ns
			$V_{DD}=15V$	-	5	10	ns
HIGH to OFF-state propagation delay	t_{PHZ}	nE to nY, nZ; see Figure 5	$V_{DD}=5V$	-	80	160	ns
			$V_{DD}=10V$	-	65	130	ns
			$V_{DD}=15V$	-	65	110	ns
LOW to OFF-state propagation delay	t_{PLZ}	nE to nY, nZ; see Figure 5	$V_{DD}=5V$	-	80	160	ns
			$V_{DD}=10V$	-	70	130	ns
			$V_{DD}=15V$	-	70	110	ns
OFF-state to HIGH propagation delay	t_{PZH}	nE to nY, nZ; see Figure 5	$V_{DD}=5V$	-	40	80	ns
			$V_{DD}=10V$	-	20	60	ns
			$V_{DD}=15V$		20	50	ns
OFF-state to LOW propagation delay	t_{PZL}	nE to nY, nZ; see Figure 5	$V_{DD}=5V$	-	45	90	ns
			$V_{DD}=10V$	-	20	60	ns
			$V_{DD}=15V$		20	50	ns

AC Characteristics 2

($T_{amb}=25^{\circ}\text{C}$, $V_{EE}=V_{SS}=0\text{V}$, $V_I=0.5V_{DD}$ (p-p), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Square wave distortion	d _{sin}	see Figure 6; RL=10kΩ; CL=15pF; channel ON; fi=1kHz	VDD=5V	0.25	-	-	%
			VDD=9V	0.04	-	-	%
any two channel crosstalk	f _{ct}	VDD=9V, see note2		1	-	-	MHz
crosstalk voltage (nE to nY to nZ)	V _{ct}	see Figure 7; RL=10kΩ; CL=15pF; E or Sn=VDD (square-wave)		50	-	-	mV
OFF frequency	f _{OFF}	VDD=10V, see note3		1	-	-	MHz
conduction frequency	f _{ON}	VDD=5V, see note4		-	-	-	MHz
		VDD=15V, see note4		9.0	-	-	MHz

Note:

- (1) f_i is biased at $0.5V_{DD}$; $V_I=0.5V_{DD}$ (p-p).
- (2) $R_L=1\text{k}\Omega$; $20\log V_{os}/V_{is}=-50\text{dB}$, see Figure 8.
- (3) $R_L=1\text{k}\Omega$; $C_L=5\text{pF}$, channel off, $20\log V_{os}/V_{is}=-50\text{dB}$, see Figure 6.
- (4) $R_L=1\text{k}\Omega$; $C_L=5\text{pF}$, channel on, $20\log V_{os}/V_{is}=-3\text{dB}$, see Figure 6.

Testing Circuit

AC Testing Circuit 1

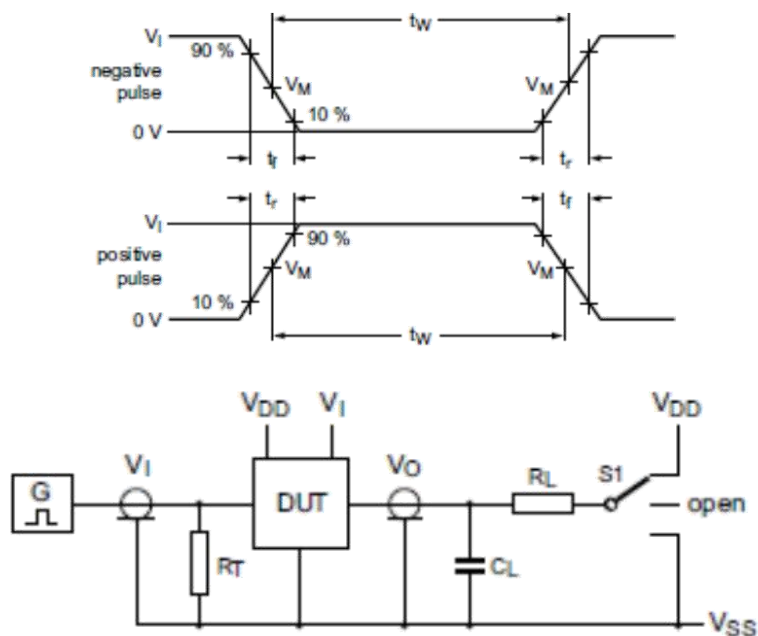


Figure 3. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L =Load resistance.

AC Testing Waveforms

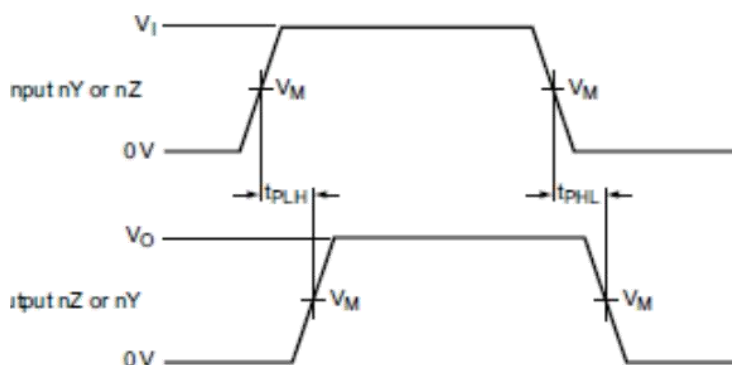


Figure 4. nY or nZ to nZ or nY propagation delays

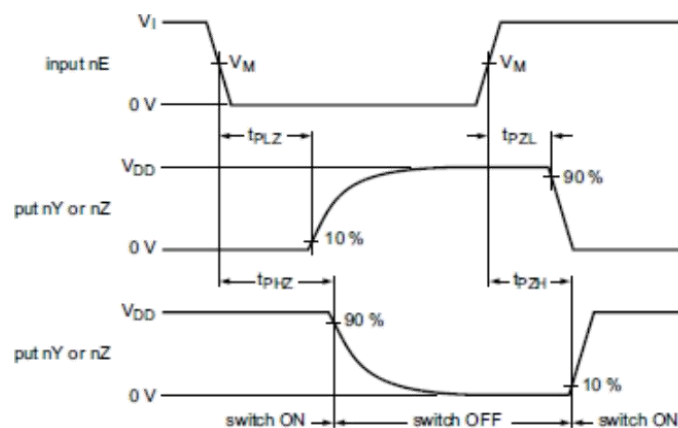


Figure 5. Enable and disable times

AC Testing Circuit 2

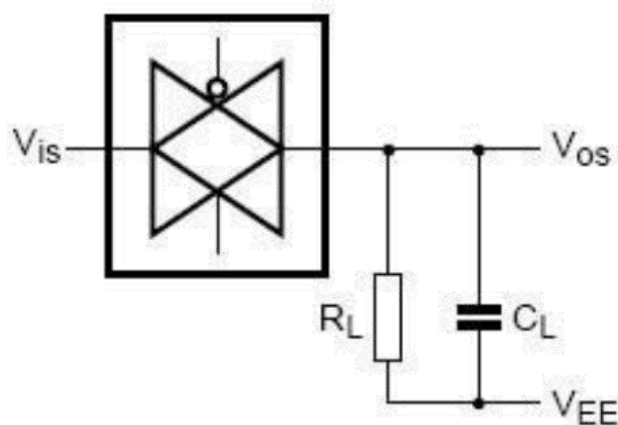


Figure 6. Square wave distortion degree of cut-off frequency and conduction frequency test pattern

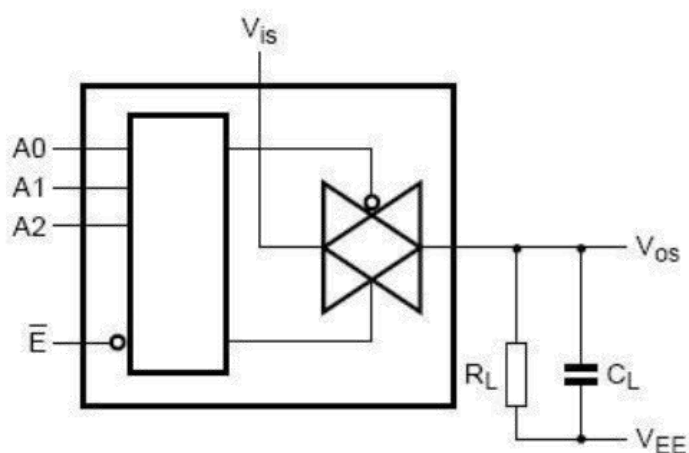


Figure 7. Crosstalk logical input/output test

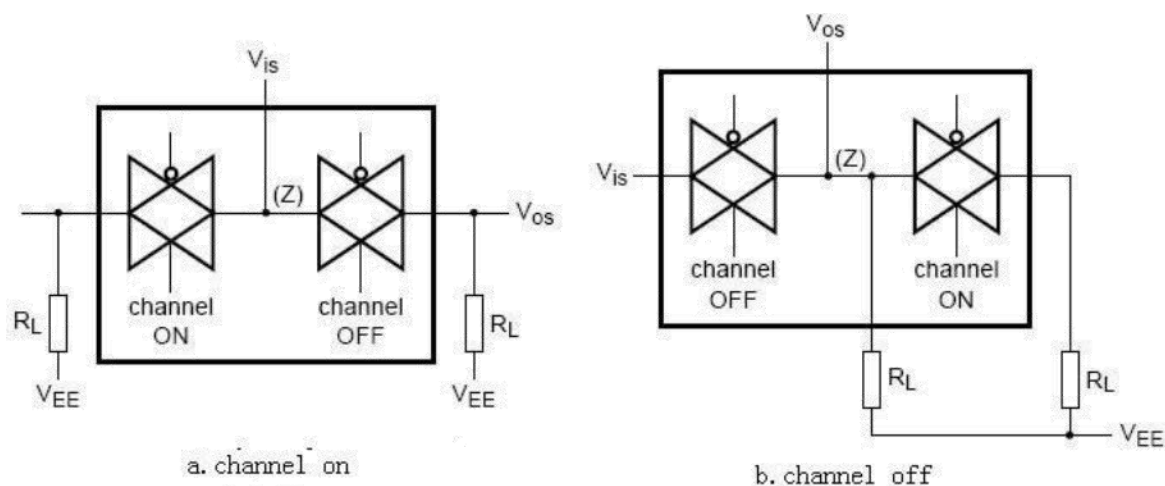
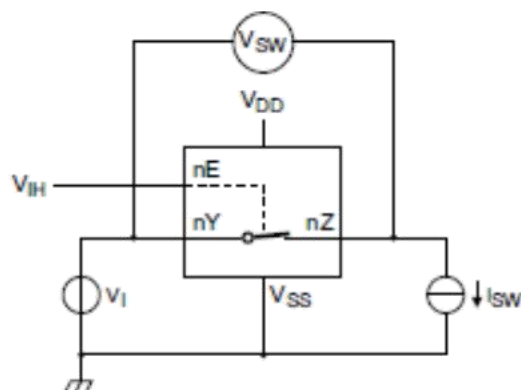


Figure 8. Inter channel Crosstalk

On Resistance Waveform And Test Circuit



$$R_{ON} = V_{SW} / I_{SW}$$

Figure 9. Test circuit for measuring R_{ON}

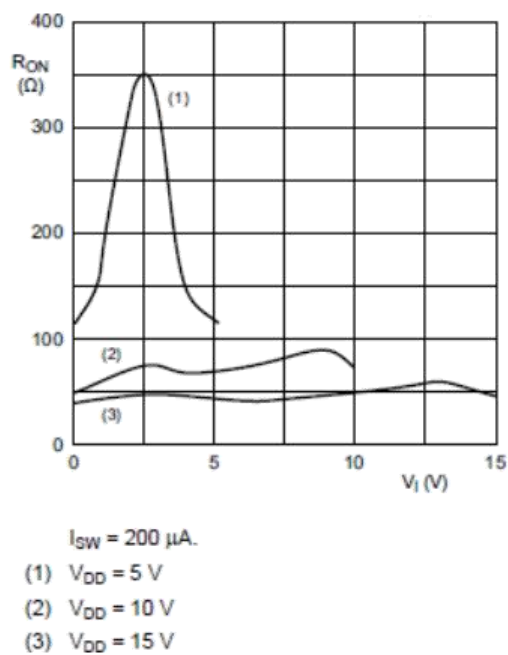


Figure 10. Typical R_{ON} as a function of input voltage

Measurement Points

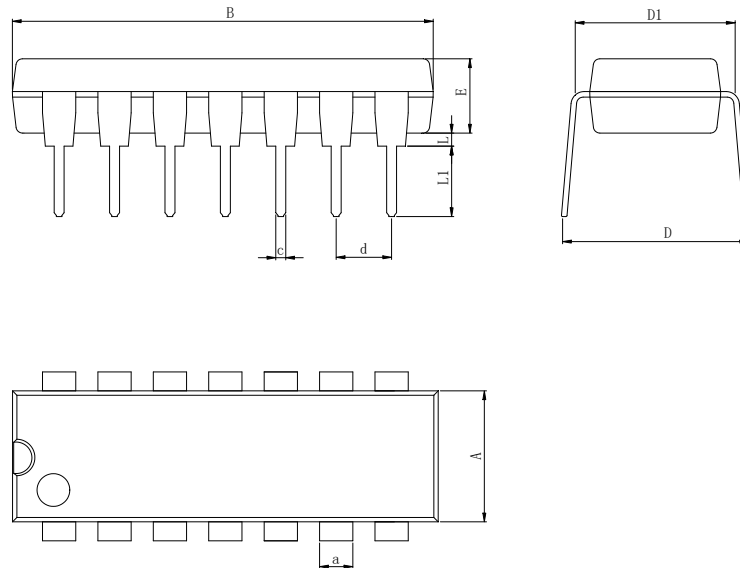
Supply voltage	Input	Output
V_{DD}	V_M	V_M
3V to 15V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

Test Data

Test	Input		Load		Switch
	V_{is}	t_r, t_f	C_L	R_L	
t_{PHL}	V_{EE}	20ns	50pF	10kΩ	V_{DD}
t_{PLH}	V_{DD}	20ns	50pF	10kΩ	V_{EE}
t_{PZH}, t_{PHZ}	V_{DD}	20ns	50pF	10kΩ	V_{EE}
t_{PZL}, t_{PLZ}	V_{EE}	20ns	50pF	10kΩ	V_{DD}
others	pulse	20ns	50pF	10kΩ	open

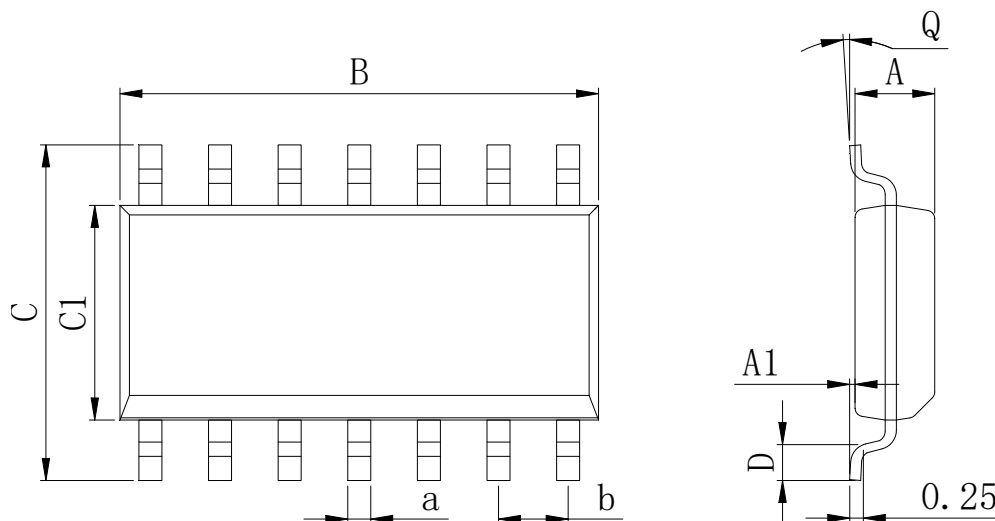
Physical Dimensions

DIP-14



Dimensions In Millimeters(DIP-14)										
Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.50	

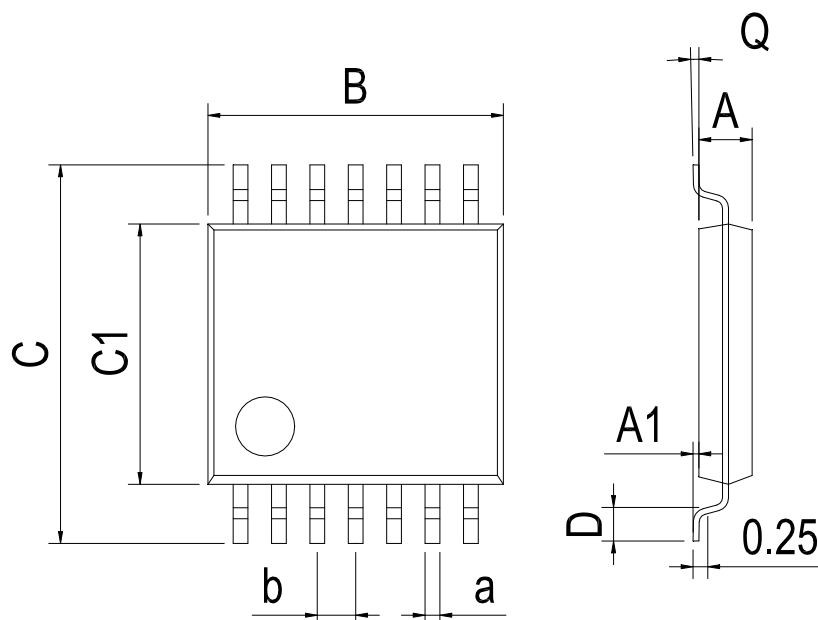
SOP-14



Dimensions In Millimeters(SOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	

Physical Dimensions

TSSOP-14



Dimensions In Millimeters(TSSOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2015-5	New	1-15
V1.1	2020-4	Document Reformatting、 Update DIP Package New Model	1-15、 1
V1.2	2024-11	Update supply voltage range from 3V to 15V、 Update Lead Temperature	1、 4

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