SQ29020

High Efficiency, 16V/20A Synchronous Step-down Regulator

General Description

The SQ29020 is a high-efficiency synchronous step-down DC-DC regulator featuring internal power and synchronous rectifier switches capable of delivering 20A of continuous output current over a wide input voltage range, from as low as 2.9V up to 16V. The output voltage is adjustable from 0.6V to 5.5V.

Silergy's proprietary Instant-PWM™ fast-response, constant-on-time (COT) PWM control method supports high input/output voltage ratios (low duty cycles) and responds to load transients within ~100ns while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation, even with low ESR ceramic output capacitors.

The stable internal reference (V_{REF}) provides ±1% accuracy over T_J= -40°C to 125°C, and the differential input sense configuration allows the feedback sensing at the most relevant load point.

Internal 7.5mΩ power and 2.4mΩ synchronous rectifier switches provide excellent efficiency for a wide range of applications, especially for low output voltages and low duty cycles. Cycle-by-cycle current limit, input under-voltage lock-out, internal soft-start, output under- and over-voltage protection, and thermal shutdown provide safe operation in all operating conditions.

The SQ29020 is available in a compact QFN3×4 package.

Features

- Wide Input Voltage Range:
  - 2.9V to 16V if VCC is Supplied by External Source
  - 3.6V to 16V if VCC is Supplied by VIN
- Internal 7.5mΩ Power Switch and 2.4mΩ Synchronous Rectifier
- Accurate Feedback Set Point: 0.6V ±1%
- Differential Remote Sense
- Fast Transient Response
- 600kHz, 800kHz and 1000kHz Operating Frequency
- Selectable Automatic High-efficiency Discontinuous Operating Mode at Light Loads
- Programmable Valley Current Limit
- Reliable Built-in Protections:
  - Automatic Recovery for Input Under-voltage (UVLO), Output Under-voltage (UVP) and Over-temperature (OTP) Conditions
  - Cycle-by-cycle Valley and Peak Current Limit (OCP)
  - Cycle-by-cycle Reverse Current Limit
- Internal and Adjustable Soft-start to Limits Inrush Current
- Smooth Pre-biased Startup
- Power Good Output Monitor for Under-voltage and Over-voltage

Applications

- Telecom and Networking Systems
- Servers
- High Power Access Points
- Storage Systems
- Cellular Base Stations

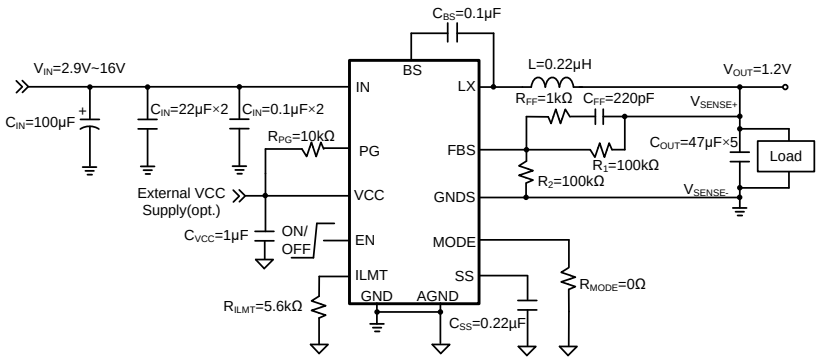


Figure 1. Typical Application Circuit

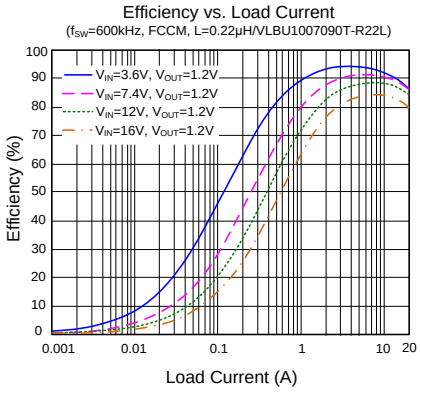


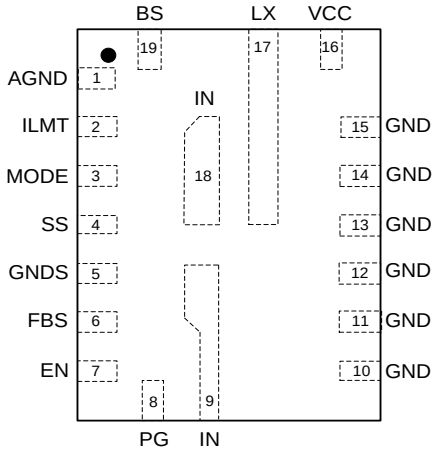
Figure 2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package Type	Top mark
SQ29020VDC	QFN3×4-19 RoHS Compliant and Halogen Free	DDE*xyz*

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin No	Pin Name	Pin Description
1	AGND	Analog ground
2	ILMT	Synchronous rectifier current limit setting. Connect a resistor to AGND to set the inductor valley current limit
3	MODE	Operation mode selection. Program MODE to select FCCM/PFM, and the operating switching frequency. See table 1
4	SS	External soft-start setting. Optionally adjust the soft-start time by adding an appropriate external capacitor between this pin and AGND pin. See Detailed Description
5	GNDS	Remote ground sense. Connect this pin directly to the negative side of the preferred voltage sense point. Short to GND if remote sense is not used
6	FBS	Remote feedback sense. Connect this pin to the center point of the output resistor divider to program the output voltage. See Design Procedure
7	EN	Enable input. Pull low to disable the device, high to enable. Do not leave this pin floating. May be used for increasing startup voltage or sequencing. See Detailed Description
8	PG	Power good indicator. Open drain output when the output voltage is within 92.5% to 120% of the regulation set point
9, 18	IN	Power input. Decouple this pin to GND pin with at least a 30μF ceramic capacitor
10, 11, 12, 13, 14, 15	GND	Power ground
16	VCC	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuits. Decouple this pin to GND with at least a 1μF ceramic capacitor. Make one good Kelvin connection from AGND to VCC capacitor GND connection. Use short, direct connections and avoid the use of vias. May be driven by an external bias supply. See Detailed Description.
17	LX	Inductor pin. Connect this pin to the switching node of the inductor
19	BS	Boot-strap supply for the high side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin

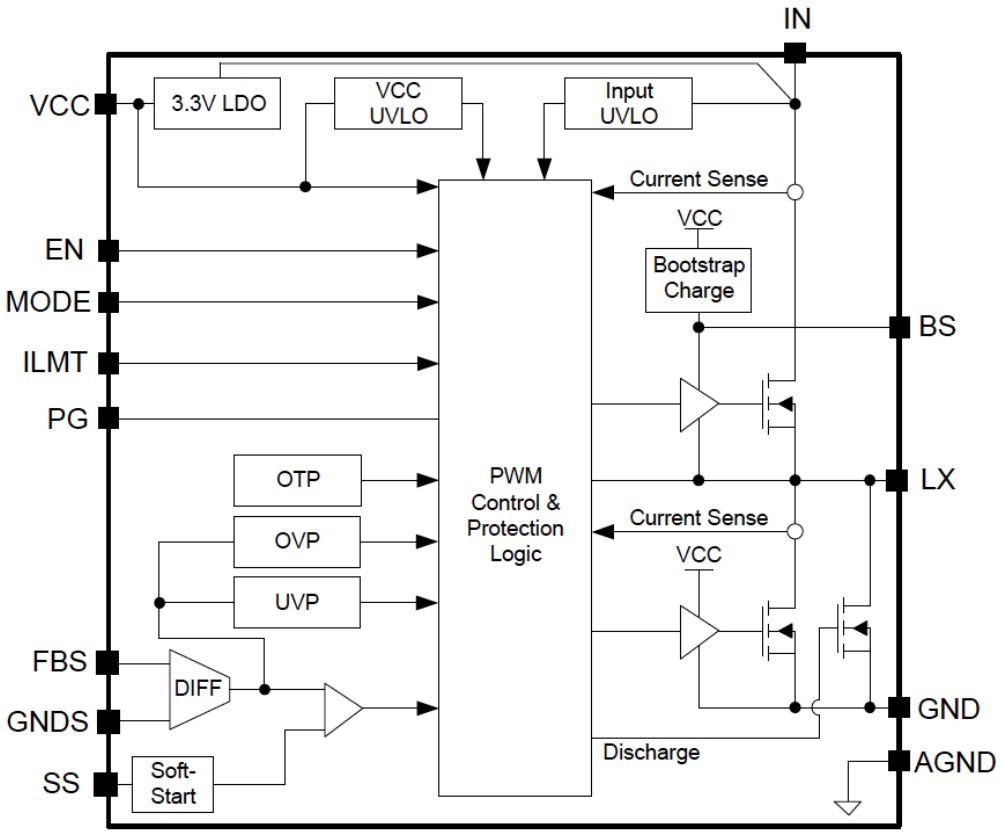


Figure 3. Block Diagram

Absolute Maximum Ratings (1)	**Min**	**Max**	**Unit**
IN	-0.3	18	V
ILMT, SS	-0.3	4	
EN, MODE, LX	-0.3	IN + 0.3	
LX, 10ns Duration	-5	IN + 5	
BS	LX - 0.3	LX + 4	
FBS, GNDS, AGND, VCC, PG	-0.3	4	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature	-65	150	

Thermal Information (2)	**Min**	**Max**	**Unit**
θJA Junction-to-ambient Thermal Resistance		24	°C/W
θJC Junction-to-case Thermal Resistance		4.5	
PD Power Dissipation TA = 25°C		4.2	W

Recommended Operating Conditions (3)	**Min**	**Max**	**Unit**
IN	2.9	16	V
Output Voltage	0.6	5.5	
GNDS	-0.2	0.2	
VCC External Bias	3.12	3.6	
Output Current		20	A
Output Current Limit Setting		24	
Peak Inductor Current		28	
Junction Temperature	-40	125	°C

Electrical Characteristics V_{IN} = 12V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise specified (4).							
Parameter		**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Input	Voltage	V_{IN}		2.9		16	V
	UVLO, rising	$V_{IN,UVLO}$		2.6	2.75	2.9	V
	UVLO, Hysteresis	$V_{IN,HYS}$			200		mV
	Shutdown Current	I_{SHDN}	V_{EN}=0V, T_J=25°C		2	5	µA
	Quiescent Current	I_Q	V_{EN}=2V, V_{FBS} = 0.65V, PFM mode, No Switching		550	850	µA
VCC	UVLO, Rising	$V_{VCC,UVLO}$				2.5	V
	UVLO, Hysteresis	$V_{VCC,HYS}$			100		mV
	Output	V_{CC}	I_{VCC}=0mA	3.15	3.3	3.45	V
	Load regulation	$V_{CC,REG}$	I_{VCC}=25mA		1.4		%
	External Bias input	$V_{CC,EXT}$	optional	3.15		3.6	V
FBS	Reference Voltage	V_{REF}	GNDS = 0V	0.594	0.600	0.606	V
	Error Amp Offset	V_{OS}		-3		3	mV
	Input Current	I_{FBS}	V_{EN}=2V, V_{FBS} = 1V	-50	0	50	nA
Power Switch	On resistance	$R_{DS(ON)HS}$	V_{BS-LX} = 3.3V, T_J=25°C		7.5	11.3	mΩ
	Leakage	$I_{HS, LKG}$	V_{EN}=0V, VLX=0V		0.01	8	µA
	Current Limit	$I_{LMT,HS}$		25.5	28	33	A
Synchronous Rectifier	On resistance	$R_{DS(ON)LS}$	V_{CC} = 3.3V, T_J=25°C		2.4	3.6	mΩ
	Leakage	$I_{LS, LKG}$	V_{EN}=0V, V_{LX}=12V		0.04	32	µA
	Reverse current	$I_{LMT,RVS}$		9	13	16	A
		$t_{RCL,BLK}$		40	60		ns
	Forward current	$I_{LMT,BOT}$	R_{ILMT} = 5.6kΩ		21.4		A
ILMT Pin Output Voltage		V_{ILMT}		1.15	1.2	1.25	V
ILMT Ratio		$I_{ILMT}/I_{LMT,BOT}$	$I_{LMT,BOT}$ >5A	9	10	11	µA/A
Discharge FET Resistance		R_{DIS}			120		Ω
Enable (EN)	Rising Threshold	$V_{EN,R}$		1.18	1.23	1.28	V
	Threshold Hysteresis	$V_{EN,HYS}$			0.2		V
	Input Current	I_{EN}	V_{EN}=2V		0		µA
Soft Start (SS)	Charging current	I_{SS1}	V_{SS}=0V		46		µA
	Discharge current	I_{SS2}	V_{SS}=1V		38		mA
	Min soft-start time	$t_{SS,MIN}$			1		ms
Overvoltage Protection Threshold		V_{OVP}		110	120	130	%V_{FBS}
Undervoltage Protection	threshold	V_{UVP}		47	52	57	
	Delay	$t_{UVP,DLY}$			20		µs
UVP/OCP Hiccup ON Time		$t_{HICCUP,ON}$	C_{SS} open		3		ms
UVP/OCP Hiccup OFF Time		$t_{HICCUP,OFF}$			12		
Power Good	Thresholds	V_{PG}	V_{FBS} falling, fault	77	81	85	%V_{FBS}
			V_{FBS} rising, good	88.5	92.5	96.5	
			V_{FBS} rising, fault	110	120	130	
			V_{FBS} falling, good	102	106	110	
	Delay	$t_{PG,R}$	V_{FBS} falling, good		0.8		ms
		$t_{PG,F}$	V_{FBS} rising, fault		20		
	Output low voltage	$V_{PG,LOW}$	V_{IN}=0V, 100kΩ from PG to 3.3V		550	750	V
			V_{IN}=0V, 10kΩ from PG to 3.3V		660	850	
			V_{EN} = 2V, V_{FBS} = 0V, I_{PG}=10mA			0.4	
	Output low leakage	$I_{PG,LKG}$	V_{PG} = 3.3V		3	5	µA

Electrical Characteristics (cont.) V_{IN} = 12V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise specified (4)						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Switching Frequency	f_{SW}	R_{MODE}=0Ω, I_{OUT}=0A, FCCM, V_{OUT}=1V, T_J=25°C	510	600	690	kHz
		R_{MODE}=30.1kΩ, I_{OUT}=0A, FCCM, V_{OUT}=1V, T_J=25°C	690	800	910	
		R_{MODE}=60.4kΩ, IOUT=0A, FCCM, V_{OUT}=1V, TJ=25°C	900	1000	1100	
Min ON Time	$t_{ON,MIN}$	I_{OUT}=3A (Note 4)		60		ns
Min OFF Time	$t_{OFF,MIN}$	I_{OUT}=3A (Note 4)		180		
Thermal Shutdown Temperature	T_{SD}			160		˚C
Thermal Shutdown Hysteresis	T_{HYS}	(Note 4)		30		

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

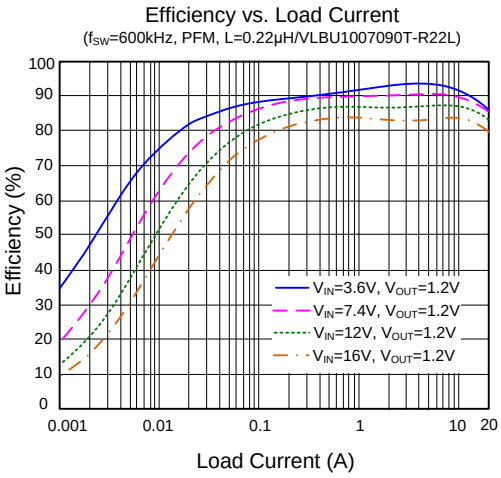
Note2: Package thermal resistance is measured in the natural convection at T_A=25˚C on a 8.5cm×8.5cm size four-layer Silergy Evaluation Board.

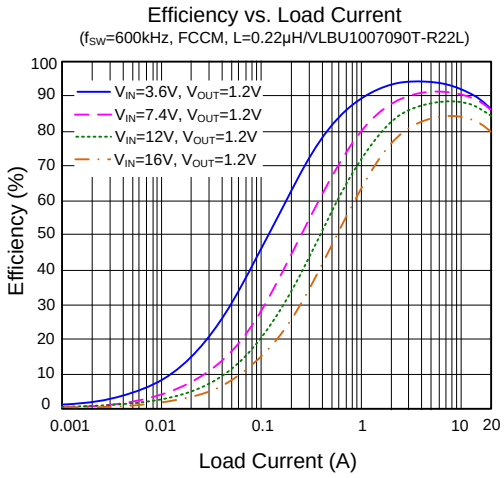
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Production testing is performed at 25˚C; limits at -40°C to +125°C are guaranteed by design, test or statistical correlation.

Typical Performance Characteristics

(T_A=25°C, V_{IN}=12V, V_{OUT}=1.2V, L=0.22µH, C_{OUT}=235µF, f_{SW}=600kHz, R_{ILMT}=5.6kΩ, C_{SS}=0.22µF, unless otherwise noted)

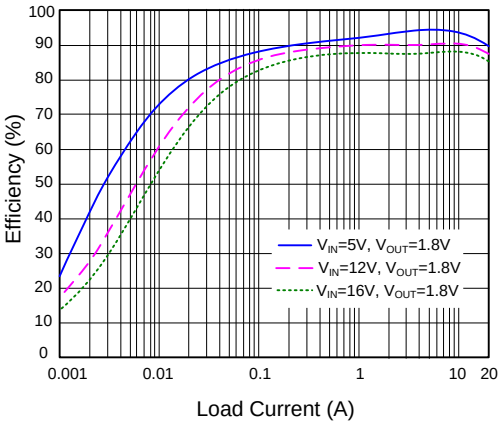




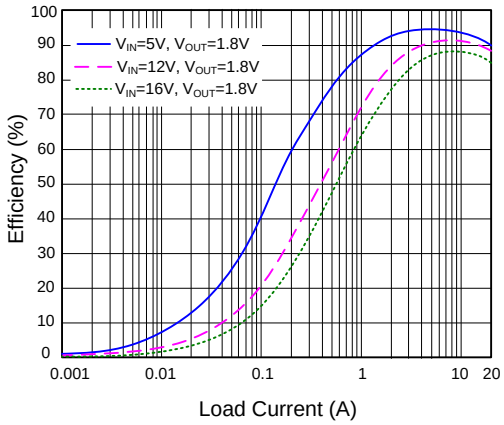
Typical Performance Characteristics (cont.)

(T_A=25°C, V_{IN}=12V, V_{OUT}=1.2V, L=0.22µH, C_{OUT}=235µF, f_{SW}=600kHz, R_{ILMT}=5.6kΩ, C_{SS}=0.22µF, unless otherwise noted)

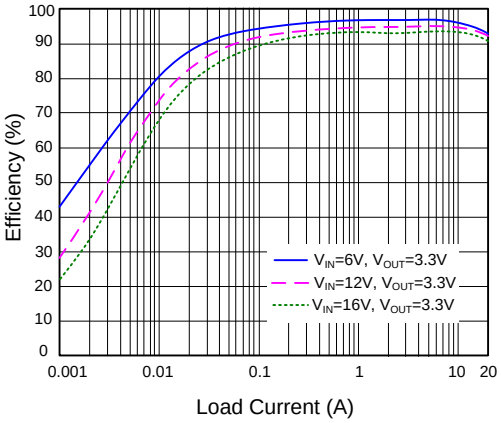
Efficiency vs. Load Current
(f_{SW}=600kHz, PFM, L=0.22µH/VLBU1007090T-R22L)



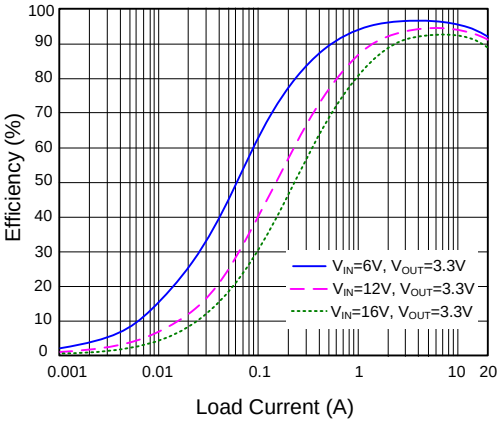
Efficiency vs. Load Current
(f_{SW}=600kHz, FCCM, L=0.22µH/VLBU1007090T-R22L)



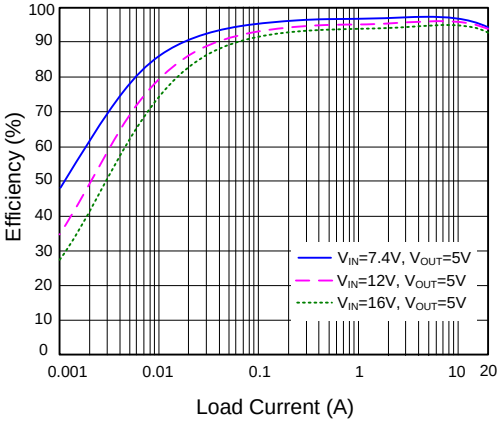
Efficiency vs. Load Current
(f_{SW}=600kHz, PFM, L=0.56µH/FCUL1060-H-R56M=P3)



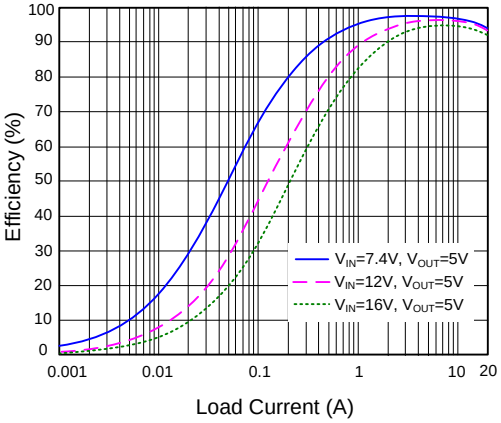
Efficiency vs. Load Current
(f_{SW}=600kHz, FCCM, L=0.56µH/FCUL1060-H-R56M=P3)



Efficiency vs. Load Current
(f_{SW}=600kHz, PFM, L=0.56µH/FCUL1060-H-R56M=P3)



Efficiency vs. Load Current
(f_{SW}=600kHz, FCCM, L=0.56µH/FCUL1060-H-R56M=P3)

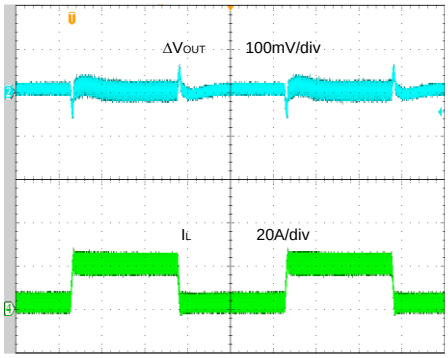


Typical Performance Characteristics (cont.)

(T_A=25°C, V_{IN}=12V, V_{OUT}=1.2V, L=0.22µH, C_{OUT}=235µF, f_{SW}=600kHz, R_{ILMT}=5.6kΩ, C_{SS}=0.22µF, unless otherwise noted)

Load Transient

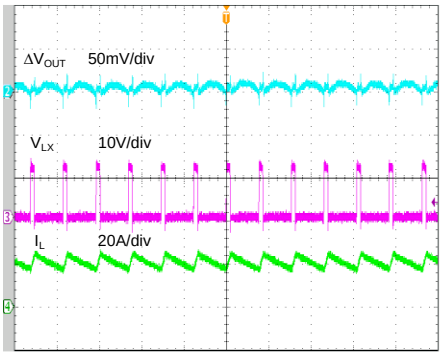
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=2~20A, FCCM)



Time (200µs/div)

Output Ripple

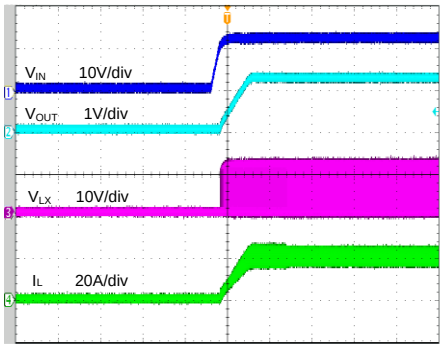
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=20A)



Time (2µs/div)

Startup from V_{IN}

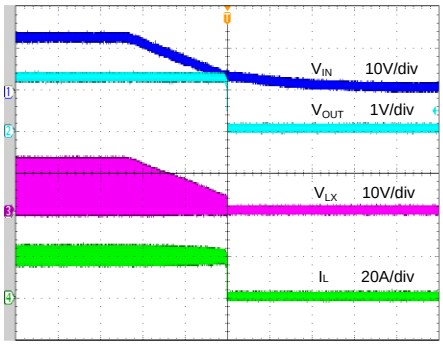
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=20A)



Time (4ms/div)

Shutdown from V_{IN}

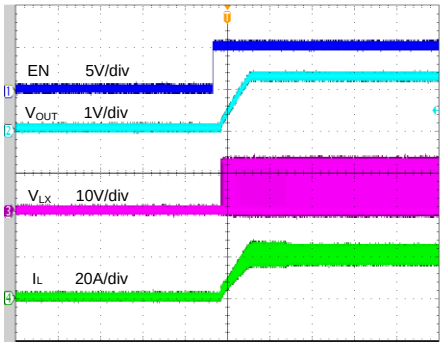
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=20A)



Time (4ms/div)

Startup from EN

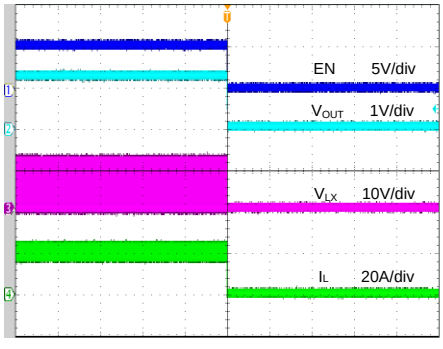
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=20A)



Time (4ms/div)

Shutdown from EN

(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=20A)



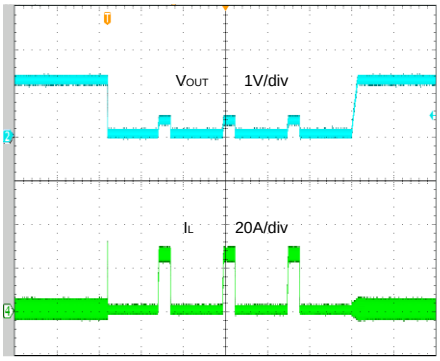
Time (4ms/div)

Typical Performance Characteristics (cont.)

(T_A=25°C, V_{IN}=12V, V_{OUT}=1.2V, L=0.22µH, C_{OUT}=235µF, f_{SW}=600kHz, R_{ILMT}=5.6kΩ, C_{SS}=0.22µF, unless otherwise noted)

Short Circuit Protection

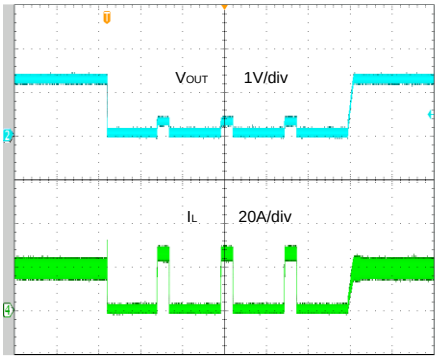
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0A~short, R_{ILMT}=5.6kΩ, FCCM)



Time (20ms/div)

Short Circuit Protection

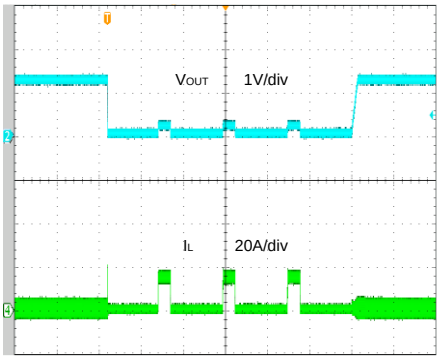
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=20A~short, R_{ILMT}=5.6kΩ)



Time (20ms/div)

Short Circuit Protection

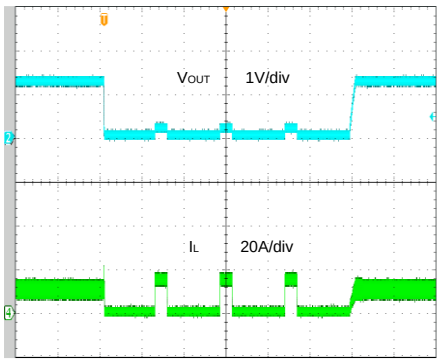
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0A~short, R_{ILMT}=10kΩ, FCCM)



Time (20ms/div)

Short Circuit Protection

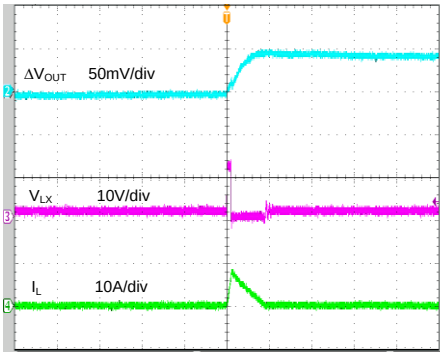
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=10A~short, R_{ILMT}=10kΩ)



Time (20ms/div)

Output Ripple

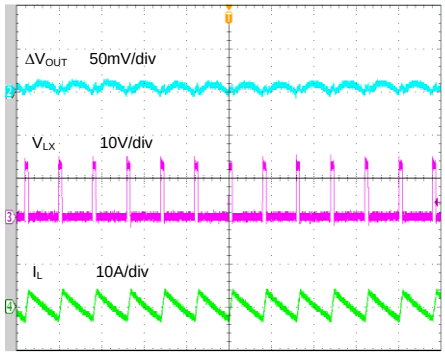
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0A, PFM)



Time (2µs/div)

Output Ripple

(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0A, FCCM)



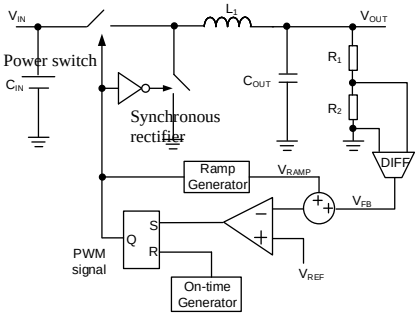
Time (2µs/div)

Detailed Description

Constant-on-time Architecture

Fundamental to any constant-on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the high-side power switch. Each on-time (t_{ON}) is a "fixed" period internally calculated to operate the regulator at the desired switching frequency over the input and output voltage range, where $t_{ON}=(V_{OUT}/V_{IN})\times(1/f_{SW})$. For example, consider a hypothetical converter configured for 1.2V output from a 12V input operating at 600kHz. The target on-time is (1.2V/12V)×(1/600kHz)=167ns. Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at FB drops below the target value. As the input or output voltages change, an appropriate t_{ON} pulse is calculated, maintaining a fairly constant operating frequency while regulating the output voltage. In a COT architecture, there is no fixed clock, so the power switch can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays. COT has significant benefits over traditional current mode or voltage mode control methods that must simultaneously monitor the feedback voltage, inductor current and compensation signals to determine when to turn off the power switch and turn on the synchronous rectifier.

Instant-PWM Operation



Silergy's Instant-PWM control method adds several proprietary improvements to traditional COT architecture. Whereas most legacy COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, Instant-PWM derives this signal internally. Another improvement optimizes operation when used with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT regulators may become unstable when used with these output capacitors.

Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for small duty cycle, since at very low duty cycle operation, once the on-time is close to the minimum on time, the switching frequency can be reduced as needed to always ensure a proper operation.

Under T_J=-40℃ ~125℃ condition, the device can support up to 5.5V output even the input voltage is as low as 8V.

Frequency Locked Loop (FLL)

When operating conditions include changes in input voltage and/or output loads, the COT operating frequency will naturally vary from the ideal. Silergy's FLL technology minimizes this variation by comparing the actual operating frequency with the desired frequency. The FLL block adjusts the calculated t_{ON} period to lock the operating frequency to the onboard reference oscillator. The FLL function is disabled during soft-start and discontinuous current mode (DCM) operating condition. Note that FLL does not impede the high frequency retriggering of the power switch during load transients.

Operating Frequency/Light Load Settings

The MODE pin sets both the operating frequency and the light load behavior of the device. This pin is sampled when the device is enabled and the operating modes are set when the internal regulator (Vcc) rises above $V_{VCC,UVLO.}$ The mode is locked until the device is restarted.

MODE Pin connection	Light-Load operation	Operating Frequency
VCC	PFM	600kHz
240kΩ* to GND	PFM	800kHz
120kΩ* to GND	PFM	1000kHz
GND	FCCM	600kHz
30kΩ* to GND	FCCM	800kHz
60kΩ* to GND *±20%	FCCM	1000kHz

Table 1

Under medium to heavy loads, the inductor current, even at the lowest point just before each t_{ON} pulse, is always positive. This is known as continuous conduction mode (CCM). At lower load currents, when $I_{OUT} \sim < 1/2\times\Delta I_{L,}$ the current through the inductor will ramp to near zero before the next t_{ON} pulse. The behavior of the device in this condition may be set to pulse frequency modulation (PFM) to optimize efficiency, or to forced continuous conduction mode (FCCM) which maintains a fixed operating frequency.

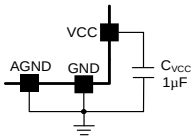
When operating in PFM under light load conditions, the synchronous rectifier will turn off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, and while the feedback is greater than the reference voltage, the control loop will not trigger another t_{ON} until needed, lowering the operating frequency, further enhancing efficiency. Fixed frequency CCM resumes smoothly as soon as the load current increases sufficiently for the inductor current to

remain positive throughout the cycle. PFM operation should not be selected if the application is sensitive to frequencies lower than the selected operating frequency, including audible frequencies.

In FCCM operation under light loads, the synchronous rectifier remains on even when the inductor current crosses zero. Current flow will continue until the next t_{ON} cycle. In this way, the device always operates in CCM and keeps a relatively constant switching frequency over the entire output current range.

Linear Regulator (VCC)

An internal linear regulator produces a 3.3V supply at VCC from IN. VCC powers the internal gate drivers, PWM logic, analog circuitry, and other blocks. Connect a 1µF (minimum) low ESR ceramic capacitor from VCC to GND. Note that an external bias supply may be used to drive VCC in the range specified by $V_{CC,EXT}$. Care should be taken to ensure that the bias supply draws no current from the VCC linear regulator.

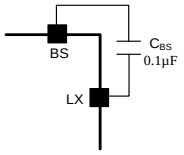


Under Voltage Lock-out

To prevent operation before all internal circuitry is ready and to ensure that the power and synchronous rectifier switches can be sufficiently enhanced, this device includes under-voltage lockout protection at IN and VCC. The device remains in a low current state and all switching actions are inhibited until IN exceeds $V_{IN,UVLO}$ and VCC exceeds $V_{IN,UVLO}$. At that time, if EN is enabled, the device will start-up by initiating a soft-start ramp. If IN or VCC fall below their respective UVLO falling thresholds, the device will be disabled.

External Bootstrap Capacitor (BS)

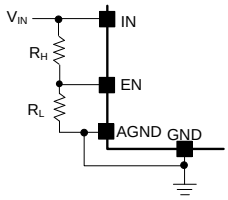
This device integrates a floating power supply for the gate driver that operates the power switch. Proper operation requires a 0.1µF low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel power MOSFET switch.



Enable Control (EN)

EN is a high-voltage capable input with a stable, logic-compatible threshold that provides convenient control of device start-up behavior such as automatic, delayed or logic-controlled starts. The accurate threshold is useful to inhibit operation until a specific IN voltage is reached.

When EN is < 0.4V the internal linear regulator that drives VCC and most internal circuitry is turned off, disabling the device. Driving EN above $V_{EN,R}$ initiates a startup sequence as the device is enabled.



For automatic start-up, connect EN to IN through resistor R_H. If power supply sequencing is required, similarly connect EN to the output of the power rail that should start first. R_H should be 1kΩ to 1MΩ.

Note that when enabling the device via EN, two thresholds will be observed. First, at ~0.8V, the internal linear regulator that drives VCC will be enabled and, assuming sufficient voltage at IN, VCC will rise. Second, as EN is driven above $V_{EN,R}$ (1.23V nom) a startup sequence will be enabled. If EN falls $V_{EN,HYS}$ below $V_{EN,R}$ (1.03V nom) switching regulation will be disabled.

Differential Remote Sense (FBS, GNDS)

FBS and GNDS may be used as a differential feedback connection directly to the output capacitor or main load connection. This helps to compensate for DC losses in the PCB at high output currents. Keep these connections short and direct. If remote sense is not required, connect GNDS directly to AGND. GNDS must be within +/-0.2V of GND and AGND.

Power Good (PG)

The power good indicator is an open drain output controlled by a window comparator connected to the internal feedback signal V_{FB}. PG will be high impedance during normal device operation when V_{FBS} is within a range of V_{REF} x 0.925 to V_{REF} x 1.05 (nom) for at least $t_{PG,R}$. Once within this range and to prevent a false fault indication, PG will remain high impedance unless V_{FB} falls below V_{REF}*0.80 or exceeds V_{REF} x 1.20 (nom) for $t_{PG,F}$.

PG is held low during start up, when the device is disabled and during an over-temperature protection (OTP) fault condition (see OTP). PG should be pulled up to a 3.3V (nom) or lower logic supply through a resistor in the range 10kΩ~100kΩ. PG will remain low even if VCC is 0V.

Programmable Soft-start Time (SS)

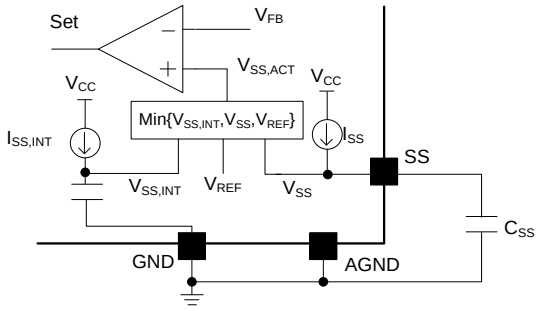
A soft-start circuit is incorporated to smoothly ramp the output to the desired voltage whenever the device is enabled.

At startup, soft-start clamps the output at a low voltage and then ramps the output to the desired voltage over the soft-start time t_{SS}, which avoids high current flow and transients during startup. The default t_{SS} is ~1mS. Longer t_{SS} may be achieved by connecting a capacitor C_{SS} from SS to AGND.

$$t_{SS}(ms)=\frac{C_{SS}(nF)\times V_{REF}}{I_{SS}(\mu A)}$$

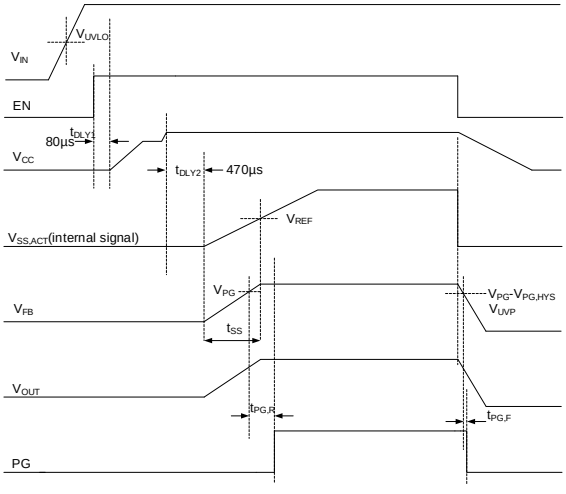
(where I_{SS} is ~46μA, V_{REF} is 0.6V)

Selecting C_{SS} = 150nF would set t_{SS} ~ 2ms. C_{SS} is not required if the default t_{SS} of ~ 1ms is adequate for the application.



Startup and Shutdown sequence

If IN exceeds $V_{IN,UVLO,}$ normal startup can be initiated by bringing EN high, or by pulling EN high from V_{IN}. After a short delay, t_{DLY1}, the internal VCC LDO is turned on to power the internal control circuits. Once VCC is up and after another short delay, $t_{DLY2,}$ the soft-start signal V_{ss} ramps and normal switching action begins. The output voltage V_{OUT} ramps up and once the output voltage is 92.5% of the regulation point, PG becomes high-impedance after a delay time $t_{PG,R}$.



Pre-biased operation

If the output is not at 0V at startup, it is considered pre-biased. In this case, the power switch and synchronous rectifiers will not begin switching until the soft-start ramp $V_{SS,ACT}$ exceeds the sensed output voltage V_{FBS}.

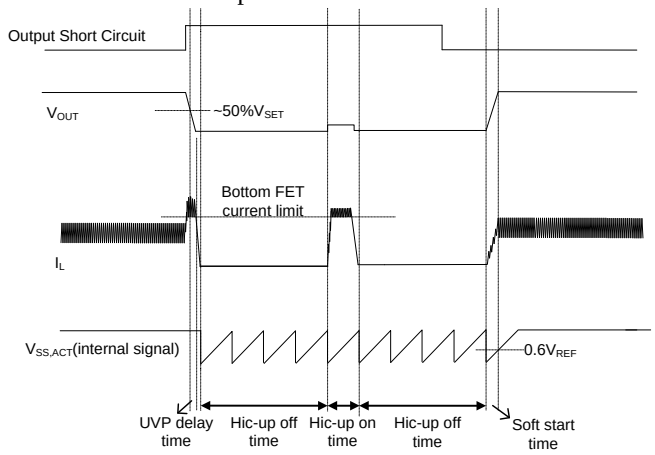
Output Discharge

The output is actively discharged when the converter is shut down by EN, UVLO or OTP. Typically 120Ω, the discharge FET parallels the synchronous rectifier and pulls LX low to discharges the output through the inductor.

Fault Protections

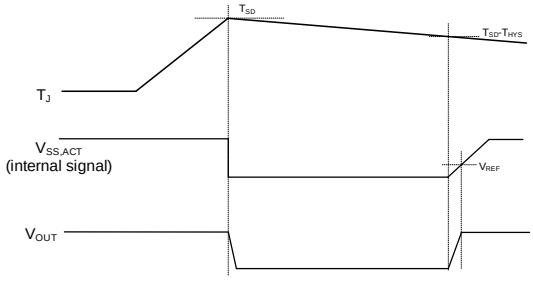
Output Under Voltage Protection (UVP)

If a fault condition, such as a short circuit at the output, brings V_{FBS} < ~50% of the set point for $t_{UVP,DLY}$, UVP will be triggered and switching will be disabled for $t_{HICCUP,OFF}$. Switching will resume for $t_{HICCUP,ON}$ and this cycle will repeat. If the output fault conditions are removed, the device will return to normal operation.



Over Temperature Protection (OTP)

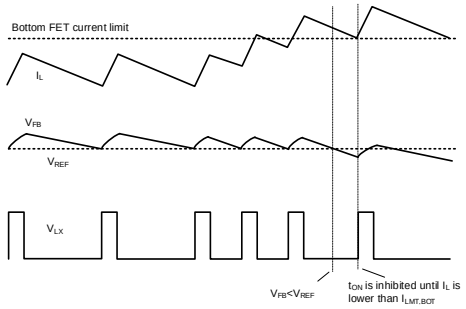
OTP includes circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 160°C. Once the junction temperature cools down by approximately 30°C, the device will resume normal operation with a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.



Valley Current Limit Protection (OCP)

Inductor current is measured in the synchronous rectifier on every cycle when it turns on and as the inductor current

ramps down. If the current exceeds $I_{LMT,BOT}$, the next t_{ON} is inhibited until the current returns back to safe levels.



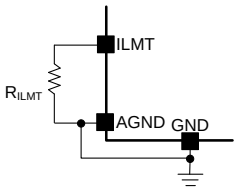
This limits the inductor current and, because the output current is higher, the output voltage naturally falls. Switching will resume once the inductor current is below the valley current limit.

Valley current limit is programmable by connecting a resistor R_{ILMT} from ILMT to AGND. The valley current limit equation is

$$I_{BOT,LMT} = \frac{V_{ILMT}}{G_{MIRROR} \times R_{ILMT}(\Omega)}$$

Where, V_{ILMT} is 1.2V, and the synchronous rectifier mirror ratio G_{MIRROR} is 10μA/A typically.

Note that OCP may not prevent UVP or OTP from triggering a latch off protection of the device.



Peak Current Limit Protection

The device also features cycle-by-cycle "peak" current limit for the power switch. During t_{ON} time, the power switch current is monitored. If the monitored current exceeds $I_{LMT,HS}$ the power switch is turned off before the end of the t_{ON} time.

Reverse Current Limit

A cycle-by-cycle "reverse" current limit protects the synchronous rectifier from excessive negative current in FCCM or PFM OQDM. If $I_{LMT,RVS}$ is exceeded, the synchronous rectifier is turned off, and a t_{ON} pulse is triggered. Reverse current sampling occurs ~60ns ($t_{RCL,BLK}$) after a t_{ON} pulse to reduce false triggering.

Output Over Voltage Protection (OVP)

This device includes output over voltage protection (OVP). If V_{FBS} rises above the feedback regulation level but below V_{OVP}, PFM / FCCM settings determine the behavior. In FCCM, the synchronous rectifier will be turned on and will remain on for most of the cycle, except for t_{ON} minimum pulses of $t_{ON,MIN}$. In PFM, the synchronous rectifier will remain on only until the inductor current reaches zero. Further switching is inhibited. If VFBS exceeds $V_{OVP,}$ OQDM is activated.

See Inductor Design regarding proper inductor value selection. Under light loads false OVP triggering is possible if the inductor is too small. This may also cause the reverse current limiting.

Output Quick Discharging Mode (OQDM)

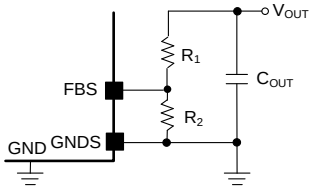
When operating in PFM under light load conditions, if FBS is driven above V_{OVP} for more than ~20μs, OQDM will be activated. This changes the operating mode to FCCM. The synchronous rectifier is turned on at a very high duty factor to discharge the output as quickly as possible. This will continue until the inductor current becomes positive and V_{FBS} is below V_{OVP}. Note that OQDM may not prevent UVP or OTP from triggering a latch off protection of the device.

Design Procedure

Feedback Resistor Selection

Choose R_1 and R_2 to program the proper output voltage. Locate these resistors very close to FBS, which is noise sensitive. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is strongly recommended for both resistors. For V_{OUT} = 1.2V, R_1=100kΩ is chosen, then using following equation, R_2 can be calculated to be 100kΩ.

$$R_2 = \frac{0.6V}{V_{SET} - 0.6V} \times R_1$$



Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R or X7R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to

reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) can be helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current,

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, therefore

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

In addition, the input capacitor determines the input voltage ripple. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1\text{-}D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications two 22µF X5R capacitors are sufficient. Take care to locate the ceramic input capacitor as close to the device IN and GND pins as possible.

Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage.

Instant-PWM operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost and size for the application. A low inductance will help reduce the inductor size and cost, and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low value inductors may help reduce DC losses and increase efficiency. On the other hand, higher inductor values tend to be larger have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) about 20% ~ 50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$) and estimating a ΔI_L as some percentage of that current.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

and

$$I_{L,PEAK} = I_{OUT,MAX} + \Delta I_L/2$$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

If FCCM light load operation is selected, be sure to select an inductor value high enough to avoid the reverse current limit from being triggered when the load current is near zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Low loss ferrite materials should be considered.

Inductor Design Example

Consider a typical design for a device providing $1.2V_{OUT}$ at 20A from $12V_{IN}$, operating at 600kHz and using a target inductor ripple current (ΔI_L) of 50% or 10A. Determine the approximate inductance value at first:

$$L_1 = \frac{1.2V \times (12V - 1.2V)}{12V \times 600kHz \times 10A} = 0.18\mu H$$

Next, select the nearest standard inductance value, in this case 0.22µH, and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{1.2V \times (12V - 1.2V)}{12V \times 600kHz \times 0.22\mu H} = 8.18A$$

and

$$I_{L,PEAK} = 20A + 8.18A/2 = 24.09A$$

The resulting 8.18A ripple current of 8.18A/20A is ~40.9%, well within the 20% ~ 50% target. Importantly, it is also well below the reverse current limit

$$I_{L,PEAK,RVS} = 8.18A/2 = 4.09A < I_{LIM,RVS}$$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 24.09A.

Output Capacitor Selection

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Output Ripple

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) and the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 8.18A using five 47µF ceramic capacitors, each with an ESR of ~5mΩ for parallel total of 235µF and 1mΩ ESR.

$$V_{RIPPLE,ESR} = 8.18A \times 1m\Omega = 8.18mV$$

$$V_{RIPPLE,CAP} = \frac{8.18A}{8 \times 235\mu F \times 600kHz} = 7.25mV$$

Total ripple = 15.43mV. The actual capacitive ripple may be higher than calculated value because the capacitance decreases with the bias voltage on the capacitor. Check the capacitor derating curves.

This same example using one 150µF 40mΩ POS cap.

$$V_{RIPPLE,ESR} = 8.18A \times 40m\Omega = 327.20mV$$

$$V_{RIPPLE,CAP} = \frac{8.18A}{8 \times 150\mu F \times 600kHz} = 11.36mV$$

Total ripple =338.56mV

Output Transient Undershoot/Overshoot

If very fast load transients must be supported, consider the effect of the output capacitor on output transient undershoot and overshoot. Instant-PWM responds quickly to dynamic load conditions, however, some consideration to the output capacitor is necessary, especially when using small ceramic capacitors which have low capacitance at low output voltages which results in insufficient stored energy for load transient. Output transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor and voltage changes caused by the combination of output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as $V_{ESR} = \Delta I_{OUT} \times ESR$. Using the ceramic capacitor example above and a fast load transient of +/- 10A, V_{ESR} = +/- 10A × 1mΩ = +/- 10mV. The POS capacitor result with the same load transient, V_{ESR} = +/- 10A × 40mΩ = +/- 400mV.

Capacitive undershoot (load increasing) is a function of the output capacitance, the load step, the inductor value, the input-output voltage difference and the maximum duty factor. During a fast load transient, the maximum duty factor of instant-PWM is a function of t_{ON} and the minimum t_{OFF} as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{ON} pulses in this case. The maximum duty factor D_{MAX} may be calculated by

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated by

$$V_{UNDERSHOOT,CAP} = -\frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 10A load increase using the ceramic capacitor example. With V_{IN} = 12V.At V_{OUT} = 1.2V, the result is t_{ON} = 167ns, $t_{OFF,MIN}$ = 180ns, D_{MAX} = 167 / (167 + 180) = 0.481 and

$$V_{UNDERSHOOT,CAP} = -\frac{0.22\mu H \times (10A)^2}{2 \times 235\mu F \times (12V \times 0.481 - 1.2V)} = -10.23mV$$

Using the POS capacitor example, the result is

$$V_{UNDERSHOOT,CAP} = -\frac{0.22\mu H \times (10A)^2}{2 \times 150\mu F \times (12V \times 0.481 - 1.2V)} = -16.04mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage.

$$V_{OVERSHOOT,CAP} = \frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 10A load decrease using the ceramic capacitor example. At V_{OUT} = 1.2V the result is

$$V_{OVERSHOOT,CAP} = \frac{0.22\mu H \times (10A)^2}{2 \times 235\mu F \times 1.2V} = 39.01mV$$

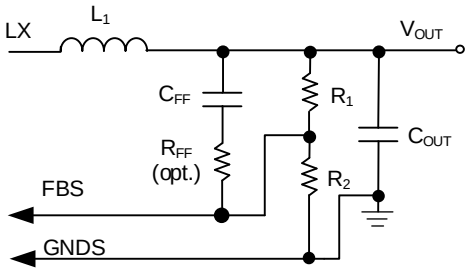
Using the POS capacitor example, the above result is

$$V_{OVERSHOOT,CAP} = \frac{0.22\mu H \times (10A)^2}{2 \times 150\mu F \times 1.2V} = 61.11mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application.

Load Transient Consideration

Although the device is internally compensated and optimized for low duty cycle applications, in applications with high step load current, adding an RC feed-forward compensation network R_{FF} and C_{FF} may further speed up the load transient response. R_{FF} = 1kΩ and C_{FF} = 220pF have been shown to perform well in most applications. Increase C_{FF} will speed up the load transient response but will require verification that no stability issues result.



Note that when C_{OUT} > 500µF and minimum load current is low, set feed-forward values as R_{FF} = 1kΩ and C_{FF} > 2.2nF to provide for sufficient ripple signal to V_{FBS} for small output ripple and good transient behavior.

Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the IC package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by:

$$P_{D,MAX} = (T_{J,MAX} - T_A) / \theta_{JA}$$

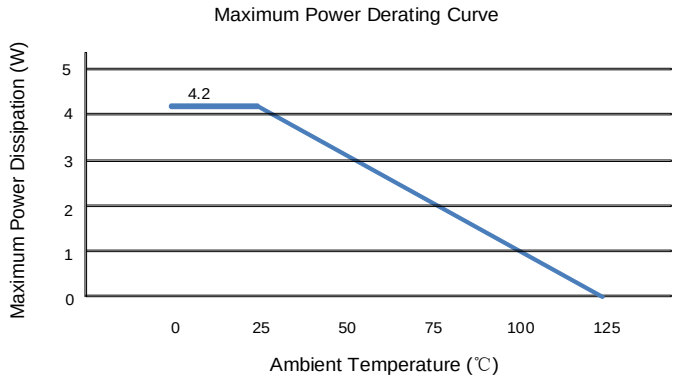
where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

The recommended operating conditions include a maximum junction temperature of 125℃. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the QFN3×4-19 package the thermal resistance θ_{JA} is 24℃/W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz. copper traces connected to each IC pin and very large, unbroken 1-oz. internal power and ground planes. Good thermal performance requires wide copper traces at all the pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A=25℃ may be calculated by the following formula:

$$P_{D,MAX} = (125℃ - 25℃) / (24℃/W) = 4.2W$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.



Layout Design

Follow these PCB layout guidelines for optimal performance and good thermal dissipation.

Input Capacitors: Place the input capacitor very near IN and GND, minimizing the loop formed by these connections. And the input capacitor should be connected to the IN and GND by wide copper plane. Place one smaller package input MLCC capacitor at the reach out port of pin18. This capacitor can be connected with GND by vias.

Output Capacitors: Guarantee the C_{OUT} negative sides are connected with GND pin by wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.

VCC Capacitor: Place the VCC capacitor close to VCC using short, direct copper trace to one nearest device GND pin.

AGND Layout: Make one Kelvin connection between AGND and GND at the C_{VCC} negative sides. C_{SS}, R_{MODE}, R_{ILMT} should connect to AGND using short, direct copper trace.

Feedback Network: Place the feedback components (R_1, R_2, R_{FF} and C_{FF}) as close to FBS pin as possible. Avoid routing the remote output sense line and remote GND sense (GNDS) line near LX, BS or other high frequency signal as they are noise sensitive. Make the feedback sampling point Kelvin connect with COUT rather than the inductor output terminal.

LX Connection: The LX connection has large voltage swings and fast edges and can easily radiate noise to adjacent components. Keep its area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance. Keep sensitive components away from the switching node or provide ground traces between for shielding, to prevent stray capacitive noise pickup.

BS Capacitor: Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX and C_{BS}) as short as possible.

Control Signals: It is not recommended to connect control signals and IN directly. A resistor in a range of 1kΩ to 1MΩ should be used if they are pulled high by IN.

GND Vias: Place adequate number of vias on the GND layer around the device for better thermal performance.

PCB Board: A four-layer layout with 2-oz copper is strongly recommended to achieve better thermal performance. The top layer and bottom layer should place power IN and GND copper plane as wide as possible. Middle1 layer should place all GND layer for conducting heat and shielding middle2 layer signal line from top layer crosstalk. Place signal lines on middle2 layer instead of the other layers, so that the other layers' GND plane not be cut apart by these signal lines.

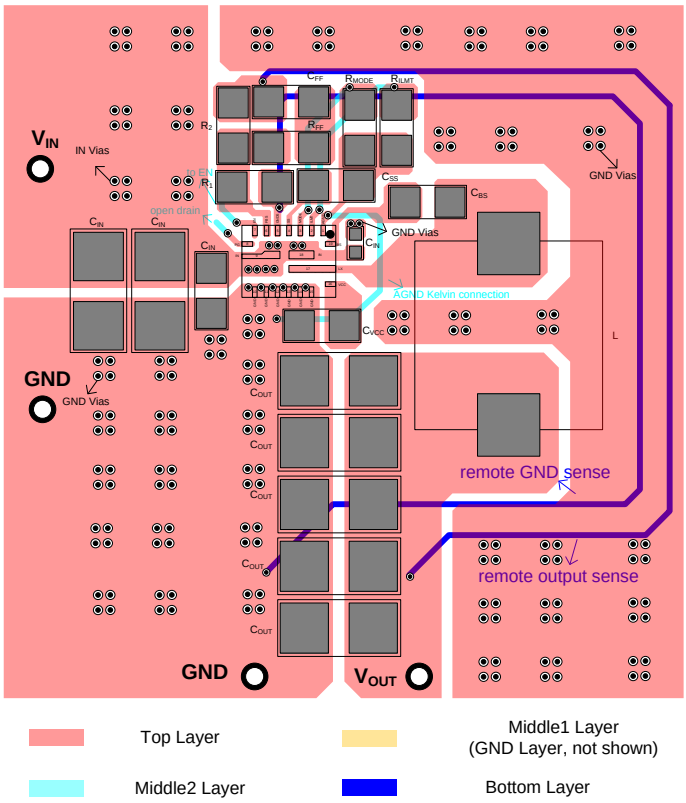
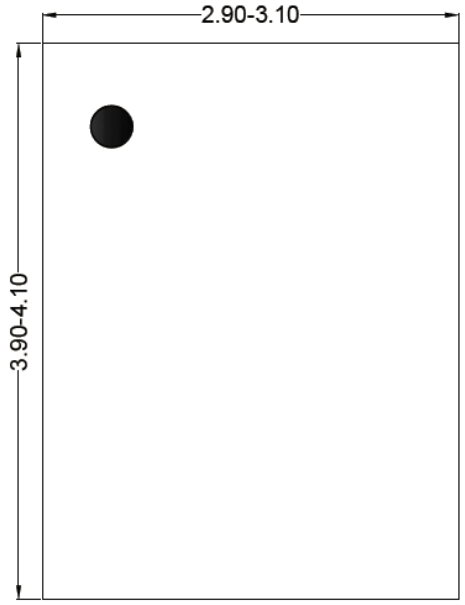
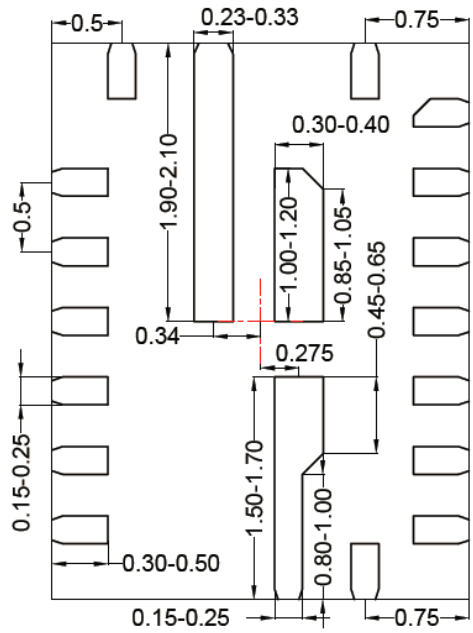


Figure 4. PCB Layout Suggestion

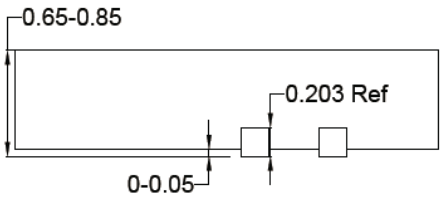
QFN3×4-19 Package Outline Drawing



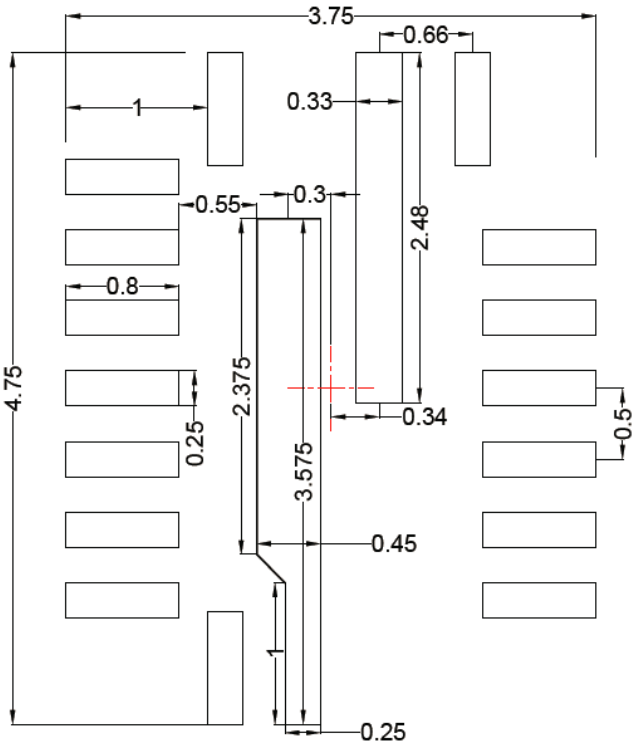
Top view



Bottom view



Front view

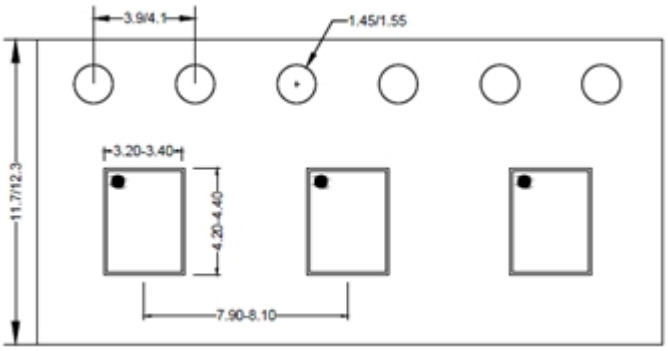


Recommended PCB layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr. Center line refers chip body center.

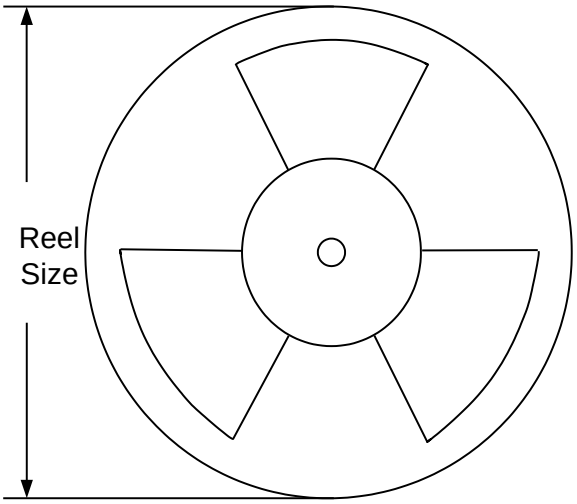
Taping & Reel Specification

1. Package orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel
QFN3×4	**12**	**8**	**13"**	**400**	**400**	**5000**

Revision History

Revision Number	Revision Date	Description	Pages changed
0.0	04/17/2020	Initial draft	-
0.0A	07/28/2020	1. The max. input voltage changes from 18V to 16V; 2. Update the Absolute Maximum Ratings 3. Add efficiency curves for PFM Mode; 4. Update the Detailed Description. a) Add Minimum Duty Cycle and Maximum Duty Cycle (page9); b) Update the diagrammatic drawing in UVP description (page11); c) Update the Layout Design (page15)	Page3 Page 5~6 Page9~15
0.9	12/16/2020	Update the Output UVP Threshold/ Power Good Threshold in EC table	Page 4

Revision history is for reference only and may not be comprehensive or complete.

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