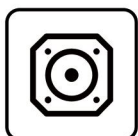


自主封測 品質把控 售後保障

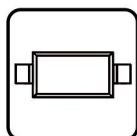
WEB | WWW.TDSEMIC.COM



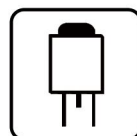
電源管理



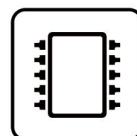
顯示驅動



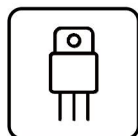
二三極管



LDO穩壓器



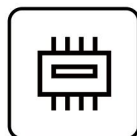
觸摸芯片



MOS管



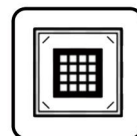
運算放大器



存儲芯片



MCU



串口通信

74HC165D-TD

產品規格說明書

1. DESCRIPTION

The **74HC165** is an 8-bit parallel-load shift register that, when clocked, shifts the data toward a serial (Q_H) output. Parallel-in access to each stage is provided by eight individual direct data (A-H) inputs that are enabled by a low level at shift/load ($SH/\overline{LD}$) input. The 74HC165 also features a clock-inhibit (CLK INH) function and a complementary serial ($\overline{Q_H}$) output.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while $SH/\overline{LD}$ is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when $SH/\overline{LD}$ is held high. While $SH/\overline{LD}$ is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

2. FEATURES

- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

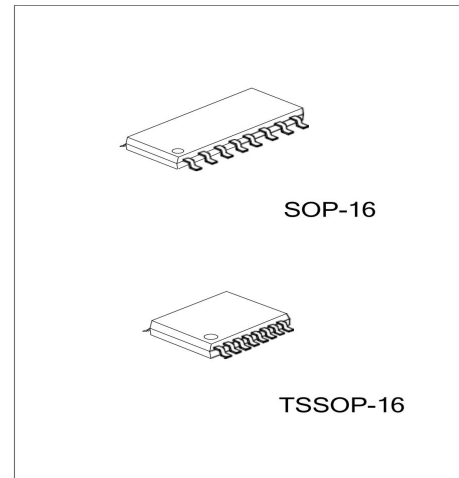
3. ORDERING INFORMATION

• Tube

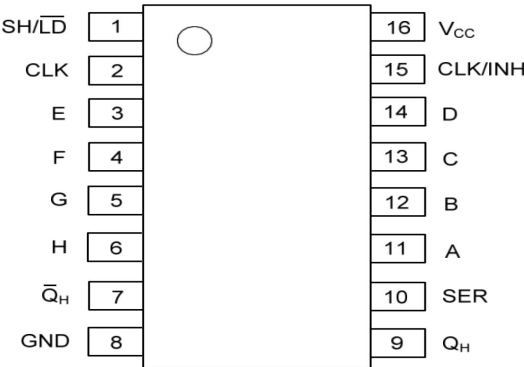
Part Number	Marking code	Package	Packing	Pcs/Tube	Pcs/Box
74HC165N	74HC165	SOP-16	Tube	50	10K

• Tape Reel

Part Number	Marking code	Package	Packing	Pcs/Reel	Pcs/ Box
74HC165D	74HC165	SOP-16	Tape Reel	4K	64K
74HC165T-R	74HC165	TSSOP-16	Tape Reel	5K	80K



4. PIN CONFIGURATION



5. PIN DESCRIPTION

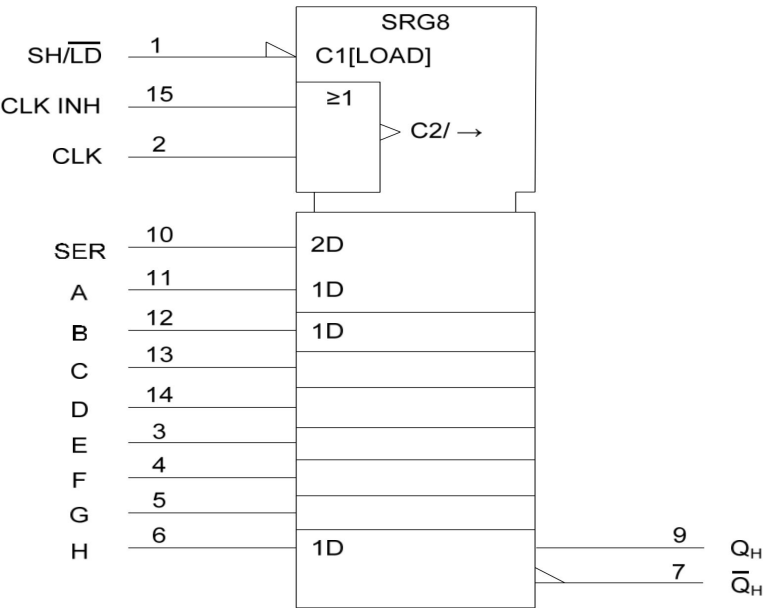
PIN NO.	PIN NAME	DESCRIPTION
1	SH/ $\overline{\text{LD}}$	Asynchronous parallel load input (active LOW)
2	CLK	Clock input (LOW-to-HIGH edge-triggered)
3, 4, 5, 6 11, 12, 13, 14	A to H	Parallel data inputs (also referred to as Dn)
7	$\overline{\text{QH}}$	Complementary output from the last stage
8	GND	Ground (0V)
9	QH	Serial output from the last stage
10	SER	Serial data input
15	CLK/INH	Clock enable input (active LOW)
16	V _{CC}	Positive supply voltage

6. FUNCTION TABLE

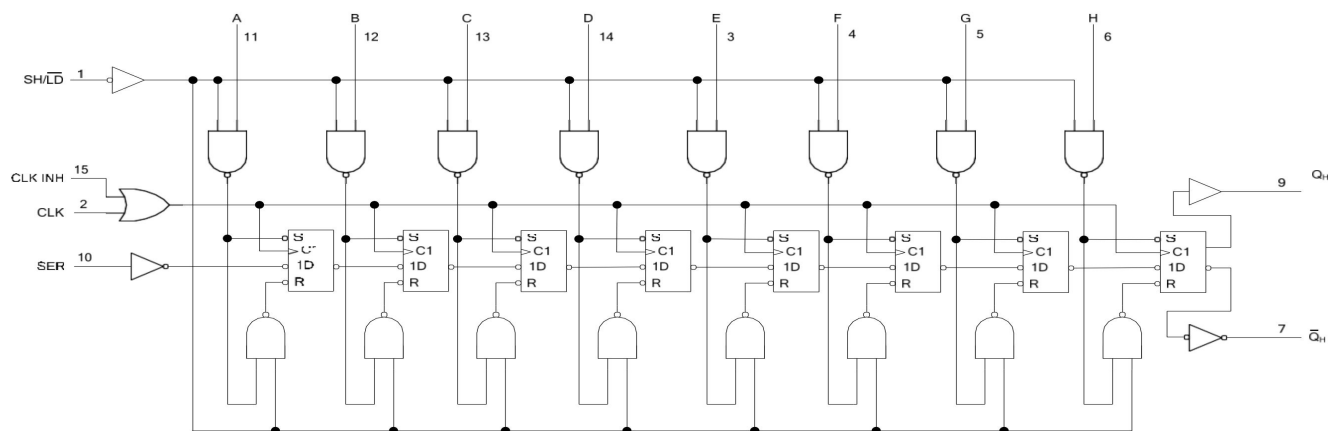
INPUTS			FUNCTION
SH/ $\overline{\text{LD}}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift↑
H	↑	L	Shift↑

↑ Shift=content of each internal register shifts toward serial output Q_H. Data at SER is shifted into the first register.

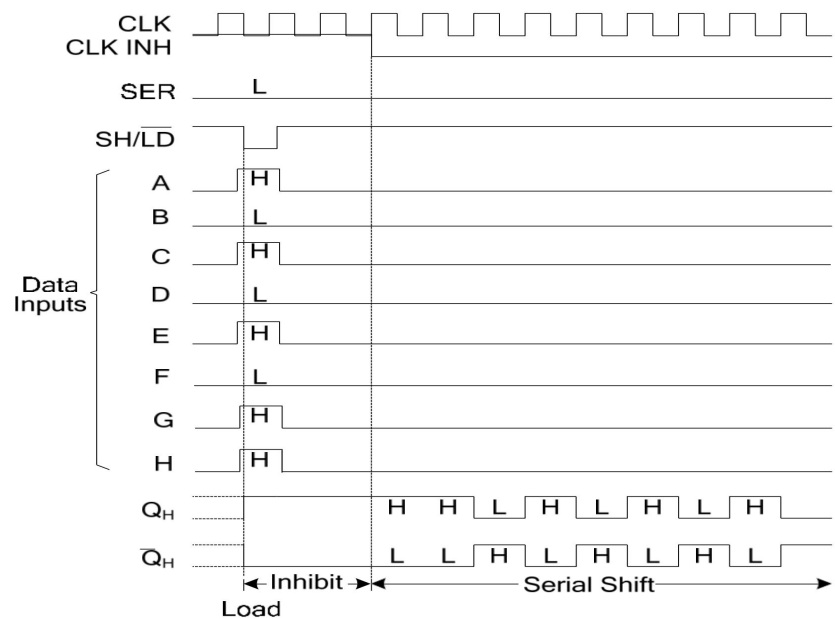
7. LOGIC SYMBOL



8. LOGIC DIAGRAM (positive logic)



9. TYPICAL SHIFT, LOAD, AND INHIBIT SEQUENCE



10. ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	-0.5 ~ 7	V
V _{CC} or GND Current	I _{CC}	±50	mA
Output Current	I _{OUT}	±25	mA
Input Clamp Current	I _{IK}	±20	mA
Output Clamp Current	I _{OK}	±20	mA
Storage Temperature	T _{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

11. RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}	-	2	5	6	V
High-level Input Voltage	V _{IH}	V _{CC} =2V	1.5	-	-	V
		V _{CC} =4.5V	3.15	-	-	V
		V _{CC} =6V	4.2	-	-	V
Low-level Input Voltage	V _{IL}	V _{CC} =2V	-	-	0.5	V
		V _{CC} =4.5V	-	-	1.35	V
		V _{CC} =6V	-	-	1.8	V
Input Voltage	V _{IN}	-	0	-	V _{CC}	V
Output Voltage	V _{OUT}	-	0	-	V _{CC}	V
Input Transition (Rise and Fall) Time	t _i	V _{CC} =2V	-	-	1000	ns
		V _{CC} =4.5V	-	-	500	ns
		V _{CC} =6V	-	-	400	ns
Operating Free-air Temperature	T _A	-	-40	-	+125	°C

12. THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-16	73	°C/W
	TSSOP-16	110	°C/W

13. ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage High-Level	V _{OH}	V _{CC} =2V, I _{OH} =-20μA	1.9	1.998	-	1.9	-	-	V
		V _{CC} =4.5V, I _{OH} =-20μA	4.4	4.499	-	4.4	-	-	V
		V _{CC} =6V, I _{OH} =-20μA	5.9	5.999	-	5.9	-	-	V
		V _{CC} =4.5V, I _{OH} =-4mA	3.98	4.3	-	3.7	-	-	V
		V _{CC} =6V, I _{OH} =-5.2mA	5.48	5.8	-	5.2	-	-	V
Output Voltage Low-Level	V _{OL}	V _{CC} =2V, I _{OL} =20μA	-	0.002	0.1	-	-	0.1	V
		V _{CC} =4.5V, I _{OL} =20μA	-	0.002	0.1	-	-	0.1	V
		V _{CC} =6V, I _{OL} =20μA	-	0.002	0.1	-	-	0.1	V
		V _{CC} =4.5V, I _{OL} =4mA	-	0.15	0.26	-	-	0.4	V
		V _{CC} =6V, I _{OL} =5.2mA	-	0.16	0.26	-	-	0.4	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} =6V, V _{IN} = V _{CC} or GND	-	±0.1	±1	-	-	±1	μA
Quiescent Supply Current	I _{CC}	V _{CC} =6V, V _{IN} =V _{CC} or GND, I _{OUT} =0	-	-	8	-	-	160	μA

14. TIMING REQUIREMENTS

PARAMETER		SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Clock frequency		f _{clock}	V _{CC} =2V	0	-	6	-	-	4.2	MHz
			V _{CC} =4.5V	0	-	31	-	-	21	MHz
			V _{CC} =6V	0	-	36	-	-	25	MHz
Pulse duration	SH/ $\overline{\text{LD}}$ low	t _w	V _{CC} =2V	80	-	-	120	-	-	ns
			V _{CC} =4.5V	16	-	-	24	-	-	ns
			V _{CC} =6V	14	-	-	20	-	-	ns
	CLK high or low		V _{CC} =2V	80	-	-	120	-	-	ns
			V _{CC} =4.5V	16	-	-	24	-	-	ns
			V _{CC} =6V	14	-	-	20	-	-	ns
Setup time	SH/ $\overline{\text{LD}}$ high before CLK↑	t _{su}	V _{CC} =2V	80	-	-	120	-	-	ns
			V _{CC} =4.5V	16	-	-	24	-	-	ns
			V _{CC} =6V	14	-	-	20	-	-	ns
	SER before CLK↑		V _{CC} =2V	40	-	-	60	-	-	ns
			V _{CC} =4.5V	8	-	-	12	-	-	ns
			V _{CC} =6V	7	-	-	10	-	-	ns
	CLK INH low before CLK↑		V _{CC} =2V	100	-	-	150	-	-	ns
			V _{CC} =4.5V	20	-	-	30	-	-	ns
			V _{CC} =6V	17	-	-	25	-	-	ns
	CLK INH high before CLK↑		V _{CC} =2V	40	-	-	60	-	-	ns
			V _{CC} =4.5V	8	-	-	12	-	-	ns
			V _{CC} =6V	7	-	-	10	-	-	ns
	Data before SH/ $\overline{\text{LD}}$ ↓		V _{CC} =2V	100	-	-	150	-	-	ns
			V _{CC} =4.5V	20	-	-	30	-	-	ns
			V _{CC} =6V	17	-	-	25	-	-	ns
Hold time	SER data after CLK↑	t _h	V _{CC} =2V	5	-	-	5	-	-	ns
			V _{CC} =4.5V	5	-	-	5	-	-	ns
			V _{CC} =6V	5	-	-	5	-	-	ns
	PAR data after SH/ $\overline{\text{LD}}$ ↓		V _{CC} =2V	5	-	-	5	-	-	ns
			V _{CC} =4.5V	5	-	-	5	-	-	ns
			V _{CC} =6V	5	-	-	5	-	-	ns

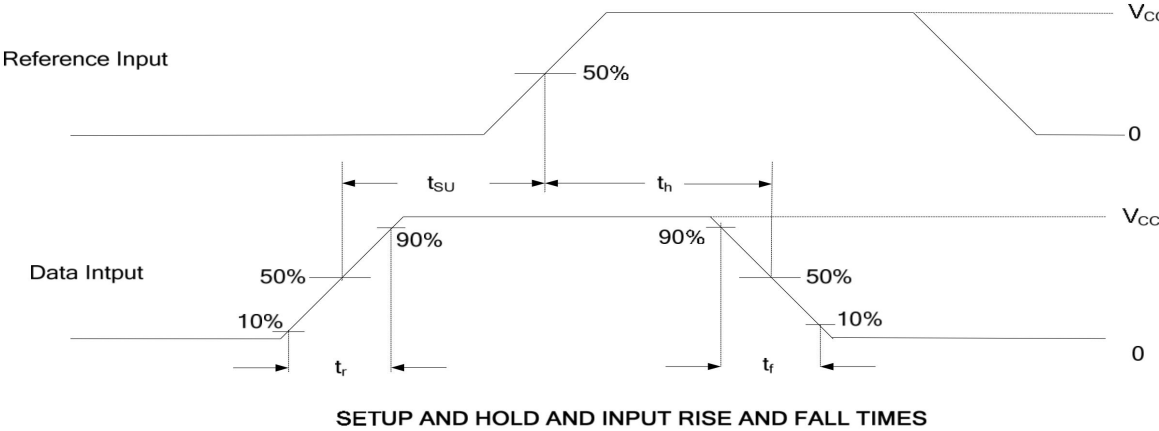
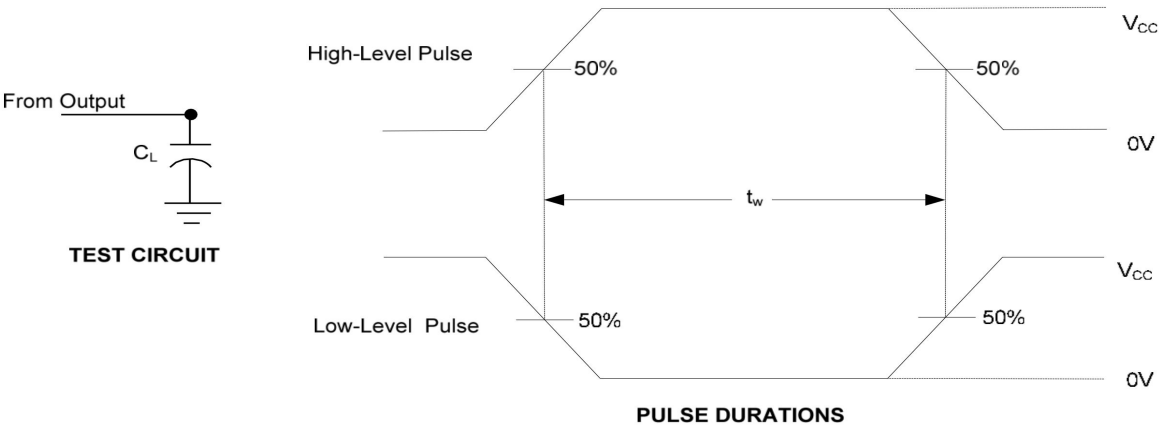
15. SWITCHING CHARACTERISTICS ($t_r = t_f = 6\text{ns}$, $C_L=50\text{Pf}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~-+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Minimum Frequency Response	f _{max}	V _{CC} =2V	6	13	-	4	-	-	MHz
		V _{CC} =4.5V	31	50	-	20	-	-	MHz
		V _{CC} =6V	36	62	-	24	-	-	MHz
Propagation delay from input (SH/ $\overline{\text{LD}}$) to output (QH or $\overline{\text{QH}}$)	t _{PD}	V _{CC} =2V	-	52	150	-	-	250	ns
		V _{CC} =4.5V	-	18	30	-	-	50	ns
		V _{CC} =6V	-	15	26	-	-	43	ns
V _{CC} =2V		-	52	150	-	-	250	ns	
V _{CC} =4.5V		-	19	30	-	-	50	ns	
V _{CC} =6V		-	16	26	-	-	43	ns	
Propagation delay from input (CLK) to output (QH or $\overline{\text{QH}}$)		V _{CC} =2V	-	36	150	-	-	180	ns
		V _{CC} =4.5V	-	13	30	-	-	36	ns
		V _{CC} =6V	-	10	26	-	-	31	ns
Propagation delay from input (H) to output (QH or $\overline{\text{QH}}$)	t _i	V _{CC} =2V	-	19	75	-	-	110	ns
		V _{CC} =4.5V	-	7	15	-	-	22	ns
		V _{CC} =6V	-	6	13	-	-	19	ns

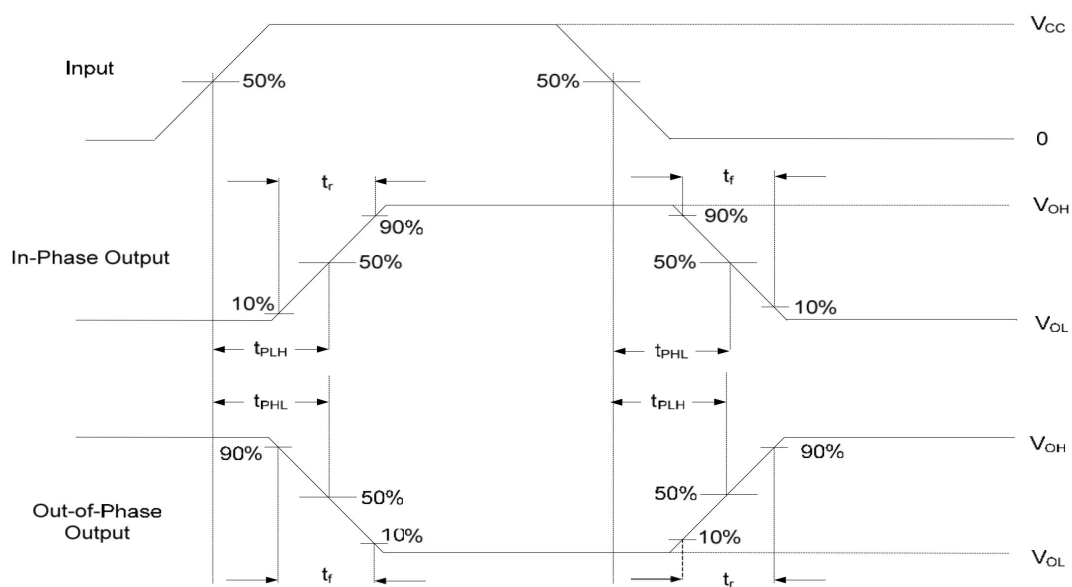
16. OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C _I	V _{CC} =2V to 6V	-	3	10	pF
Power Dissipation Capacitance	C _{PD}	No load	-	75	-	pF

17. TEST CIRCUIT AND WAVEFORMS



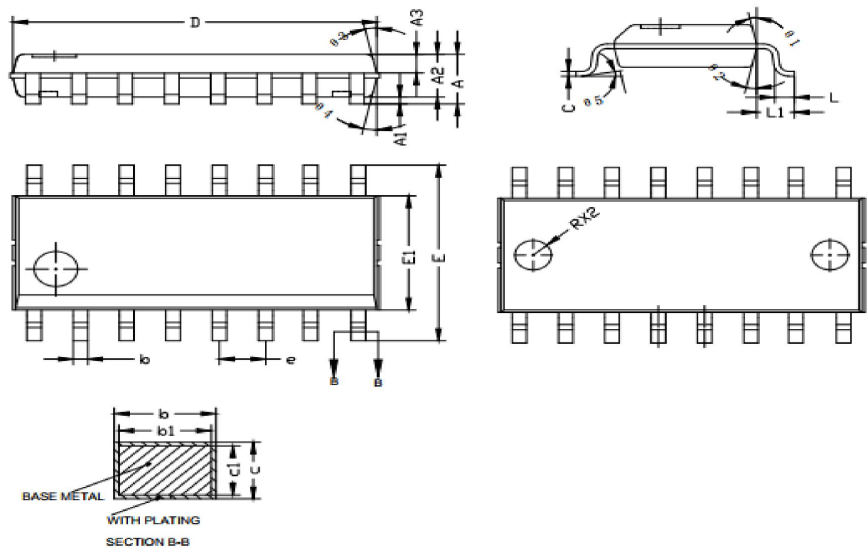
18. TEST CIRCUIT AND WAVEFORMS (Cont.)



PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

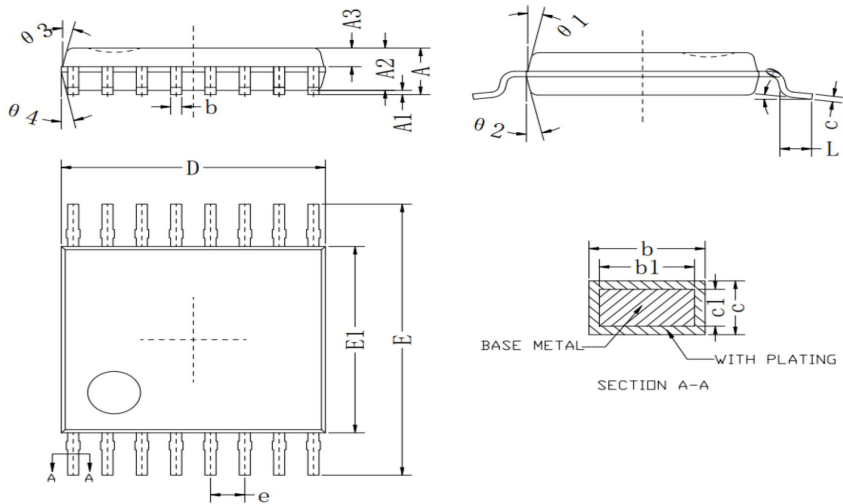
19. PACKAGE INFORMATION

SOP 16 package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.70
A1	0.10	0.15	0.21
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.33	--	0.47
b1	0.32	0.41	0.44
c	0.20	--	0.24
c1	0.19	0.20	0.21
D	9.50	9.90	10.05
E	5.80	6.00	6.20
E1	3.85	3.90	4.00
e	1.27(BSC)		
L	0.50	0.60	0.70
L1	1.10(BSC)		
θ 1	8°	~	15°
θ 2	8°	~	15°
θ 3	8°	~	15°
θ 4	8°	~	15°
θ 5	0°	~	6°
R	0.45*	0.50*	0.05*

TSSOP16 package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.20
A1	0.05	0.10	0.15
A2	0.80	1.00	1.05
A3	0.38	0.43	0.48
b	0.19	--	0.29
b1	0.16	0.22	0.26
c	0.13	--	0.15
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65(BSC)		
L	0.45	0.60	0.75
θ	0°	~	8°
θ 1	10°	~	14°
θ 2	10°	~	14°
θ 3	10°	~	14°
θ 4	10°	~	14°