Description

The WL9003 family are the 300mA LDO. It uses an advanced CMOS process and a PMOSFET pass device to achieve high power supply rejection ratio (PSRR), low noise, low dropout, low ground current, fast start-up and excellent output accuracy.

The WL9003 family are stable with a 1.0μF ceramic output capacitor, uses a precision voltage reference and feedback loop to achieve excellent Regulation and transient response.

The WL9003 family offered in a small SOT23-5 package, which are ideal for small form factor portable equipment.

Features

- Low Power Consumption: 35 μA (Typ)
- Maximum Output Current: 300mA
- Low Dropout Voltage:
  75mV@100mA (V_{OUT}=3.3V)
  210mV@300mA (V_{OUT}=3.3V)
- Operating Voltage Range: 2.0V ~ 6.0V
- Output Voltage Accurate: ± 2%
- High PSRR: 75dB @1kHz
- Very Low Noise is 45uVrms at 1.2V output
- Good Transient Response
- Integrated Short-Circuit Protection
- Over-Temperature Protection
- Output Current Limit
- Low Temperature Coefficient
- Stable with Ceramic Capacitor
- RoHS Compliant and Lead (Pb) Free
- -40°C to +85°C Operating Temperature Range
- Fixed Output Voltage Versions: 1.2,1.5,1.8,2.5,2.8,3.0 and 3.3V（steps 0.05V）
  Special Request: Any Voltagebetween 1.0V and 3.3V under specific business agreement
- Available in Green SOT23-5 Package

Applications

- Battery-powered equipment
- Wireless Communication Equipment
- Reference voltage sources
- Audio/Video Equipment
- Low Power Microcontrollers
- Portable games

Application Circuits

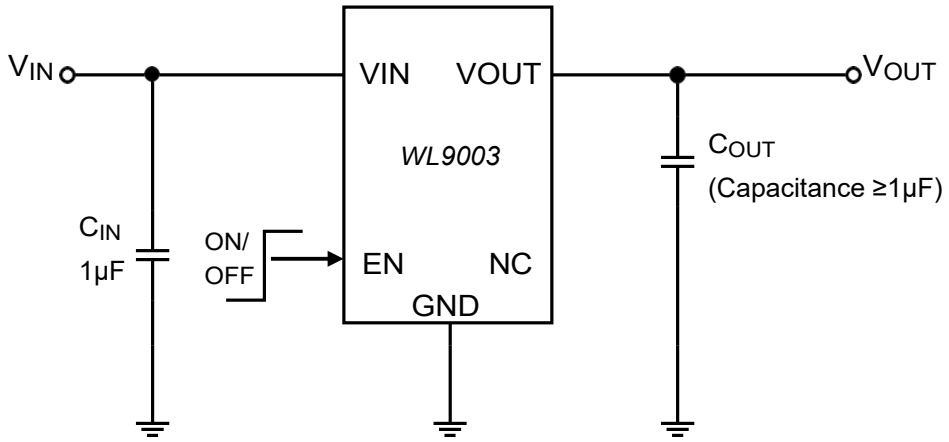
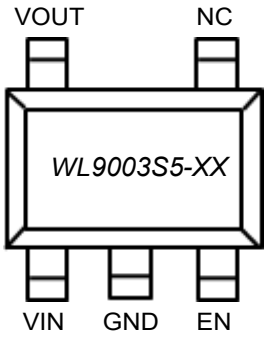


Figure 1. WL9003 Typical Application Circuit

Pin Configuration （TOP VIEW）



SOT23-5

Pin Description

Pin No. SOT23-5	Pin Name	Pin Function
1	VIN	Supply input pin. Must be closely decoupled to GND with a 1μF orgreater ceramic capacitor
2	GND	Ground
3	EN	Enable control input, active high. Do not leave EN floating
4	NC	No Connect
5	VOUT	Output pin. A 1μF low-ESR capacitor should be connected to this pin to ground

Order Information

WL9003①②-③④

Designator	Symbol	Description
①②	S5	SOT23-5L
③④	Integer e.g 3.3=33	Output Voltage 1.2,1.5,1.8,2.5,2.8,3.0 and 3.3V

Part NO.	Description	Package	T/R Qty
WL9003S5-XX	WL9003 6.0V,High PSRR Low Noise 300mA RF LDO	SOT23-5L	3,000 PCS

Top Marking For WL9003S5-XX

Part NO.	Package	VOUT	Product Code (Note)
WL9003S5-12	SOT23-5L	1.2V	DA=YLL
WL9003S5-15	SOT23-5L	1.5V	DS=YLL
WL9003S5-18	SOT23-5L	1.8V	DC=YLL
WL9003S5-25	SOT23-5L	2.5V	DH-YLL
WL9003S5-28	SOT23-5L	2.8V	DJ-YLL
WL9003S5-30	SOT23-5L	3.0V	DK-YLL
WL9003S5-33	SOT23-5L	3.3V	DE=YLL

Note:YLL Internal Code Represents the assembly lot no. 0~9, A~Z repeated

For marking information, contact our sales representative directly

Pb-free, Green RoHS All WPMtek parts are Pb-Free and adhere to the RoHS directive.

Absolute Maximum Ratings

Item		Symbol	Rating	Unit
Supply Input Voltage		V_{IN}	-0.3 ~ 7.0	V
EN to GND		V_{EN}	-0.3 ~ V_{IN} +0.3V	V
Regulated Output Voltage		V_{OUT}	-0.3 ~ V_{IN} +0.3V	V
Output Current		I_{OUT}	Internally limited	mA
Power Dissipation P_D @T_A=+25℃	SOT23-5	P_D	500	mW
Thermal Resistance (Junction to air)	SOT23-5	θ_{JA}	250	°C /W
Human Body Model (HBM)		±4000		V
Charged Device Mode (CDM)		±1500		V
Machine Mode (MM)		200		V
Storage Temperature Range		T_{STG}	-65 ~ +150	°C
Operating Junction Temperature		T_J	+150	°C
Lead Temperature (Soldering 10s)		T_{LEAD}	+260	°C

Note：

1、Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended period may affect device reliability.

2、Ratings apply to ambient temperature at +25°C.

3、The package thermal impedance is calculated in accordance to JESD 51-7.

Recommended Operating Conditions

Item	Min	Max	Unit
Operating Ambient Temperature	-40	+85	°C
Input Voltage	2.0	6.0	V
Output Voltage	0.8	3.3	V

Electronic Characteristics

Test Conditions: VIN = VOUT +1V,CIN=COUT=1uF,TA=25℃, unless otherwise specifi

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Voltage	VIN			2.0	——	6.0	V
Quiescent Current	IQ	VIN >VOUTNOM , VIN=EN IOUT =0mA		——	35	50	μA
Shutdown Current	ISHDN	EN=0 V , VOUT =0 V		——	0.01	0.05	μA
Output Voltage	VOUT	VIN = VOUTNOM +1V IOUT =10mA		VOUT x 0.98	——	VOUT x 1.02	V
Output Current	IOUT	VIN = VOUTNOM +1V		300	——	——	mA
Dropout Voltage VOUT =3.3V	VDROP	IOUT =100mA		——	75	95	mV
		IOUT =300mA		——	210	300	
Line Regulation	Δ VLINE	IOUT =10mA VOUTNOM +1.0V ≦ VIN ≦5.5V		——	0.03	0.1	% / V
Load Regulation	Δ VLOAD	VIN = VOUTNOM +1V 1mA≦ IOUT ≦300mA		——	20	30	mV
EN Threshold Voltage	VCEH	CE“High”Voltage		1.5	——	——	V
	VCEL	CE“Low”Voltage		——	——	0.3	V
EN PIN Current	IEN			——	0.01	——	μA
Current Limit	ILIMIT			——	500	——	mA
Short Current	ISHORT	VOUT = GND		——	100	——	mA
Output Noise Voltage	VON	VOUT=2.8V , IOUT =200mA BW = 10Hz~100KHz,		——	70	——	μVrms
		VOUT=1.2V , IOUT =200mA BW = 10Hz~100KHz,		——	45	——	μVrms
Power Supply Rejection Rate	PSRR	IOUT =20mA VOUT =3.3V	f=1kHz	——	75	——	dB
			f=10kHz	——	70	——	dB
Temperature Coefficient	Δ VOUT / Δ T * VOUT	IOUT =30mA ,TA=0~70°C		——	± 100	——	ppm/°C
Soft-start Time	TS	From enable to power on		——	25	——	μs
ENpull-down resistance	RPD	EN pull-down resistance		0.8	1	1.3	MΩ
Thermal Shutdown Temperature	T_{SHDN}	——		——	155	——	°C
Thermal Shutdown Hysteresis	ΔT_{SHD}	——		——	20	——	°C

Note : All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Functional Block Diagram

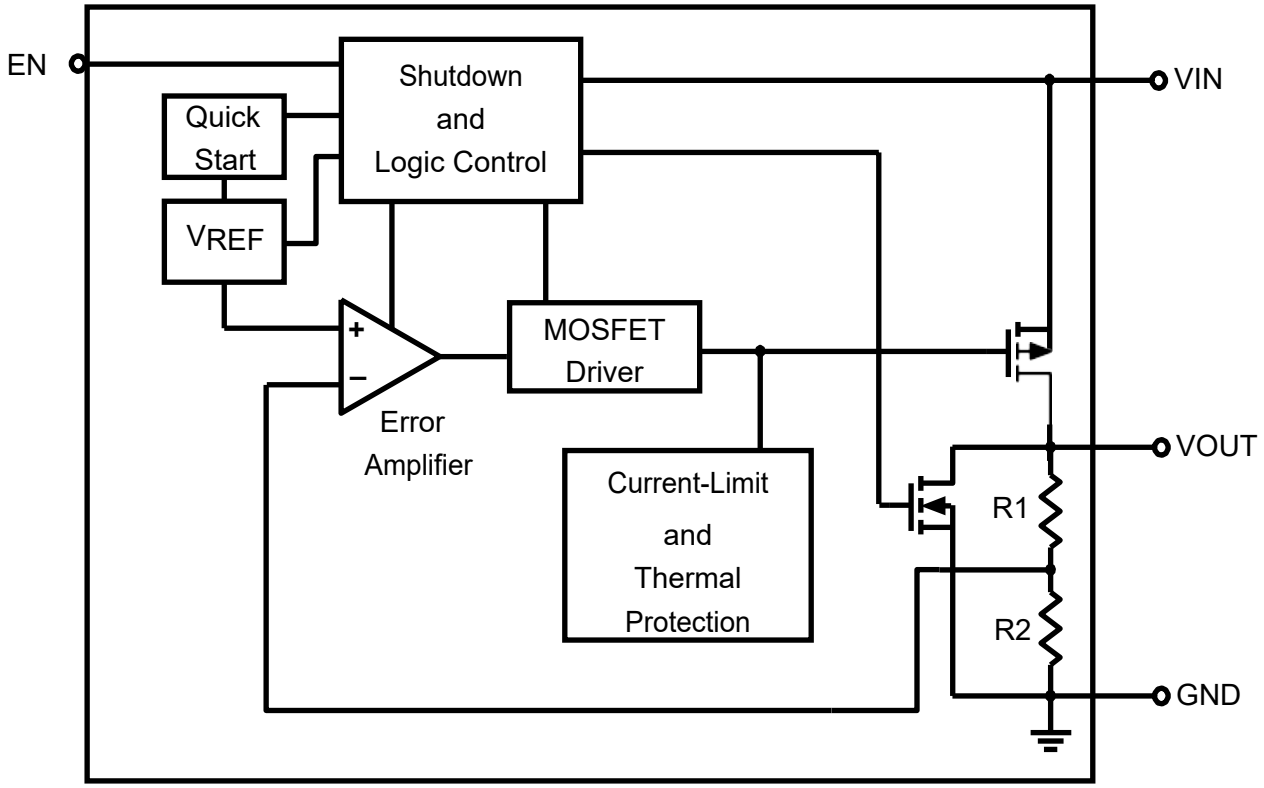
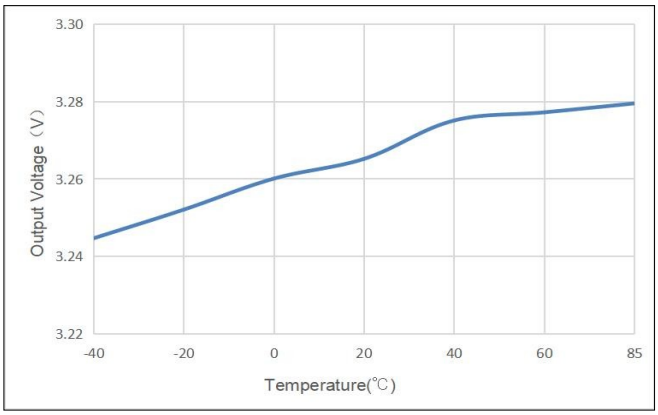


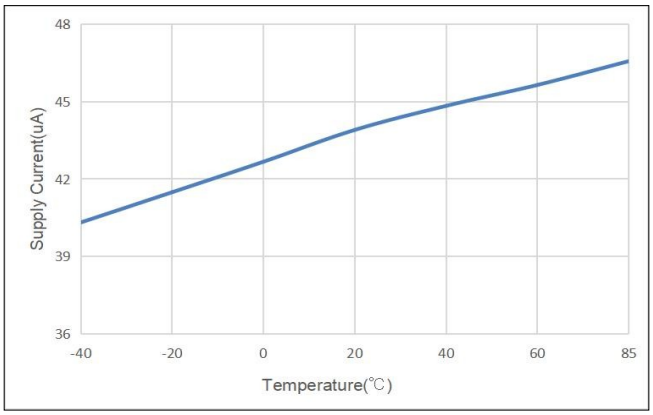
Figure 2.WL9003 Block Diagram

Typical Performance Characteristics

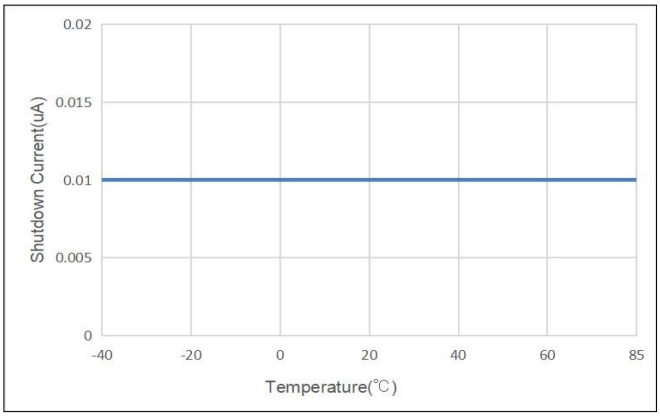
(V_{IN}=4.3V,V_{OUT}=3.3V,I_{OUT}=1mA,C_{IN}=C_{OUT}=1μF,unless otherwise noted. Typical values are at T_A=25°C.)



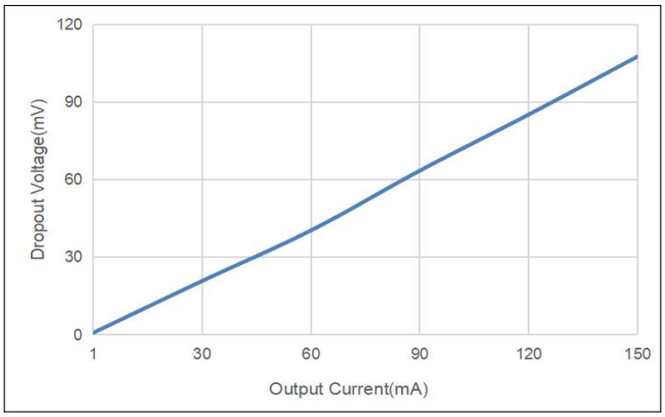
Output Voltage VS Temperature



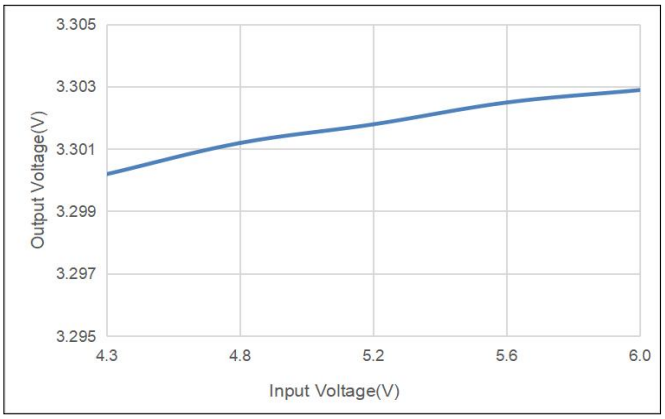
Supply Current VS Temperature



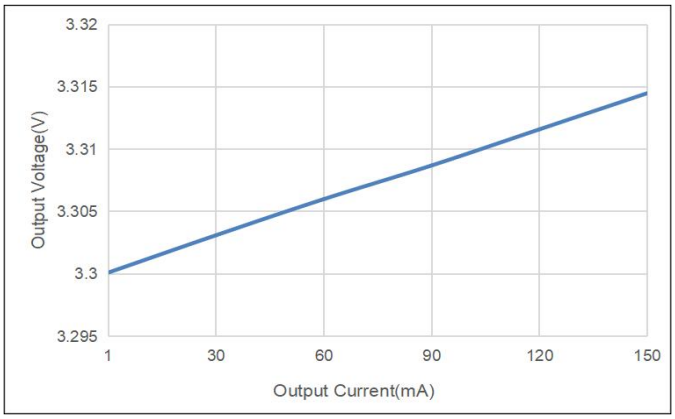
Shutdown Current VS Temperature



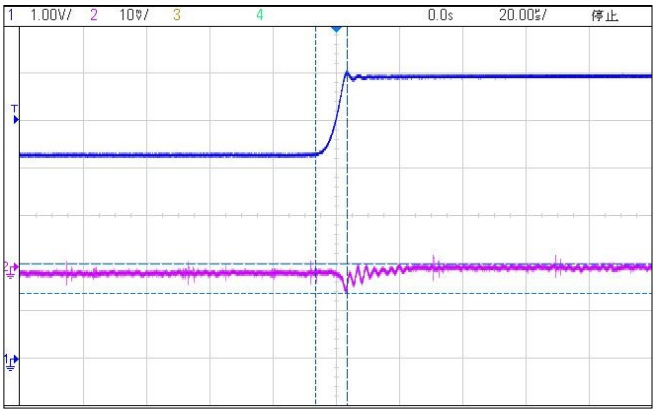
Dropout Voltage VS Output Current



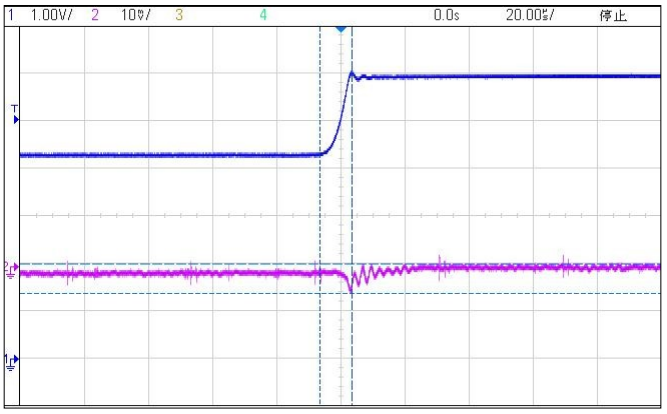
Output Voltage VS Input Voltage



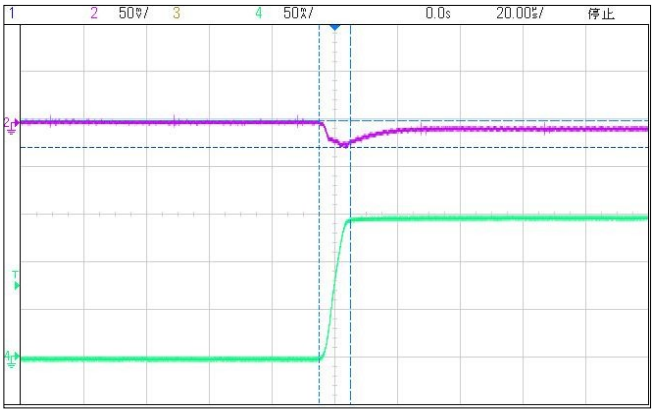
Output Voltage VS Output Current



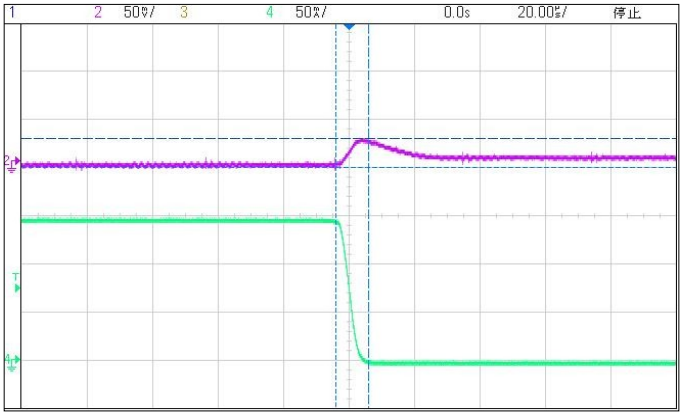
Input Transient(4.3~6V t=10us 10mA)



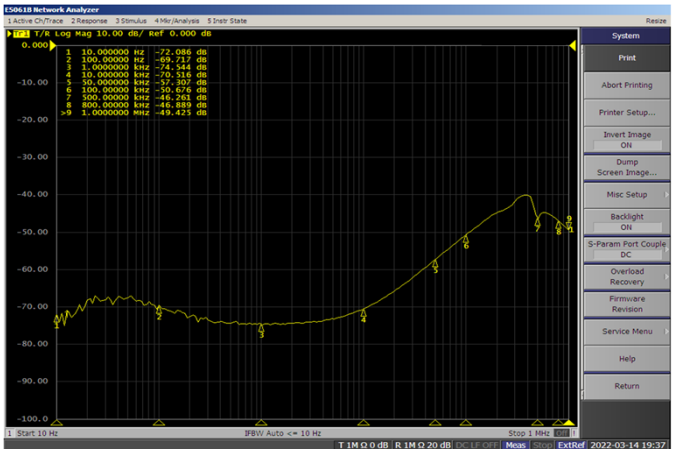
Input Transient(6~4.3V t=10us 10mA)



Load Transient(1mA~150mA t=10us)



Load Transient(150mA~1mA t=10us)



PSRR Vs. Frequency

Application Guideline

■ Input Capacitor

A ⩾ 1μF ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

■ Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is ⩾1μF, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to VOUT and GND pins.

■ Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage V_{DROP} also can be expressed as the voltage drop on the pass-FET at specific output current (I_{RATED}) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized asan resistance RDS(ON). Thus the dropout voltage can bedefined as ($V_{DROP} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{RATED}$). Fornormal operation, the suggested LDO operating range is ($V_{IN} > V_{OUT} + V_{DROP}$) for good transient response and PSRR ability. Vice versa, while operating at the ohmic region will degrade the performance severely.

■ Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below:

T_A=25°C, AISIS DEMO PCB

The max $P_D = (Tj - T_A) / \theta_{JA}$.

Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

$P_D = (V_{IN} – V_{OUT}) \times I_{OUT}$

■ Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the WL9003 ground pin using as wide and as short of a copper trace as is practical.Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.