

Description

The WL9005 series are highly precise, low noise, positive voltage LDO regulators manufactured using CMOS processes. The series achieves high ripple rejection and low dropout and consists of a standard voltage source, an error correction, current limiter and a phase compensation circuit plus a driver transistor. Output voltage is selectable in 0.05V increments within a range of 0.8V \sim 5.0V. The series is also compatible with low ESR ceramic capacitors which give added output stability. It provides up to 500mA of output current in miniaturized packaging. The features of low quiescent current as low as 0.3 μ A and almost zero disable current is ideal for powering the battery equipment to a longer service life. The other features include current limit function, Integrated Short-Circuit Protection ,over temperature protection and Fast discharge function.

Features

- > Low Power Consumption: 0.3 μA (Typ)
- Maximum Output Current: 500mA
- ► Low Dropout Voltage: 100mV@100mA (Vout=3.3V)
- Operating Voltage Range: 2.0V ~ 7.0V
- Output Voltage Accurate: ± 1.5%
- ➤ High PSRR: 70dB @1kHz
- Good Transient Response
- Integrated Short-Circuit Protection
- Over-Temperature Protection
- Output Current Limit
- Low Temperature Coefficient
- Stable with Ceramic Capacitor
- RoHS Compliant and Lead (Pb) Free
- → -40°C to +85°C Operating Temperature Range
- Fixed Output Voltage Versions: 0.8,1.0,1.2,1.5,1.8,2.5,2.8,3.0,3.3,3.6 and 5.0V (steps 0.05V) Special Request: Any Voltagebetween 0.8V and 5.0V under specific business agreement
- Available in Green SOT23-3,SOT23-5,SOT89-3,DFN1x1-4L,DFN2x2-6L Packages

Applications

- Battery-powered equipment
- Wireless Communication Equipment
- Reference voltage sources
- Audio/Video Equipment
- Low Power Microcontrollers
- Portable games



Application Circuits

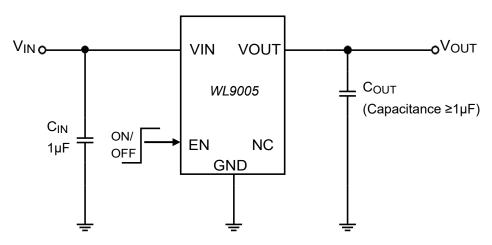
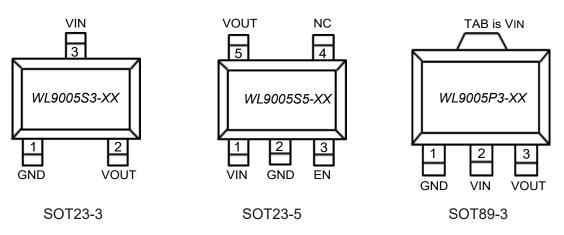


Figure 1. WL9005 Typical Application Circuit

Pin Configuration (TOP VIEW)



VIN ΕN ΕN NC EP. 5 GND Éxposed`\ NC Mark Mark Pad/ VIN **VOUT** VOUT **GND** PIN 1# Indicator PIN 1# Indicator

WL9005D4-XX DFN-4L (1mm × 1mm) 0.4mm height(max),0.65mm pitch WL9005F6-XX DFN-6L (2mm × 2mm) 0.6mm height(max),0.65mm pitch



Pin Description

Pin No.							
SOT23-5	SOT23-3	SOT89-3	DFN1010-4L	DFN2020-6L	Pin Name	Pin Function	
S5	S3	P3	D4	D6			
1	3	2	4	3	VIN	Power Input	
2	1	1	2	2	GND	Ground	
3			3	1	EN	Enable Control Input	
5	2	3	1	4	VOUT	Output Voltage	
4				5、6	NC	No Connect	
EP / TAB	EP / TAB In PCB layout, prefer to use large copper area to cover this pad for better thermal dissipation						

Order Information

WL9005(1)(2)-(3)(4)

Designator Symbol		Description		
12	S3 , S5 , P3 , D4 , F6	SOT23-3L , SOT23-5L , SOT89-3L , DFN1X1-4L , DFN2X2-6L		
34	Integer e.g 3.3=33	Output Voltage 0.8,1.0,1.2,1.5,1.8,2.5,2.8,3.0,3.3, 3.6 and 5.0V		

Part NO.	Description	Package	T/R Qty
WL9005S3-XX		SOT23-3L	3,000 PCS
WL9005S5-XX	WL9005	SOT23-5L	3,000 PCS
WL9005P3-XX	7V ,0.3μA IQ ,High PSRR ,500mA	SOT89-3L	1,000 PCS
WL9005D4-XX	Low-Dropout LDO	DFN1X1-4L	10,000 PCS
WL9005F6-XX		DFN2X2-6L	5,000 PCS



Absolute Maximum Ratings

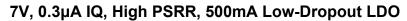
Item		Symbol	Rating	Unit
Supply Input Voltage		Vin	-0.3 ~ 9	V
EN to GND		VEN	-0.3 ~ 9	V
Regulated Output Volta	ge	Vout	-0.3 ~ 5	V
Output Current		lout	Internally limited	mA
	SOT23-3L		450	
Davis Diagination	SOT23-5L		500	
Power Dissipation	SOT89-3L	P _D	700	mW
P _D @T _A =+25°C	DFN1X1-4L		530	
	DFN2X2-6L		750	
	SOT23-3L		275	
The same of Development	SOT23-5L		250	
Thermal Resistance	SOT89-3L	θμΑ	180	°C /W
(Junction to air)	DFN1X1-4L		235	
	DFN2X2-6L		165	
Human Body Model (HBM)			±4000	
Charged Device Mode	(CDM)		±2000	
Machine Mode (MM)			200	
Storage Temperature R	ange	Tstg	-65 ~ +150	°C
Operating Junction Temperature		TJ	+150	°C
Lead Temperature (Sol	dering 10s)	TLEAD	+260	°C

Note:

- 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended period may affect device reliability.
- 2. Ratings apply to ambient temperature at +25°C.
- 3. The package thermal impedance is calculated in accordance to JESD 51-7.

Recommended Operating Conditions

Item	Min	Max	Unit
Operating Ambient Temperature	-40	+85	°C
Input Voltage	2.0	7.0	V
Output Voltage	0.8	5.0	V





Electronic Characteristics

Test Conditions: VIN = VOUT +1V,CIN=COUT=1uF,TA=25°C, unless otherwise specifi

Parameter	Symbol	Test Conditions		Min	Тур	Max	Unit
Input Voltage	Vin			2.0		7.0	V
Quiescent Current	IQ	VIN >VOUTNOM , VIN=E	N		0.3	0.5	μA
Shutdown Current	ISHDN	EN=0 V , Vout =0 V			0	0.1	μΑ
Output Voltage	Vout	VIN = VOUTNOM +1V IOUT =10mA		VOUT x 0.985	——	VOUT x 1.015	V
Output Current	lout	VIN = VOUTNOM +1V		500			mA
Dropout Voltage	\/ppop	IOUT =100mA			100		>/
Vout =3.3V	VDROP	IOUT =500mA			600	750	mV
Line Regulation	Δ VLINE	IOUT =10mA VOUTNOM +1.0V ≦ VIN	IOUT = 10mA VOUTNOM + $1.0\text{V} \le \text{VIN} \le 7\text{V}$		0.05		% / V
Load Regulation	Δ VLOAD	VIN = VOUTNOM +1V 1mA≦ IOUT ≦100mA			5	20	mV
EN Threshold	VCEH	CE"High"Voltage		1.2			V
Voltage	VCEL	CE"Low"Voltage				0.4	V
EN PIN Current	lEN				0.01		μA
Current Limit	ILIMIT				650		mA
Short Current	ISHORT	Vout = GND			100		mA
Output Noise Voltage	Von	Vout=3.3V , lout =200 BW = 100Hz~10KHz,	Vout=3.3V , Iout =200mA BW = 100Hz~10KHz,		100		μVrms
Power Supply	DCDD	IOUT =100mA,	f=1kHz		70		dB
Rejection Rate	PSRR	VOUT =3.3V	f=10kHz		65		dB
Temperature Coefficient	Δ Vout / Δ T * Vout	IOUT =30mA , TA=0~70°C			± 100		ppm/°C
Thermal Shutdown Temperature	T _{SHDN}				160		°C
Thermal Shutdown Hysteresis	ΔT_{SHD}				20		°C

Note: All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).



Functional Block Diagram

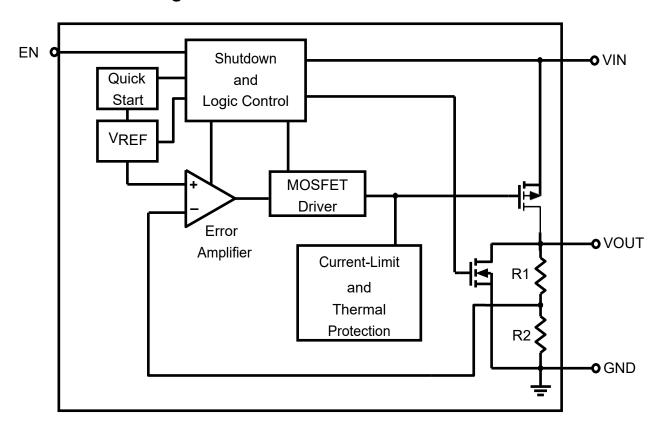
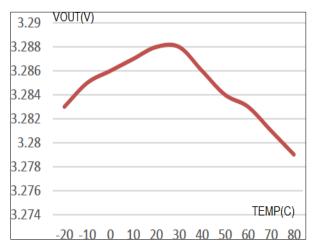
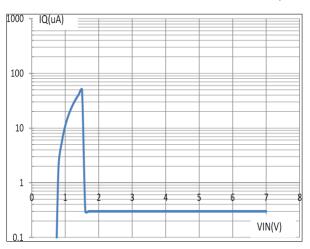


Figure 2. WL9005 Block Diagram



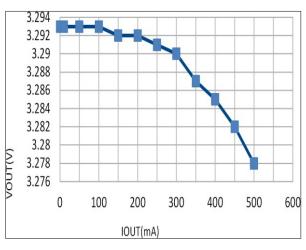
Typical Performance Characteristics (VIN = EN =4.3V ,VOUT=3.3V,CIN=COUT=1uF,TA=25℃)

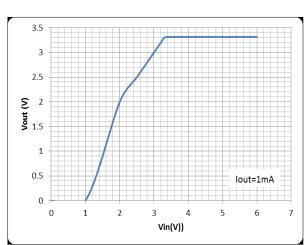




Output Voltage vs TEMP

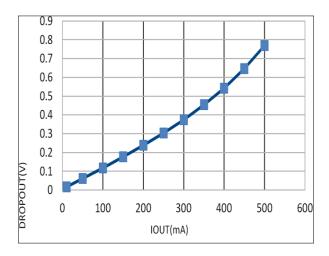
Input Voltage vs. IQ (Note about IQ)

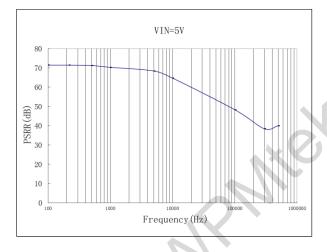




Load Regulation

Line Regulation





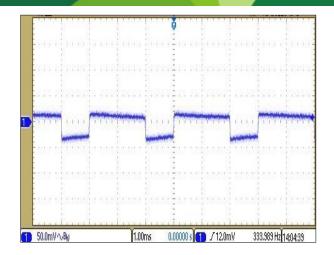
Dropout Voltage vs.Load Curren

PSRR vs. Frequency





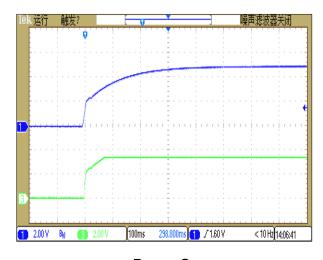
7V, 0.3µA IQ, High PSRR, 500mA Low-Dropout LDO

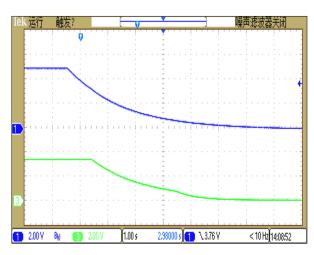


1.00 V By 2.00 V [1.00 s 0.00000 s] 1 \1.44 V < 10 Hz [15,43,23

Load Transient Response

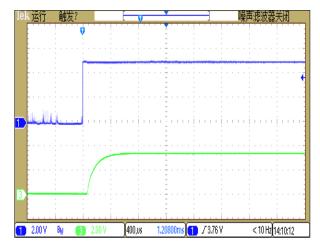
Short Output & Over-Current Response

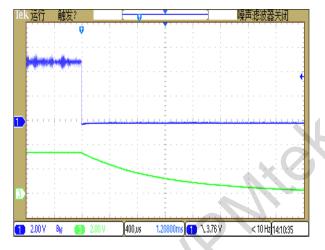




Power-On

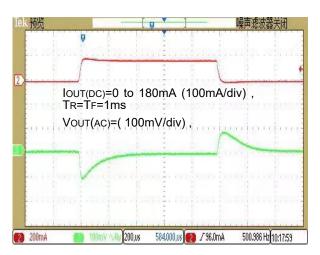
Power-Off

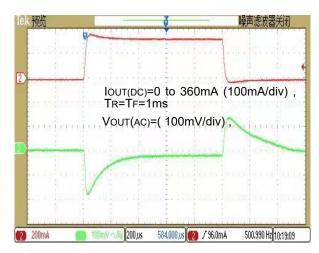




Enable Disable







Load Transient VIN=EN=5V

Load Transient VIN=EN=5V

Note about IQ:

IQ refers to the working current when the chip is no-load, only when Vin >Vout The chip will have a very low working current, the above diagram is for Vout 1.5v Measured Curve, when Vin<Vout, the chip is in an abnormal state that can not reach the intended output, therefore, the operating current will increase significantly. For applications where IQ requirements are strict, make sure the chip stops working when Vin <Vout.

Application Guideline

■ Input Capacitor

 $A \geqslant 1 \mu F$ ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is $\geqslant 1\mu F$, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to VOUT and GND pins.



Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage V_{DROP} also can be expressed as the voltage drop on the pass-FET at specific output current (I_{RATED}) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized as an resistance RDS(ON). Thus the dropout voltage can be defined as ($V_{DROP} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{RATED}$). Fornormal operation, the suggested LDO operating range is ($V_{IN} > V_{OUT} + V_{DROP}$) for good transient response and PSRR ability. Vice versa, while operating at the ohmic region will degrade the performance severely.

■ Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below:

T_A=25°C, WPM DEMO PCB,

The max $P_D = (T_j - T_A) / \theta_{JA}$.

Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

■ Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the WL9005 ground pin using as wide and as short of a copper trace as is practical. Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.



Marking Information

For marking information, contact our sales representative directly

WL9005S3-12	WL9005S3-15	WL9005S3-18	WL9005S3-25	WL9005S3-28
AJ12C	AJ15C	AJ18C	AJ25C	AJ28C
WL9005S3-30	WL9005S3-33	WL9005S3-36	WL9005S3-50	WL9005S5-12
AJ30C	AJ33C	AJ36C	AJ50C	AJ=Sa
WL9005S5-15	WL9005S5-18	WL9005S5-25	WL9005S5-28	WL9005S5-30
AJ=Se	AJ=Sh	AJ=2E	AJ=2H	AJ=3B
WL9005S5-33	WL9005S5-36	WL9005S5-50	WL9005P3-12	WL9005P3-15
AJ=3C	AJ=3F	AJ=5B	AJ=Sa	AJ=Se
WL9005P3-18	WL9005P3-25	WL9005P3-28	WL9005P3-30	WL9005P3-33
AJ=Sh	AJ=2E	AJ=2H	AJ=3B	AJ=3C
WL9005P3-36	WL9005P3-50	WL9005D4-12	WL9005D4-15	WL9005D4-18
AJ=3F	AJ=3F	AY	BY	CY
WL9005D4-25	WL9005D4-28	WL9005D4-30	WL9005D4-33	WL9005D4-36
DY	EY	FY	GY	HY
WL9005D4-50				
KY				

All WPMtek parts are Pb-Free and adhere to the RoHS directive.

WPMtek reserves the right to make changes to the product specification and data in this document without notice. WPMtek makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does WPMtek assume any liability arising from the application or use of any products or circuits, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Any enquiry ,please write to sales@wpmtek.com for futher information.

Ver1.53 - 11 - www.wpmtek.com