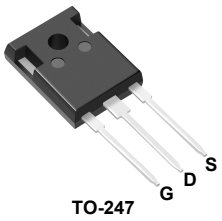
Applications

For Soft Switching Boost PFC switch, HB or AHB or LLC half bridge and full bridge topologies.
Such as phase-shift-bridge(ZVS),LLC Application-Server Power, Telecom Power, EV Charging, Solar inverter.



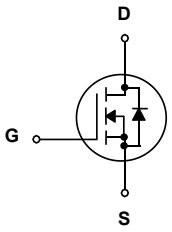
TO-247

Features

Low drain-source on-resistance: RDS(ON) = 0.031Ω (typ.)
Easy to control Gate switching
Enhancement mode: Vth = 3 to 5 V

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	35	mΩ
$Q_{g,typ}$	158.2	nC
I_D	90	A
Body diode dv/dt	50	V/ns



Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D		-	90	A	T_C=25°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	240	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	2560	mJ	Tc=25℃,VDD=50V,L=20mH , RG=25Ω
Avalanche current, single pulse	I_{AR}	-	-	16	A	Tc=25℃,VDD=50V,L=20mH , RG=25Ω
MOSFET dv/dt ruggedness	dv/dt	-	-	26	V/ns	V_{DS}=0...150V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	500	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	
Operating junction temperature	T_j	-55	-	150	°C	
Soldering Temperature Distance of 1.6mm from case for 10S	T_L			260	°C	
Reverse diode dv/dt[3]	dv/dt	-	-	50	V/ns	V_{DS}=0...400V, I_{SD}<=48A, T_j=25°C see table 8

1) Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
2) Pulse width t_p limited by $T_{j,max}$
3) Identical low side and high side switch with identical R_G

Thermal characteristics

Table 3 Thermal characteristics

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Thermal resistance, junction	- case	R_{thJC}	-	-	0.205	°C/W	-
Thermal resistance, junction	- ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint

Table 4 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.61	-	V	V_{GS}=0V, I_F=1A, T_j=25°C
Reverse recovery time	t_{rr}	-	173.5	-	ns	Vr=400v,IF=44.2A,di/dt=100A/us see table 8
Reverse recovery charge	Q_{rr}	-	1.19	-	uC	Vr=400v,IF=44.2A,di/dt=100A/us see table 8
Peak reverse recovery current	I_{rrm}	-	12.7	-	A	Vr=400v,IF=44.2A,di/dt=100A/us see table 8

Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	655	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{(GS)th}$	3		5	V	V_{DS}=V_{GS}, I_D=250uA
Zero gate voltage drain current	I_{DSS}	-	-	5	uA	V_{DS}=650V, V_{GS}=0V, T_j=25°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=30V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.031	0.035	Ω	V_{GS}=10V, I_D=28A, T_j=25°C
Gate resistance (Intrinsic)	R_G	-	1.2	-	Ω	f=1MHz, open drain

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	6033	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
Output capacitance	C_{oss}	-	169	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
Reverse transfer capacitance	C_{rss}	-	12.1	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
Turn-on delay time	$t_{d(on)}$	-	67.6	-	ns	V_{DD}=400V,V_{GS}=13V,I_D=44.2A R_G=1.8Ω;see table 9
Rise time	t_r	-	29.8	-	ns	V_{DD}=400V,V_{GS}=13V,I_D=44.2A R_G=1.8Ω;see table 9
Turn-off delay time	$t_{d(off)}$	-	30	-	ns	V_{DD}=400V,V_{GS}=13V,I_D=44.2A R_G=1.8Ω;see table 9
Fall time	t_f	-	325.4	-	ns	V_{DD}=400V,V_{GS}=13V,I_D=44.2A R_G=1.8Ω;see table 9

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	45	-	nC	V_{DD} =480V, I_D =44.2A, V_{GS} =10V
Gate to drain charge	Q_{gd}	-	61	-	nC	V_{DD} =480V, I_D =44.2A, V_{GS} =10V
Gate charge total	Q_g	-	158.2	-	nC	V_{DD} =480V, I_D =44.2A, V_{GS} =10V
Gate plateau voltage	$V_{plateau}$	-	6.14	-	V	V_{DD} =480V, I_D =44.2A, V_{GS} =10V

Electrical characteristics diagram

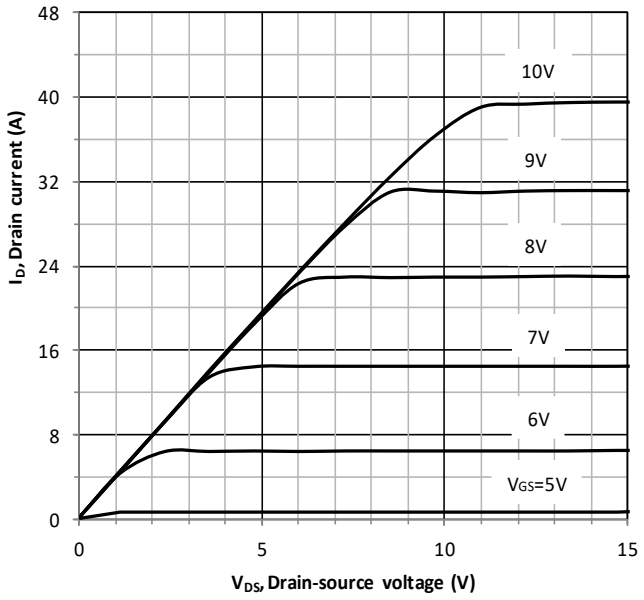
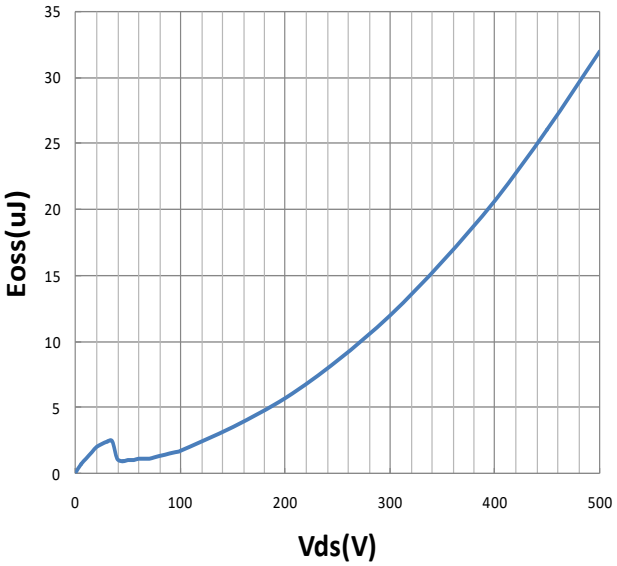
Diagram 1: Typ. output characteristics	Diagram 2: Typ. Coss stored energy
	
I_D=f(V_{DS});T_j=25 °C; parameter: V_{GS}	*Eoss=f(VDS)*

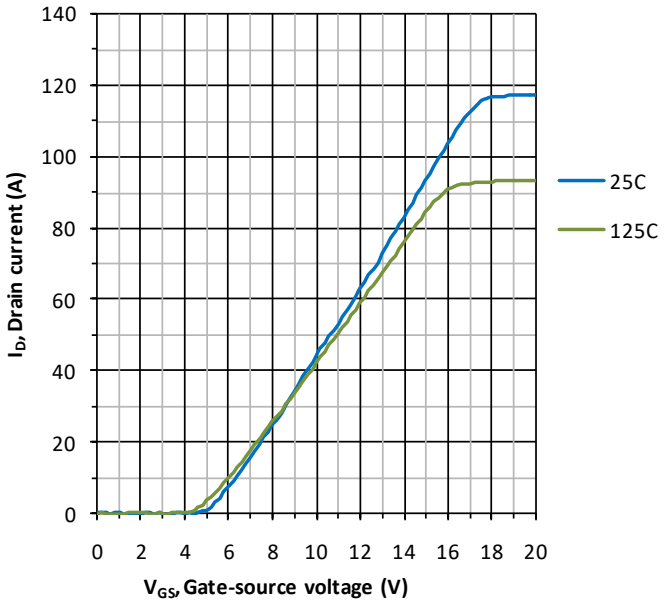
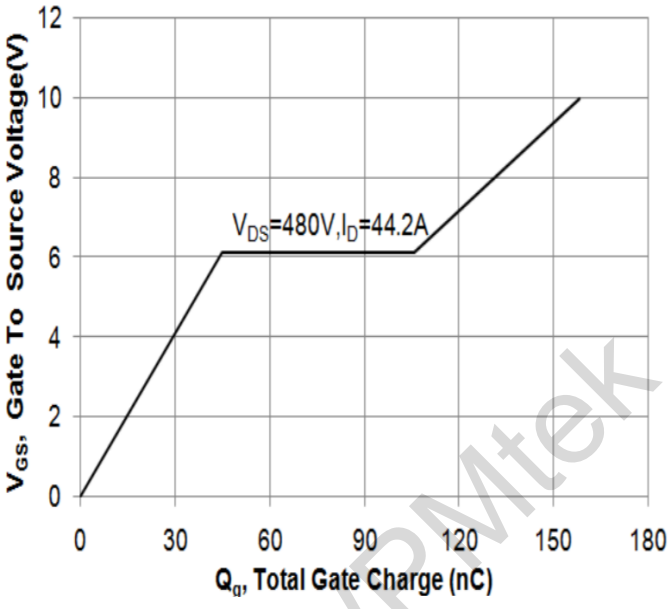
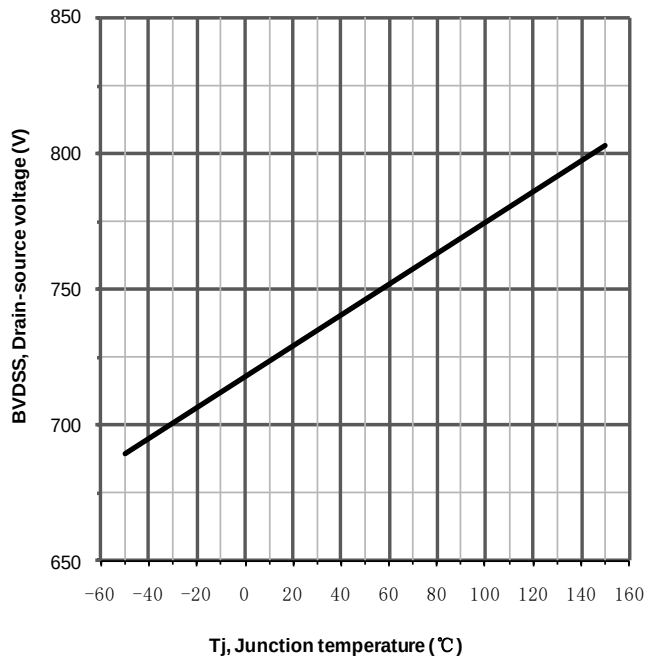
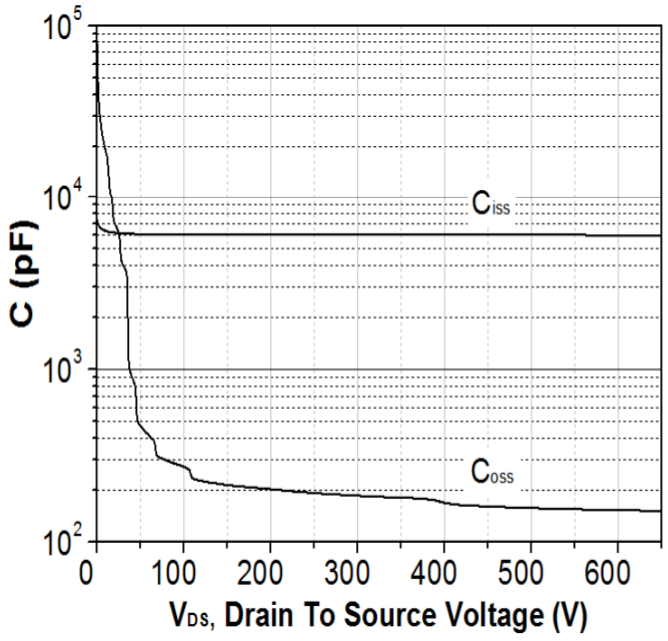
Diagram 3: Typ. transfer characteristics	Diagram 4: Typ. gate charge
	
I_D=f(V_{GS});parameter: T_j	V_{GS}=f(Q_{gate});I_D=44.2A pulsed; parameter: V_{DD}

Diagram 5: Drain-source breakdown voltage



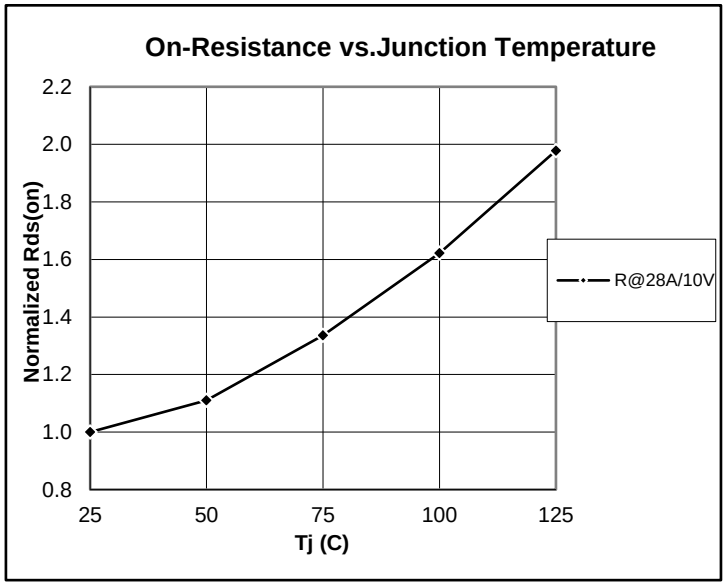
$V_{BR(DSS)}$=f(T_j);I_D=10mA

Diagram 6: Typ. capacitances



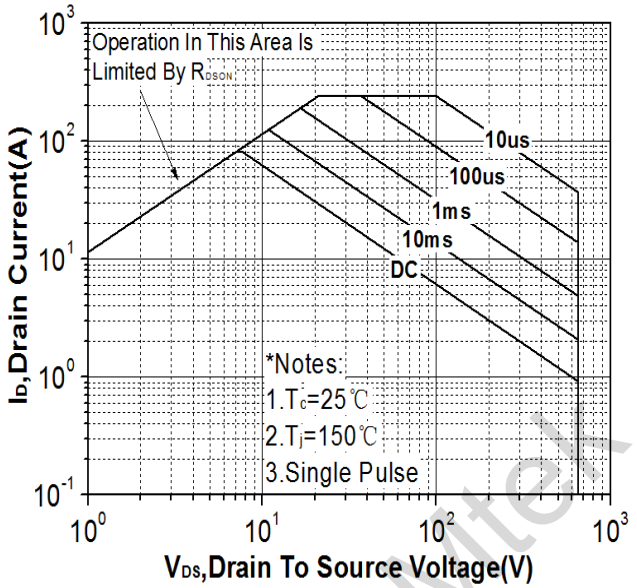
C=f(V_{DS});V_{GS}=0V; f=10 kHz

Diagram7:Typ. On-Resistance vs. Junction Temperature



$R_{ds(on)}$=f(T_j);Vgs=10V/I_D=28A

Diagram 8: Safe operating area T_C=25 °C，TO247



I_D=f(V_{DS}); T_C=25 °C; V_{GS}> 7V; D=0; parameter tp

Test Circuits

Table 8 Diode characteristics

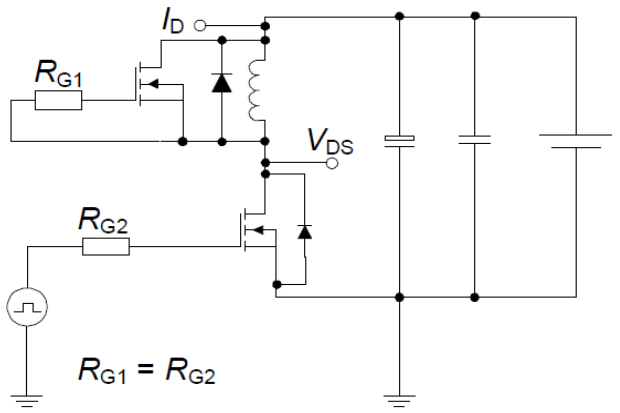
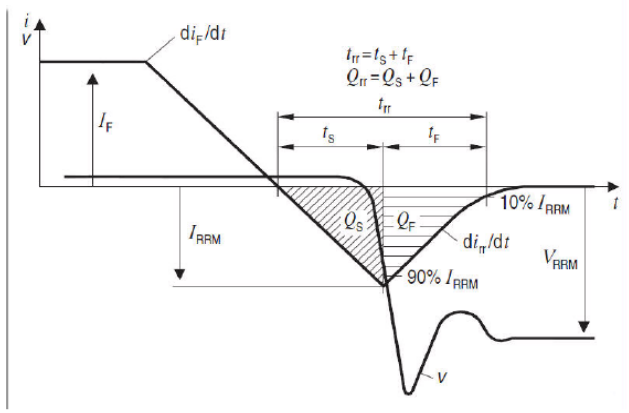
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

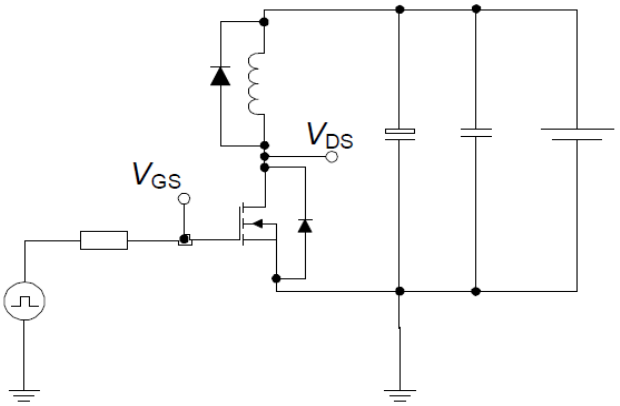
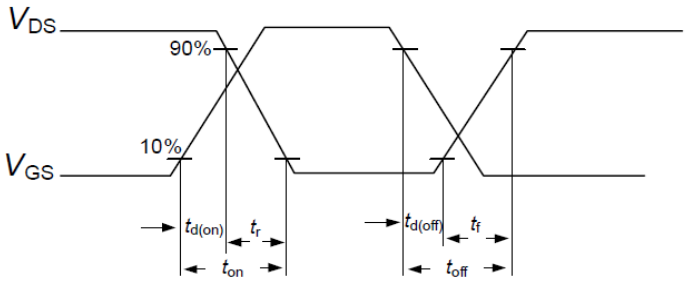
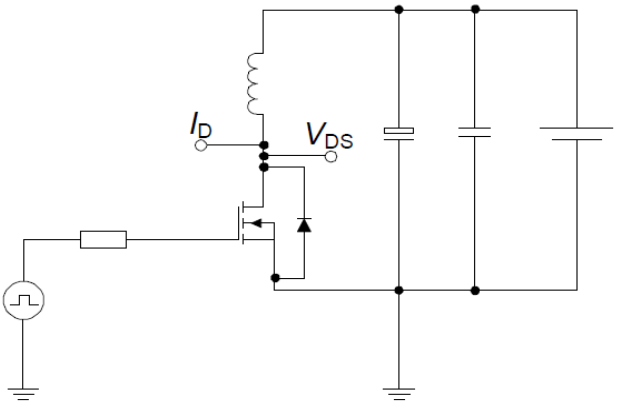
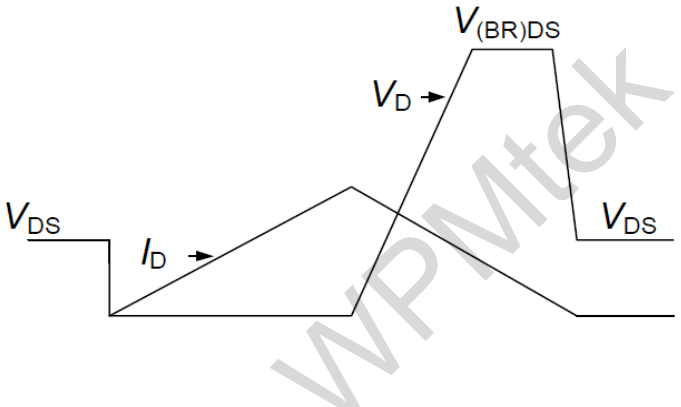
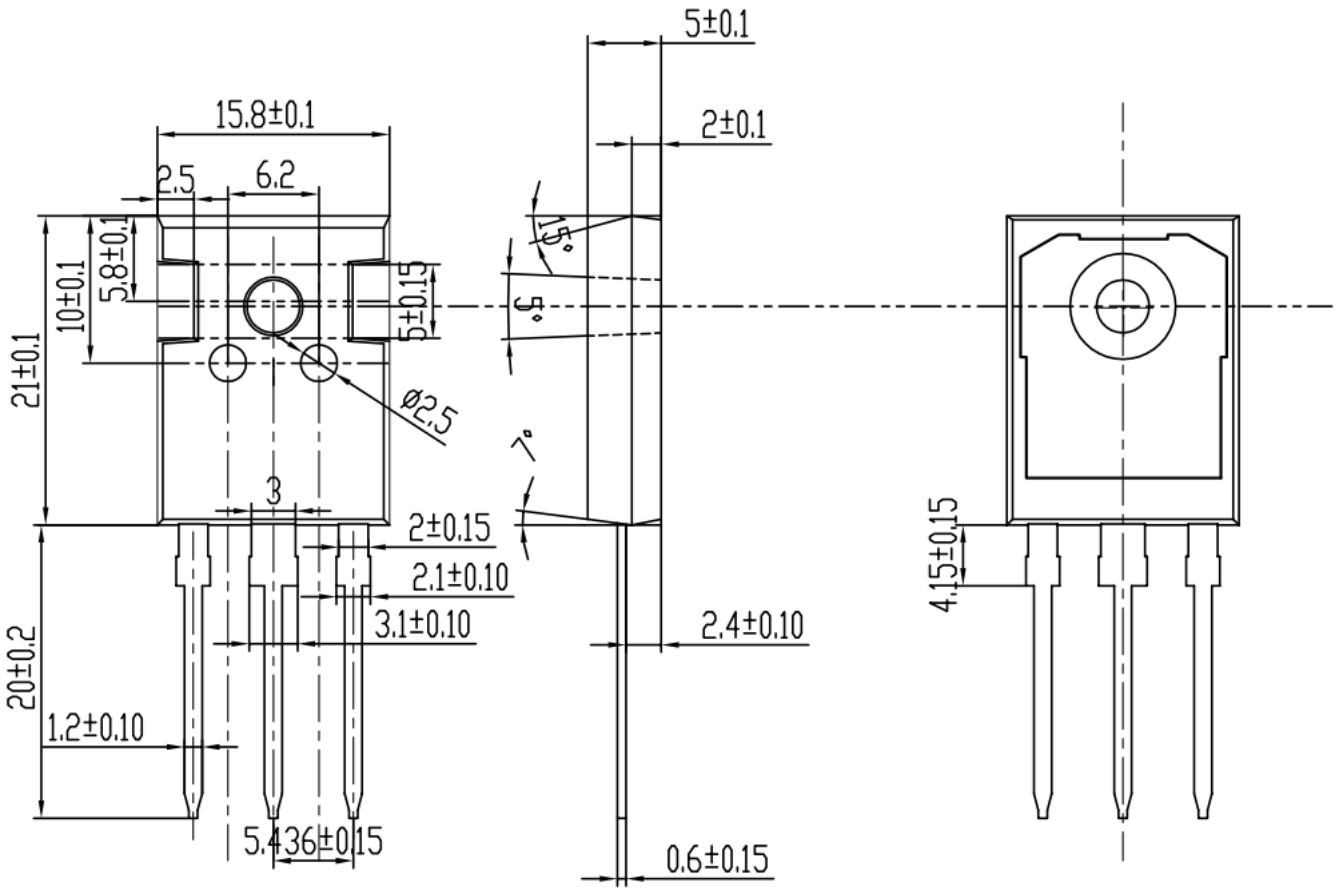
Switching times test circuit for inductive load	Switching times waveform
	

Table10 Unclamped inductive load

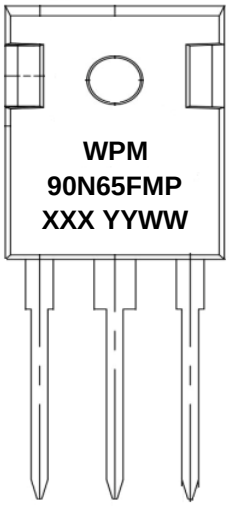
Unclamped inductive load test circuit	Unclamped inductive waveform
	

Package Outlines



Figure： Outline TO247

Marking Information



WPM=WPMtek's Logo
90N65FMP=Marking
XXX YYWW=Date Code