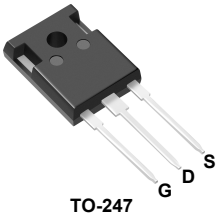
Applications

For Soft Switching Boost PFC switch, HB or AHB or LLC half bridge and full bridge topologies.
Such as phase-shift-bridge(ZVS),LLCLLC Application-Server Power,Telecom Power, EV Charging,Solar inverter.



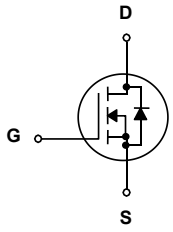
TO-247

Features

Low drain-source on-resistance: RDS(ON) = 0.056Ω (typ.)
Easy to control Gate switching
Enhancement mode: Vth = 2.5 to 4.5 V

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	68	mΩ
$Q_{g,typ}$	87.22	nC
I_D	54	A



Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D		-	54	A	T_C=25°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	162	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	807	mJ	
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	357	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	
Operating junction temperature	T_j	-55	-	150	°C	
Continuous diode forward current	I_S	-	-	48	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	162	A	T_C=25°C
Reverse diode dv/dt[3]	dv/dt	-	-	15	V/s	V_R=400V, I_F=25 A, di_F/dt=100A/µs; see table 8

1) Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
2) Pulse width t_p limited by $T_{j,max}$
3) Identical low side and high side switch with identical R_G

Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.43	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint

Table 4 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.68	-	V	V_{GS}=0V, I_F=3.8 A, T_j=25°C
Reverse recovery time	t_{rr}	-	458.8	-	ns	V_R=400V, I_F=25.8A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	8.739	-	uC	V_R=400V, I_F=25.8A, di_F/dt=100A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	39.6	-	A	V_R=400V, I_F=25.8A, di_F/dt=100A/µs; see table 8

Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	655	-	-	V	V_{GS}=0V, I_D=10mA
Gate threshold voltage	$V_{(GS)th}$	2.5		4.5	V	V_{DS}=V_{GS}, I_D=250uA
Zero gate voltage drain current	I_{DSS}	-	-	1	uA	V_{DS}=655V, V_{GS}=0V, T_j=25°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=30V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.056	0.068	Ω	V_{GS}=10V, I_D=14A, T_j=25°C
Gate resistance	R_G	-	12.6	-	Ω	f=1MHz, open drain

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	6884	-	pF	V_{GS}=0V, V_{DS}=50V, f=1MHz
Output capacitance	C_{oss}	-	440	-	pF	V_{GS}=0V, V_{DS}=50V, f=1MHz
Reverse transfer capacitance	C_{rss}		9.0		pF	V_{GS}=0V, V_{DS}=50V, f=1MHz
Turn-on delay time	$t_{d(on)}$	-	34.4	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=25.8A, R_G=1.7Ω; see table 9
Rise time	t_r	-	27.2	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=25.8A, R_G=1.7Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	185	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=25.8A, R_G=1.7Ω; see table 9
Fall time	t_f	-	22	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=25.8A, R_G=1.7Ω; see table 9

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	19.13	-	nC	V_{DD}=400V, I_D=25.8A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	39.46	-	nC	V_{DD}=400V, I_D=25.8A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	87.22	-	nC	V_{DD}=400V, I_D=25.8A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	6.4	-	V	V_{DD}=400V, I_D=25.8A, V_{GS}=0 to 10V

[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Test Circuits

Table 8 Diode characteristics

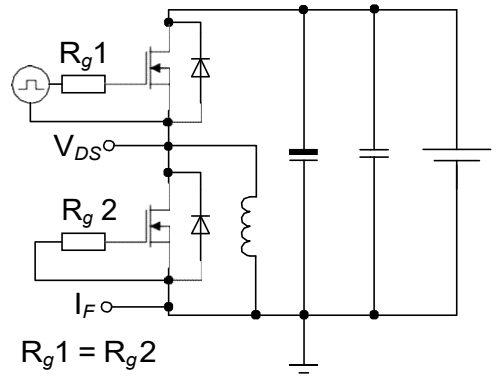
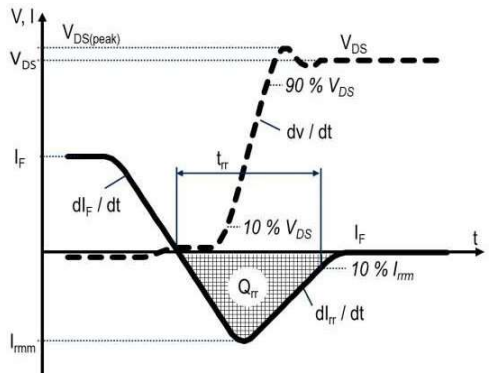
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

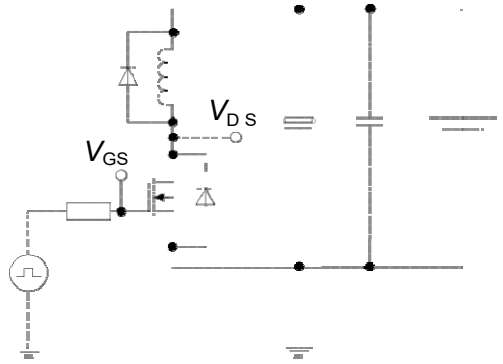
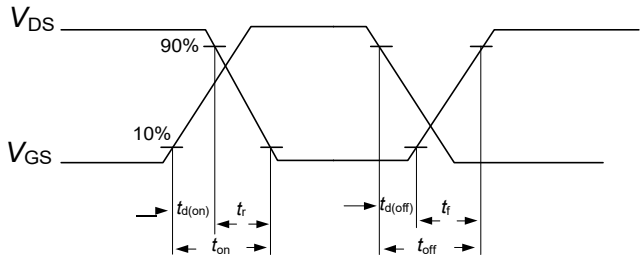
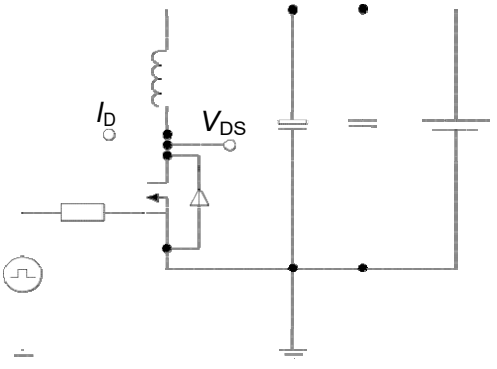
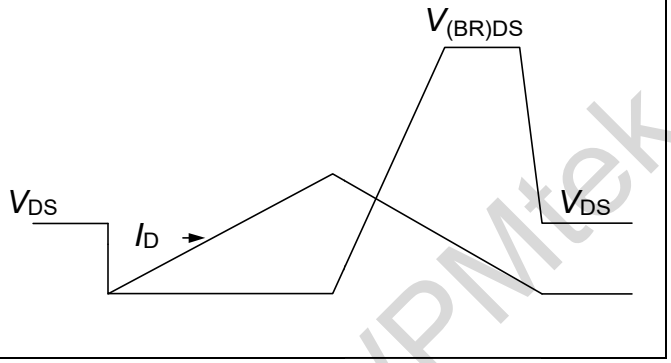
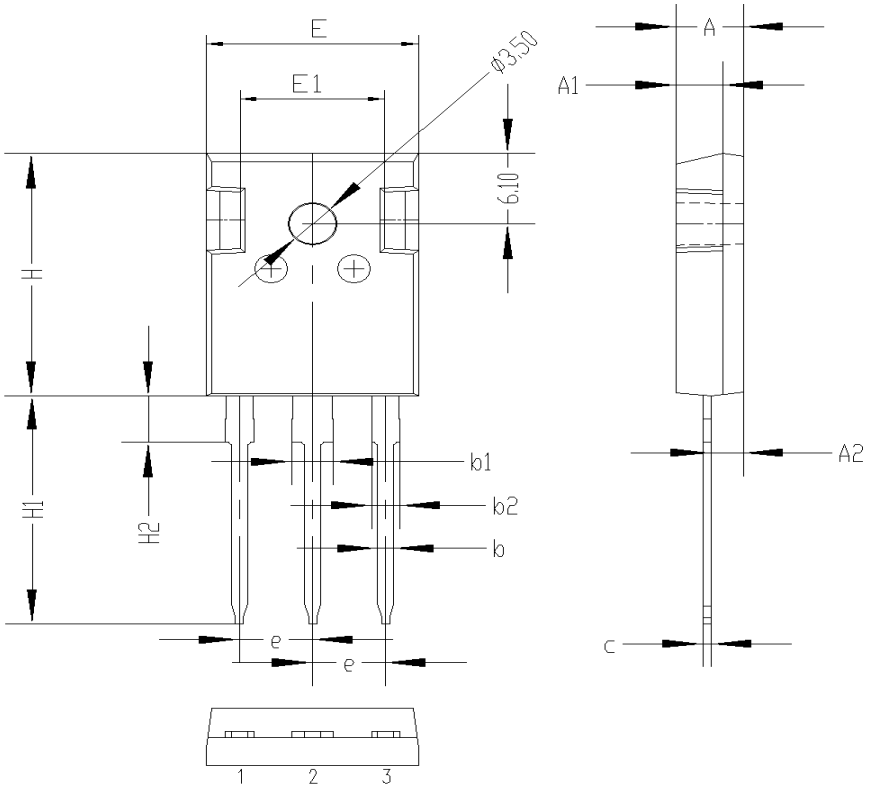
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

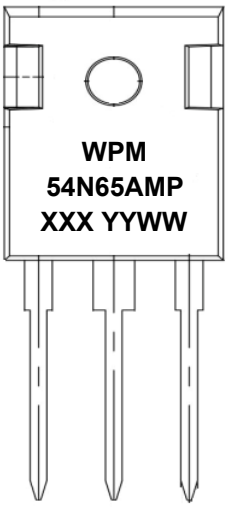
Package Outlines



	单位: mm		
	MIN	NOM	MAX
A	4.8	5	5.2
A1	3.3	3.5	3.7
A2	2.1	2.3	2.5
b	1	1.2	1.4
b1	2.9	3.1	3.3
b2	1.9	2.1	2.3
c	0.4	0.6	0.8
e	5.25	5.45	5.65
E	15.6	15.8	16
E1	10.6	10.8	11
H	20.8	21	21.2
H1	19.4	19.9	20.4
H2	3.9	4.1	4.3
G	5.9	6.1	6.3
ØP	3.3	3.5	3.7

Figure1：Outline PG-TO247

Marking Information



WPM=WPMtek's Logo
54N65AMP=Marking
XXX YYWW=Date Code