GS4917

80mW，Capless，Stereo Headphone Amplifier with Shutdown

Features

- **Supply Voltage Range: 2.7V ~ +5.5V**
- **GS4917A: External Feedback Gain Network**
  GS4917B: Fixed -2V/V Gain
- **Capless Structure**
  Eliminates Ground-Referenced Outputs
  Eliminates Output DC-Blocking Capacitors
  Provides Flat Frequency Response
- **80mW into 32Ω Load from 5V Power Supply at THD+N = 0.1% (Typical, per Channel)**
- **THD+N =0.02% (f = 1kHz)**
- **High PSRR: -78dB (at 217Hz)**
- **Quiescent Current:2.7mA (TYP)**
- **Shutdown Control**
- **Short-Circuit and Thermal-Overload Protections**
- **Under-Voltage Lockout Function**
- **Enhanced Noise Cancellation by Differential Inputs**
- **Operating Temperature: -40°C ~ +85°C**
- **Available in a Green QFN-3X3-16 Package**

General Description

The GS4917 is stereo headphone amplifier which is designed for portable applications and can operate from a 2.7V to 5.5V single supply. Capless design can produce a ground-referenced output from a single power supply, and can eliminate output DC-blocking capacitors for less-component height and low-cost. For GS4917-BFR, the internal gain setting (-2V/V) is to further reduce component count. For GS4917-AFR, the gain can be adjusted by external feedback resistors.

The GS4917 has low quiescent current 2.7mA at 5V supply, low 0.02% THD+N, 80mW per channel into 32Ω load from 5V power supply at THD+N = 0.1%. The high supply rejection ratio (PSRR) of -78dB at 217Hz allows the device to operate from noisy digital supplies without an additional linear regulator. The device provides short-circuit and thermal-overload protections. Build-in shutdown control also helps for pop/click-free on/off control.

The GS4917 is available in a Green QFN-3×3-16 package. It operates over an ambient temperature range of -40℃ to +85℃

Applications

- Smart Phone
- Notebook PCs
- Portable Audio Equipment
- PDAs

Package/Ordering Information

MODEL	ORDER NUMBER	PACKAGE DESCRIPTION	PACKAGE OPTION	MARKING INFORMATION
GS4917	GS4917-AFR	QFN3X3-16	Tape and Reel,5000	GS4917A
	GS4917-BFR			GS4917B

- **Absolute Maximum Ratings**

Condition	Min	Max
Supply Voltage Range	+2.7V	+5.5V
PV_{SS} to SV_{SS}	-0.3V	+0.3V
PGND to SGND	-0.3V	+0.3V
PV_{DD} to SV_{DD}	-0.3V	+0.3V
PV_{DD} and SV_{DD} to PGND or SGND	-0.3V	+6V
PV_{SS} and SV_{SS} to PGND or SGND	-6V	+0.3V
IN to SGND	SV_{SS}-0.3V	SV_{DD}+0.3V
$\overline{SHDN}$ to SGND	-0.3V	SV_{DD}+0.3V
OUT to SGND	SV_{SS}-0.3V	SV_{DD}+0.3V
C1P to PGND	-0.3V	PV_{DD}+0.3V
C1N to PGND	PV_{SS}-0.3V	+0.3V
Output Short Circuit to GND or V_{DD}	Continuous	
Junction Temperature	+150°C	
Storage Temperature Range	-65°C	+150°C
Operating Temperature Range	-40°C	+85°C
Lead Temperature (soldering, 10sec)	+260°C	
Package Thermal Resistance (T_A=+25℃)		
QFN3X3-16, θ_{JA}	130°C/W	
ESD Susceptibility		
HBM	6KV	
CDM	2KV	
Latch up	200mA	

Note: Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. GAINSIL recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

Pin Configuration

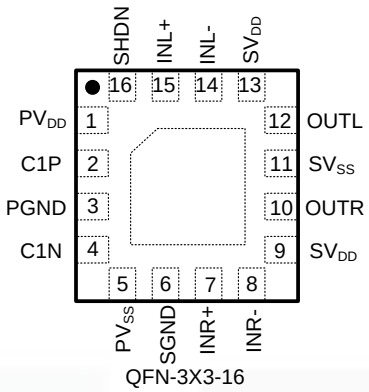


Figure 1. Pin Assignment Diagram

PIN DESCRIPTION

Pin	Name	Function
1	PV_{DD}	Charge-Pump Power Supply. Powers charge-pump inverter, charge-pump logic, and oscillator. Connect to positive supply (2.7V to 5.5V). Bypass with a 1µF capacitor to PGND as close to the pin as possible.
2	C1P	Positive Terminal for Flying Capacitor. Connect a 1µFcapacitor to C1N.
3	PGND	Power Ground. Connect to ground.
4	C1N	Negative Terminal for Flying Capacitor. Connect a 1µF capacitor to C1P.
5	PV_{SS}	Charge-Pump Output. Connect to SV_{SS}.
6	SGND	Signal Ground. Connect to ground.
7	INR+	Noninverting Right-Channel Audio Input.
8	INR-	Inverting Right-Channel Audio Input.
9，13	SV_{DD}	Amplifier Positive Power Supply. Connect to positive supply (2.7V to 5.5V). Bypass with a 1µF capacitor to SGND as close to the pin as possible.
10	OUTR	Output for Right-Channel.
11	SV_{SS}	Amplifier Negative Power Supply. Connect to PV_{SS}.
12	OUTL	Output for Left-Channel.
14	INL-	Inverting Left-Channel Audio Input.
15	INL+	Noninverting Left-Channel Audio Input.
16	$\overline{SHDN}$	Active-Low Shutdown Input.
Exposed Pad	—	Exposed Pad. Can be connected to GND or left floating.

Electrical Characteristics

(PV_{DD} = SV_{DD} = 5V, PGND = SGND = 0V, SHDN = SV_{DD}, C1 = C2 = 1μF, R_L = ∞, resistive load referenced to ground; for GS4917-AFR, gain = -1V/V (R_{IN} = R_F = 10kΩ); for GS4917-BFR, gain = -2V/V (internally set). T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	GS4917			
			TYP	MIN	MAX	UNITS
General						
Supply Voltage Range	V_{DD}			2.7	5.5	V
Quiescent Supply Current	I_{DD}		2.7		4	mA
Shutdown Supply Current	I_{SHDN}	$\overline{SHDN}$ = SGND = PGND	0.01		8	μA
$\overline{SHDN}$ Input Logic High	V_{IH}			1.2		V
$\overline{SHDN}$ Input Logic Low	V_{IL}				0.4	V
$\overline{SHDN}$ to Full Operation Time	t_{SON}		3.2			ms
Amplifiers						
Voltage Gain	A_V	GS4917-BFR	-2	-2..12	-1.88	V/V
Gain Matching	ΔA_V	GS4917-BFR, between the right and left channels	0.2			%
Output Offset Voltage	V_{OS}	Between IN+ and IN-,input AC-coupled to ground(GS4917-AFR)	1.1	-3	3	mV
Input Impedance	R_{IN}	GS4917-BFR, measured at INL and INR	14.6	12.5	17	kΩ
Common-Mode Voltage Range	CMRR	Input referred, GS4917-AFR	99			dB
Power Supply Rejection Ratio	PSRR	f = 217Hz, V_{RIPPLE} =200mV_{P-P}	107			dB
		f = 10kHz, V_{RIPPLE} =200mV_{P-P}	96			
Output Power	P_{OUT}	R_L = 32Ω，THD+N = 0.1%	80			mW
Output Impedance in Shutdown			2			kΩ
Total Harmonic Distortion Plus Noise	THD+N	R_L = 32Ω，P_{OUT} = 55mW,f = 1kHz	0.02			%
Signal-to-Noise Ratio	SNR	R_L = 32Ω， P_{OUT} = 20mW,BW< 20kHz	100			dB
Capacitive Drive	C_L	No sustained oscillation	200			pF
Charge-Pump Oscillator Frequency	f_{OSC}		420	200	500	kHz
Crosstalk		R_L = 32Ω，V_{IN} = 200mV_{P-P},f = 10kHz,A_V = -1V/V	72			dB
Thermal Shutdown Threshold			140			℃
Thermal Shutdown Hysteresis			10			℃

Typical Performance characteristics @T_A=+25℃, V_{DD}=5V/3V INP=INM= V_{CM} =0V , R_{LOAD}=NC ;

SHDN=1

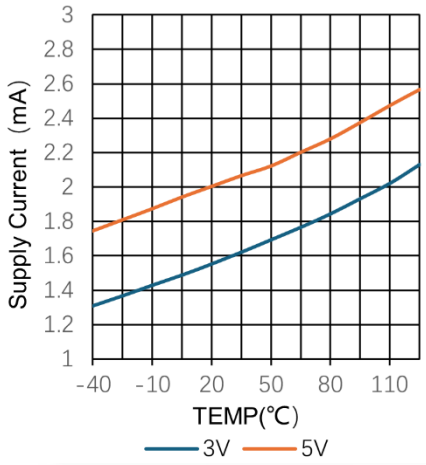


Figure 2. Supply Current vs Temperature

SHDN=0

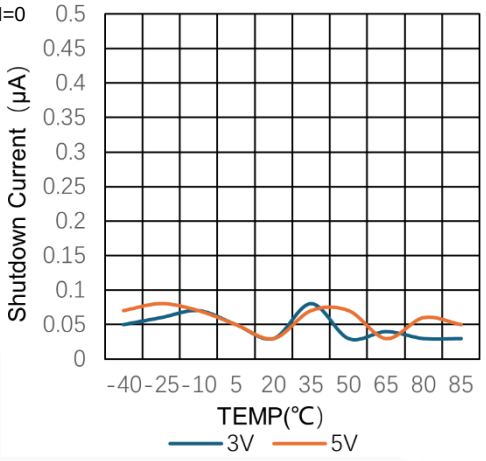


Figure 3. Shutdown Current vs Temperature

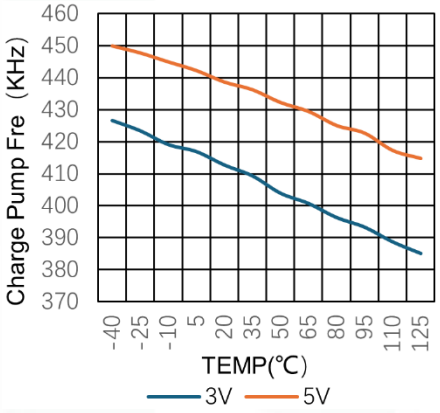


Figure 4. Charge Pump Fre vs Temperature

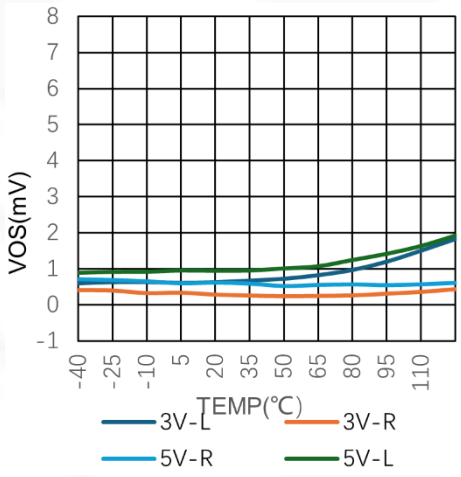


Figure 5.VOS vs Temperature

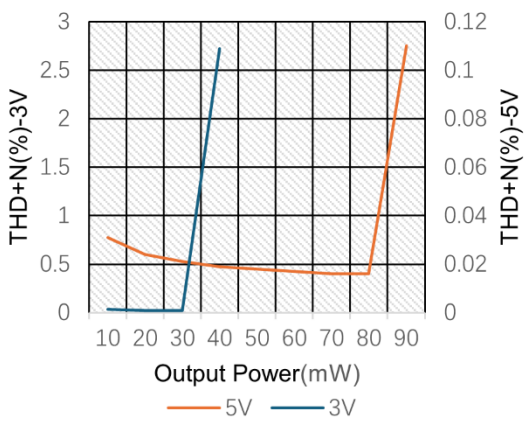


Figure 6. THD+N vs Output Power （double）

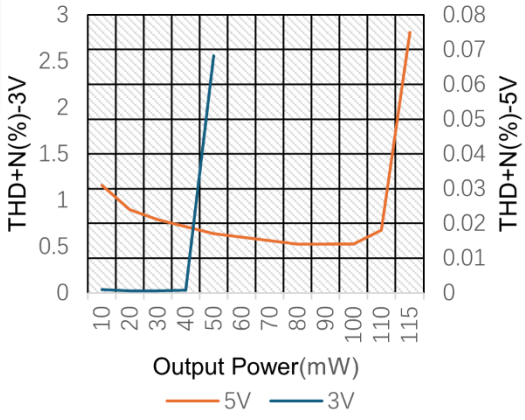


Figure 7. THD+N vs Output Power（single）

Typical Performance characteristics

（@T_A=+25℃, V_{DD}=5.5V/2.7V INP=INM=V_{CM}=0V，f=10kHz，R_{LOAD}=32Ω）

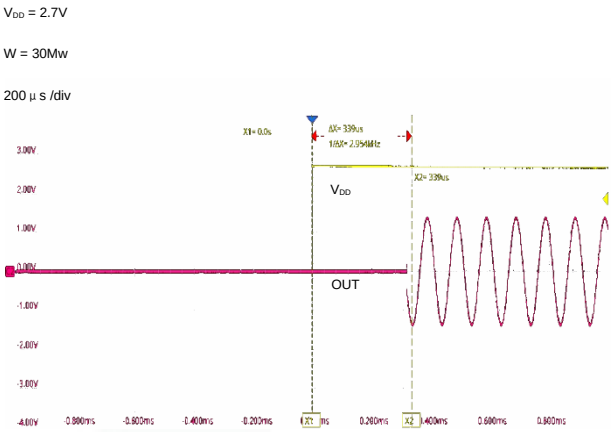


Figure 8. Turn On Time vs Supply Voltage（OUT）

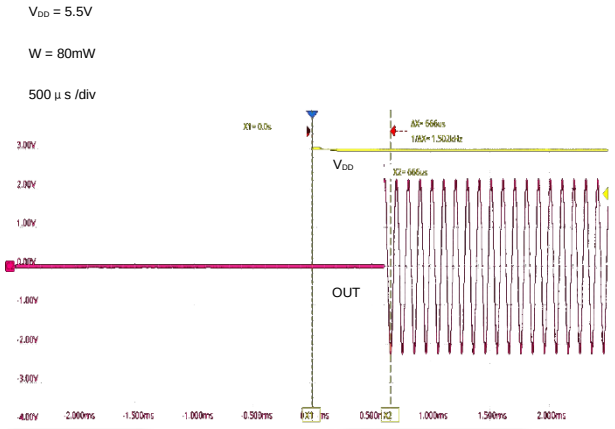


Figure 9. Turn On Time vs Supply Voltage（OUT）

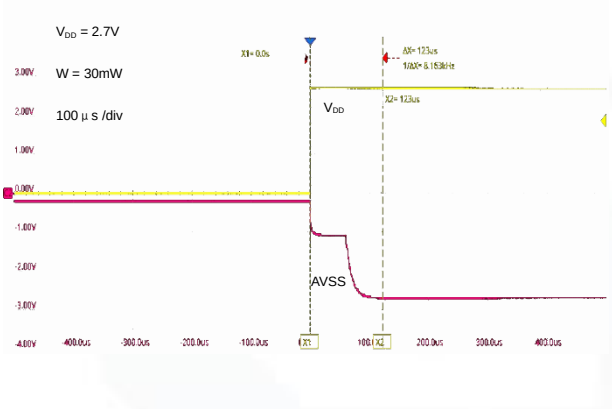


Figure 10. Turn On Time vs Supply Voltage（AVSS）

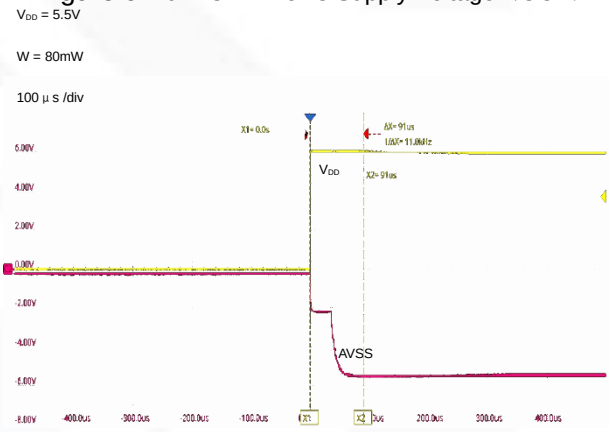


Figure 11. Turn On Time vs Supply Voltage（AVSS）

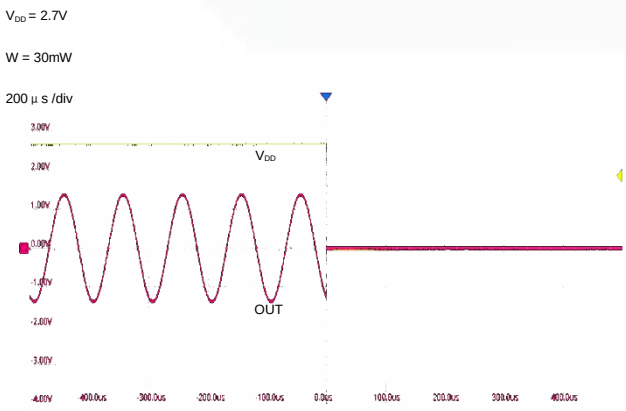


Figure 12. Turn Off Time vs Supply Voltage（OUT）

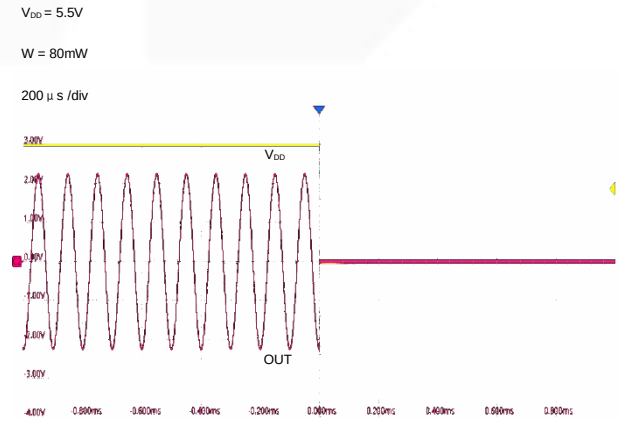


Figure 13. Turn Off Time vs Supply Voltage（OUT）

Typical Performance characteristics （@T_A=+25℃, V_{DD}=5V/3V INP=INM= V_{CM} =0V，R_{LOAD}=NC）

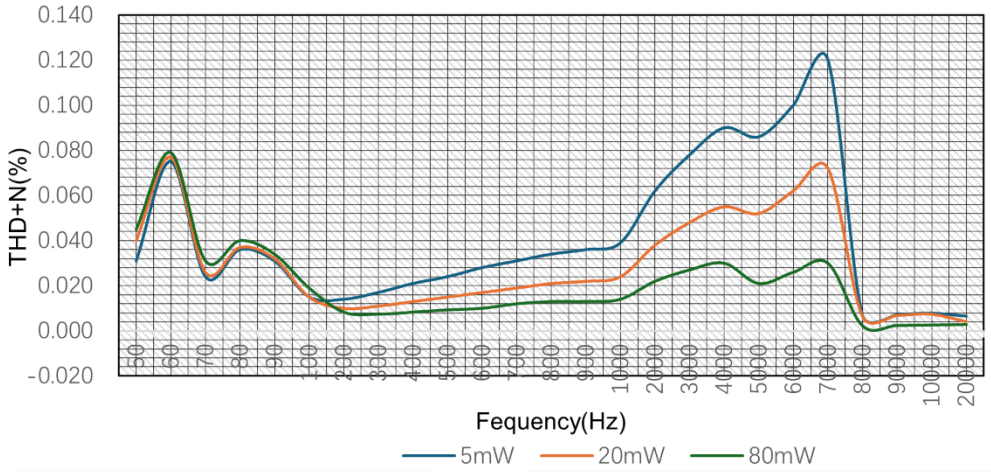


Figure 14. THD+N vs Frequency（5V）

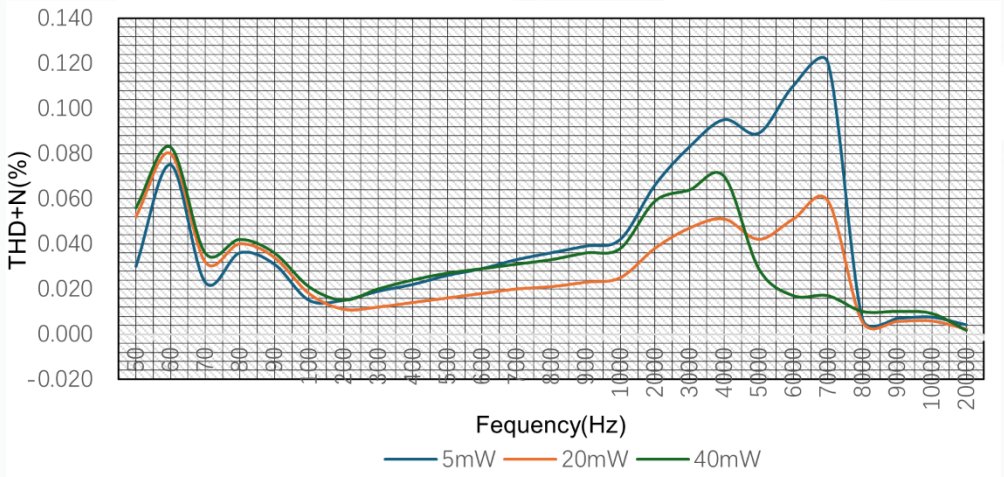


Figure 15. THD+N vs Frequency（3V）

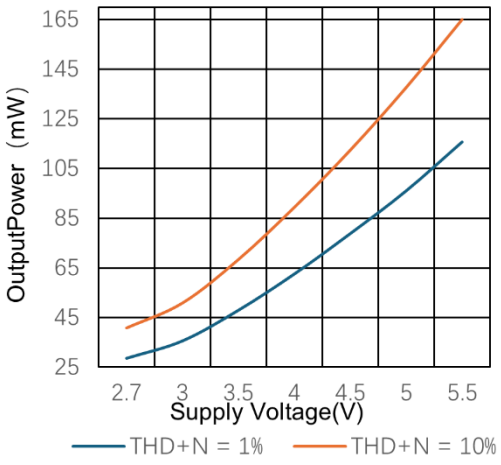


Figure 16. Output Power vs Supply Voltage（double）

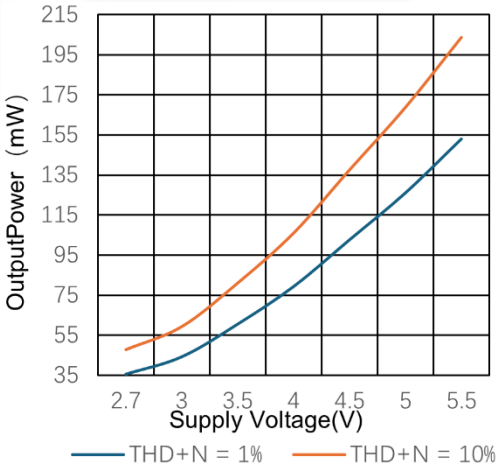
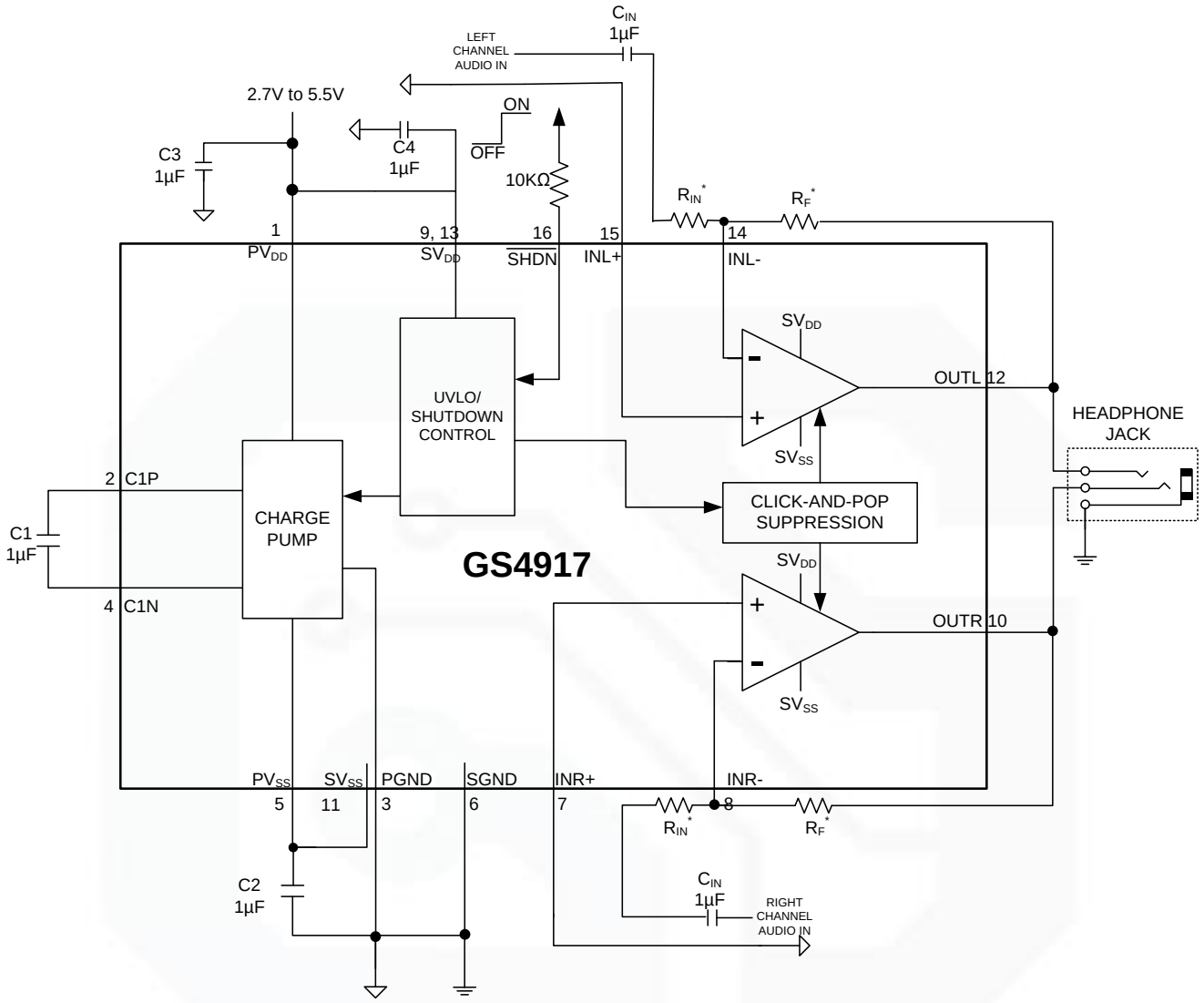


Figure 17. Output Power vs Supply Voltage（single）

FUNCTIONAL DIAGRAM/TYPLCAL APPLICATION CIRCUIT



* GS4917A, R_{IN} AND R_F are external to device.

GS4917B, R_{IN} = 15kΩ，R_F = 30kΩ, R_{IN} and R_F are inside the device

Figure 18. Typical Single-Ended Input Application Circuit

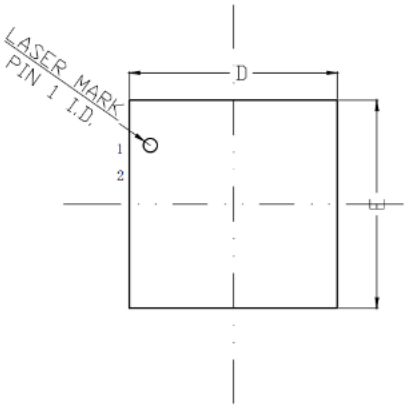
NOTES:

1.To ensure the normal operation of the device, decoupling capacitor (C3) must be placed as close to GS4917 as possible. The loop length formed by C3, SV_{DD} and GND should be no longer than 1.2cm; otherwise the device will not start up at high supply voltage.

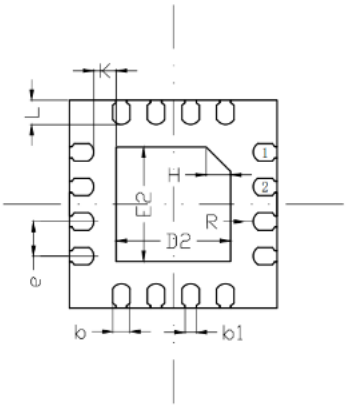
2.In order to get good performance, it's important to select the right C1, C2 and C3 in application. All tests are performed with circuit set up with X5R and X7R capacitors. Capacitors having high dissipative loss, such as Y5V capacitor, may cause performance degradation and unexpected system behavior.

Package Information

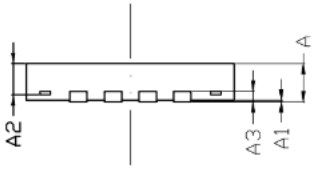
QFN3X3-16



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2	0.40	0.45	0.50
A3		0.15REF	
b	0.18	0.25	0.30
b1		0.16REF	
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.55	1.65	1.75
E2	1.55	1.65	1.75
e	0.40	0.50	0.60
H		0.35REF	
K	0.30	--	--
L	0.30	0.35	0.40
R	0.14	--	--