

NAU88L24

Ultra-Low Power Audio CODEC with Stereo Class D Drivers and Ground-Referenced Headphone Amplifier with Advanced Headset Detection

GENERAL DESCRIPTION

The NAU88L24 is an ultra-low power high performance audio codec designed for smartphone, tablet PC, and other portable devices that supports both analog and digital audio functions. It includes one I2S/PCM interface, one digital mixer, two high quality DACs, two high quality ADCs, two mono differential or one stereo differential analog microphone inputs, four analog single-ended microphone inputs, four digital PDM microphone inputs, one single ended stereo auxiliary or one differential mono inputs, one differential HS mic input, one stereo 2.9W class D loudspeaker amplifier driver for 4 Ω loading and 5V supply, and one stereo class G headphone amplifier with automatic headset detection.

The advanced on-chip signal processing engine that includes dynamic range compressors (DRC), 5-band parametric equalizer (PEQ), and programmable high pass and notch filter block, can maximize audio quality and eliminate any undesirable frequency components.

The NAU88L24 also has powerful headset detection that supports jack insertion / ejection, microphone detection, distinct key / short key / long key / key release detection features as well as an integrated frequency locked loop (FLL) to support various clocks.

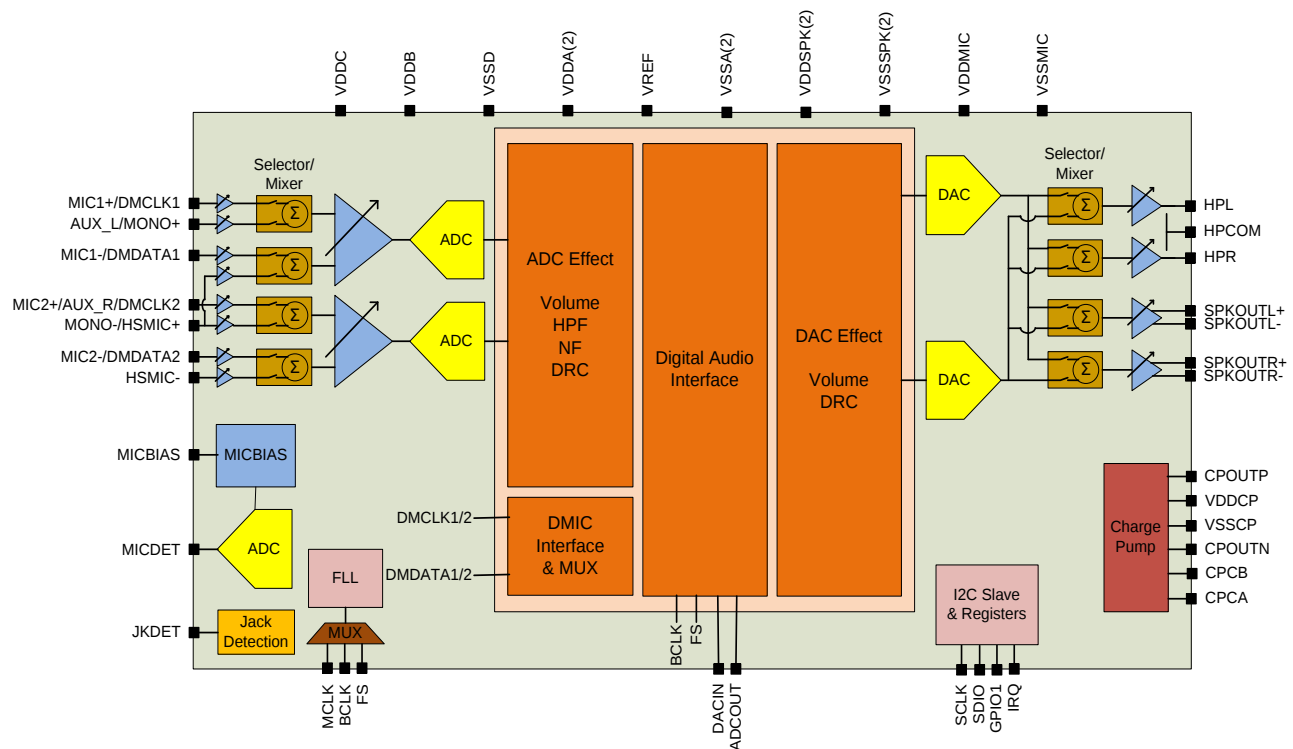
FEATURES

- DAC: 103dB SNR (A-weighted) @ 0dB gain, 1.8V and -77dB THD @ 20mW and RL= 32 Ω , DAC playback to headphone output mode
- ADC: 100dB SNR (A-weighted) @ 0dB MIC gain, 1.8V, Fs = 48KHz and -85dB THD, 1.8V, MIC gain 6dB, OSR 128x
- 1 Digital I2S/PCM I/O port
- Dynamic Range Compressor (DRC)
- 5 Band Parametric Equalizer
- 1 Headset Microphone, 4 Analog or 4 Digital PDM MIC input supports
- Stereo .97W Class D Loudspeaker @ 4.2V, 8 Ω , 1% THD+N (1.38W @ 5.0V, 8 Ω , 1% THD+N)
- Class G Headphone Amplifier (27mW @ 32 Ω , 1% THD+N)
- Stereo Auxiliary Input
- Sampling rate from 8K to 96 KHz
- Headset Detection
- Jack Insertion and Ejection Detection
- MIC Detection and Distinct Keys Detection
- Package:
QFN-48 (6X6mm, 0.4mm Pitch) package
WLCSP-56 package with 0.4mm Pitch package
Package is Halogen-free, RoHS-compliant and TSCA-compliant

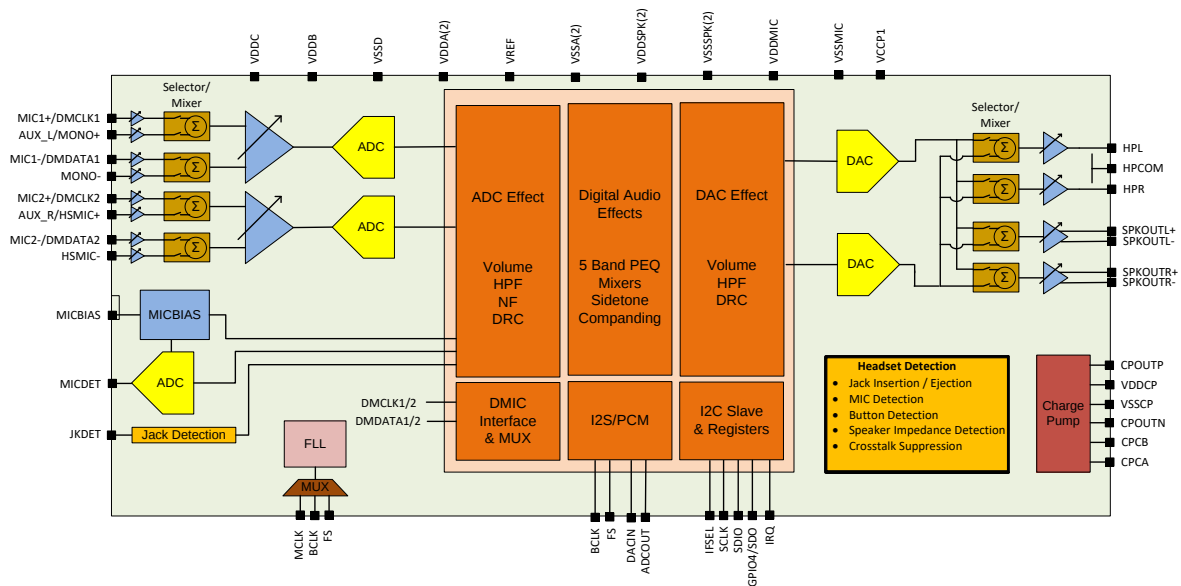
Applications

- Tablets / Ultra-Portable Laptops
- Smartphones
- Audio Docking Systems
- Portable Game Players
- Cameras

Block Diagram



QFN 48



56 Balls WLCSP

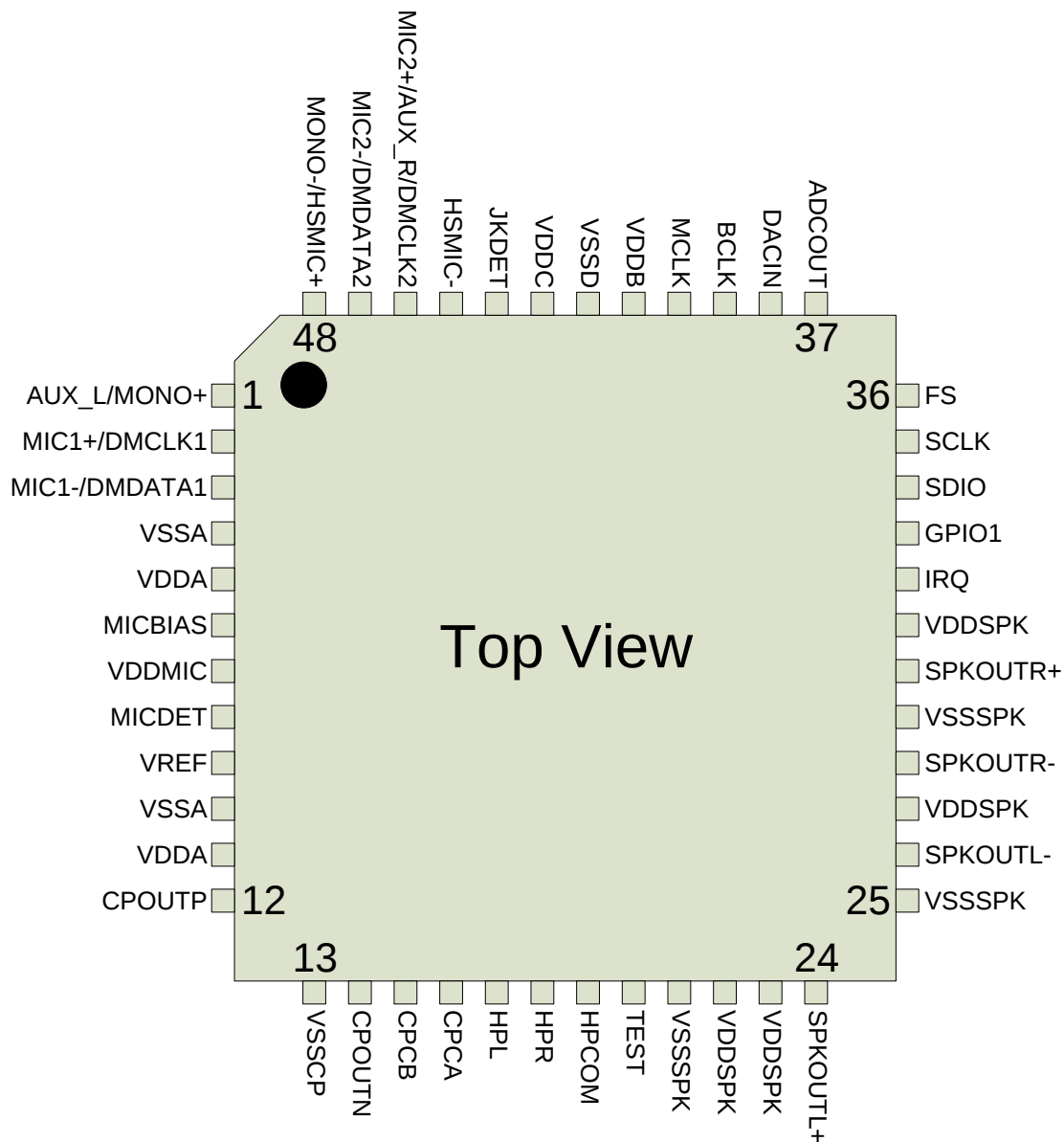
Table of Contents

BLOCK DIAGRAM	2
PIN DIAGRAM-QFN48.....	6
PIN DIAGRAM-WLCSP.....	7
Ordering Information.....	7
PIN DESCRIPTION-QFN48.....	8
PIN DESCRIPTION-56 BALLS WLCSP	10
ELECTRICAL CHARACTERISTICS	12
1 GENERAL DESCRIPTION.....	15
1.1 Inputs	15
1.2 Outputs	15
1.3 ADC, DAC and Digital Signal Processing	15
1.4 Digital Interfaces	15
2 POWER SUPPLY	15
2.1 Power on and off reset.....	16
3 INPUT PATH DETAILED DESCRIPTIONS	16
3.1 Analog Microphone Inputs	16
3.1.1 V _{REF}	17
3.1.2 MIC Bias	18
3.2 Digital MIC Inputs.....	18
3.3 Line Inputs	19
3.4 Programmable Gain Amplifier (PGA)	19
4 ADC DIGITAL BLOCK.....	19
4.1 ADC Dynamic Range Compressor (DRC)	20
4.1.1 Level Estimation	20
4.1.2 Static Curve	20
4.2 ADC Digital Volume Control.....	22
4.3 ADC Programmable High Pass Filter.....	22
4.4 Programmable Notch Filter	23
4.5 ADC Path Digital Mixer	24
4.6 5-Band Equalizer	24
4.7 Companding.....	25
4.8 Additional ADC Application Notes.....	25
5 DAC DIGITAL BLOCK.....	25
5.1 DAC Dynamic Range Control (DRC)	26
5.1.1 Level Estimation	26
5.1.2 Static Curve	26
5.2 DAC Digital Volume Control.....	27
5.3 DAC Soft Mute	27
5.4 5-Band Equalizer	28
5.5 DAC Path Digital Mixer with Side tone.....	28
5.6 Companding.....	29

5.6.1	μ-law	30
5.6.2	A-law	30
5.7	Additional DAC Application Notes	30
6	CLOCKING AND SAMPLE RATES	30
6.1	Frequency Locked Loop (FLL)	32
7	CONTROL INTERFACES	34
7.1	2-Wire-Serial Control Mode (I ² C Style Interface)	35
7.2	2-Wire Protocol Convention	35
7.3	2-Wire Write Operation	35
7.4	2-Wire Read Operation	36
7.5	Digital Serial Interface Timing	36
7.1	Four-Wire SPI Control Interface	37
7.1.1	Four-Wire SPI Write Operation	37
7.1.2	Four-Wire SPI Read Operation	38
7.2	Software Reset	40
8	DIGITAL AUDIO INTERFACES	40
8.1	Right-Justified Audio Data	40
8.2	Left-Justified Audio Data	41
8.3	I2S Audio Data	41
8.4	PCM A Audio Data	41
8.5	PCM B Audio Data	42
8.6	PCM Time Slot Audio Data	42
8.7	TDM I2S Audio Data	43
8.8	TDM PCM A Audio Data	43
8.9	TDM PCM B Audio Data	43
8.10	TDM PCM Offset Audio Data	44
9	OUTPUTS	45
9.1	Stereo Class D Speaker Outputs	45
9.1.1	Differential Mixer	45
9.1.2	Device Protection	46
9.1.3	Class D without filter	46
9.1.4	Class D Filters	47
9.1.5	NAU88L24 EMI performance	48
9.2	Class G Headphone Driver and Charge Pump	48
10	HEADSET DETECTION	49
10.1	Jack Detection	49
10.2	Microphone Detection	50
10.3	Key/Button Detection	50
10.3.1	SAR ADC	53
10.4	Jack Interrupt Sequence	54
10.4.1	Jack Insert	54
10.4.2	Jack Eject	54
10.4.3	Short Key Press	54
10.4.4	Key Release	54

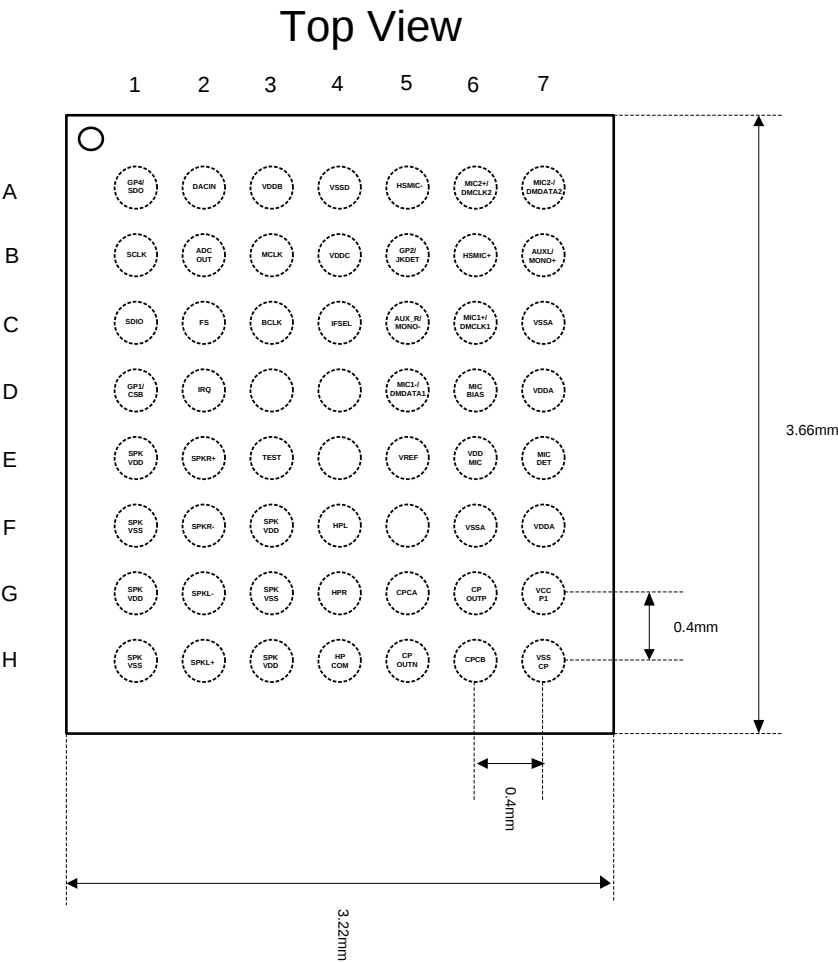
11	BASIC REGISTER SEQUENCES	55
11.1	To enable VREF and General Bias	55
11.2	Enable/Disable Input PGA	55
11.3	Enable analog ADC	55
11.4	Enable/Disable FLL	55
11.5	Enable/Disable DAC	56
11.6	Enable/Disable Class D Driver	56
11.7	Enable/Disable Headphone	56
11.8	Enable DAC to Headphone Low Power MP3 Playback Mode	57
11.9	Enable DAC to Class D Low Power MP3 Playback Mode	57
11.10	Jack Detection	57
12	CONTROL AND STATUS REGISTERS	59
13	TYPICAL APPLICATION DIAGRAM	92
14	PACKAGE INFORMATION	94
14.1	QFN 48L 7X7MM^2	94
14.2	QFN48L 6x6MM^2	95
14.3	WLCSP 56 Balls	96
	ORDERING INFORMATION	97
	REVISION HISTORY	98
	IMPORTANT NOTICE	99

Pin Diagram-QFN48



Note: NAU88L24IG (6mm X 6mm QFN 48 pin) have same pin diagram and pin descriptions

Pin Diagram-WLCSP



Ordering Information

Part Number	Dimension	Package	Package Material
NAU88L24YG	7 x 7 mm	QFN-48	Green
NAU88L24IG	6 X 6 mm	QFN-48	Green
NAU88L24VG	3.22 X 3.66 mm	56 Balls WLCSP	Green

Pin Description-QFN48

Pin #	Name	Type	Functionality
1	AUX_L/MONO +	Analog Input	PGA Mono+ or Left channel Auxiliary Analog Input
2	MIC1+/DMCLK1	Analog Input / Digital Output	PGA MIC1+ Analog Input or Digital Microphone 1 Clock Output
3	MIC1-/DMDATA1	Analog Input / Digital Input	PGA MIC1- Analog Input or Digital Microphone 1 Data Input
4	VSSA	Ground	Analog Supply Ground
5	VDDA	Supply	Analog Supply
6	MICBIAS	Analog Output	Microphone Bias Output
7	VDDMIC	Supply	Microphone supply
8	MICDET	Analog Input	Microphone button detection input
9	VREF	Analog I/O	Internal DAC & ADC voltage reference decoupling I/O
10	VSSA	Ground	Analog Supply Ground
11	VDDA	Supply	Analog Supply
12	CPOUTP	Analog I/O	Charge Pump positive voltage
13	VSSCP	Ground	Charge Pump Supply ground
14	CPOUTN	Analog I/O	Charge Pump negative voltage
15	CPCB	Analog I/O	Charge Pump switching capacitor node B
16	CPCA	Analog I/O	Charge Pump switching capacitor node A
17	HPL	Analog Output	Headphone left channel output
18	HPR	Analog Output	Headphone right channel output
19	HPCOM	Analog Input	Headphone ground reference
20	TEST	N/C	Class-D amplifier Test point
21	VSSSPK	Ground	Class-D amplifier supply ground
22	VDDSPK	Supply	Class-D amplifier supply
23	VDDSPK	Supply	Class-D amplifier supply
24	SPKOUTL+	Analog Output	Class-D amplifier Left Channel positive Output
25	VSSSPK	Ground	Class-D amplifier supply ground
26	SPKOUTL-	Analog Output	Class-D amplifier Left Channel negative Output
27	VDDSPK	Supply	Class-D amplifier supply
28	SPKOUTR-	Analog Output	Class-D amplifier Right Channel negative Output
29	VSSSPK	Ground	Class-D amplifier supply ground
30	SPKOUTR+	Analog Output	Class-D amplifier Right Channel positive Output
31	VDDSPK	Supply	Class-D amplifier supply
32	IRQ	Digital Output	Programmable Interrupt Output
33	GPIO1	Digital I/O	General Purpose IO (I2C)
34	SDIO	Digital I/O	Serial Data for I2C or SPI
35	SCLK	Digital Input	Serial Data Clock for I2C or SPI
36	FS	Digital I/O	Frame Sync input or output for I2S or PCM data
37	ADCOUT	Digital Output	Serial Audio data Output for I2S or PCM data
38	DACIN	Digital Input	Serial Audio data input for I2S or PCM data
39	BCLK	Digital I/O	Serial data bit clock input or output for I2S or PCM data
40	MCLK	Digital Input	CODEC Master clock input
41	VDDDB	Supply	Digital IO Supply
42	VSSD	Ground	Digital IO ground

43	VDDC	Supply	Digital core supply
44	JKDET	Analog Input	Jack detect input
45	HSMIC-	Analog Input	Headset Microphone negative Analog input
46	MIC2+/AUX_R /DMCLK2	Analog Input / Digital Output	PGA MIC2+ or AUXR Analog Input or Digital Microphone 2 Clock Output
47	MIC2-/DMDATA2	Analog Input / Digital Input	PGA MIC2- Analog Input or Digital Microphone 2 Data Input
48	MONO-/HSMIC+	Analog Input	PGA Mono-, or Headset Microphone positive Analog Input

Note: Analog I/O supply by VDDA, and Digital I/O supply is VDDDB. Pins 2,3, 46,47 are connected to VDDA

Pin Description-56 Balls WLCSP

Pin #	Name	Type	Functionality
A1	GPIO4/SDO	Digital I/O	General Purpose IO / 3 Wire Data Output
A2	DACIN	Digital Input	Serial Audio data input for I2S or PCM data
A3	VDDDB	Supply	Digital IO Supply
A4	VSSD	Ground	Digital IO ground
A5	HSMIC-	Analog Input	Headset Microphone negative Analog input
A6	MIC2+/DMCLK2	Analog Input / Digital Output	PGA MIC2+ Analog Input or Digital Microphone 2 Clock Output
A7	MIC2-/DMDATA2	Analog Input / Digital Input	PGA MIC2- Analog Input or Digital Microphone 2 Data Input
B1	SCLK	Digital Input	Serial Data Clock for I2C or SPI
B2	ADCOUT	Digital Output	Serial Audio data Output for I2S or PCM data
B3	MCLK	Digital Input	CODEC Master clock input
B4	VDDC	Supply	Digital core supply
B5	JKDET	Analog Input	General purpose IO or Jack detect input
B6	AUX_R/HSMIC+	Analog Input	Right channel Auxiliary Analog Input or Headset Microphone positive Analog Input
B7	AUX_L/MONO +	Analog Input	PGA Mono or Left channel Auxiliary Analog Input
C1	SDIO	Digital I/O	Serial Data for I2C or SPI
C2	FS	Digital I/O	Frame Sync input or output for I2S or PCM data
C3	BCLK	Digital I/O	Serial data bit clock input or output for I2S or PCM data
C4	IFSEL	Digital I/O	Select Control Interface for 3 wire or 2 wire mode
C5	MONO-	Analog Input	PGA Mono
C6	MIC1+/DMCLK1	Analog Input / Digital Output	PGA MIC1+ Analog Input or Digital Microphone 1 Clock Output
C7	VSSA	Ground	Analog Supply Ground
D1	GPIO1/CSB	Digital I/O	General Purpose IO (I2C) or Chip Select Bar (SPI)
D2	IRQ	Digital Output	Programmable Interrupt Output
D5	MIC1-/DMDATA1	Analog Input / Digital Input	PGA MIC1- Analog Input or Digital Microphone 1 Data Input
D6	MICBIAS	Analog Output	Microphone Bias Output
D7	VDDA	Supply	Analog Supply
E1	VDDSPK	Supply	Class-D amplifier supply
E2	SPKOUTR+	Analog Output	Class-D amplifier Right Channel positive Output
E3	TEST	N/C	Class-D amplifier Test point
E5	VREF	Analog I/O	Internal DAC & ADC voltage reference decoupling I/O
E6	VDDMIC	Supply	Microphone supply
E7	MICDET	Analog Input	Microphone button detection input
F1	VSSSPK	Ground	Class-D amplifier supply ground
F2	SPKOUTR-	Analog Output	Class-D amplifier Right Channel negative Output
F3	VDDSPK	Supply	Class-D amplifier supply
F4	HPL	Analog Output	Headphone left channel output
F6	VSSA	Ground	Analog Supply Ground
F7	VDDA	Supply	Analog Supply
G1	VDDSPK	Supply	Class-D amplifier supply
G2	SPKOUTL-	Analog Output	Class-D amplifier Left Channel negative Output
G3	VSSSPK	Ground	Class-D amplifier supply ground
G4	HPR	Analog Output	Headphone right channel output

G5	CPCA	Analog I/O	Charge Pump switching capacitor node A
G6	CPOUTP	Analog I/O	Charge Pump positive voltage
G7	VCCP1	Supply	Charge Pump Supply; same value as VDDA
H1	VSSSPK	Ground	Class-D amplifier supply ground
H2	SPKOUTL+	Analog Output	Class-D amplifier Left Channel positive Output
H3	VDDSPK	Supply	Class-D amplifier supply
H4	HPCOM	Analog Input	Headphone ground reference
H5	CPOUTN	Analog I/O	Charge Pump negative voltage
H6	CPCB	Analog I/O	Charge Pump switching capacitor node B
H7	VSSCP	Ground	Charge Pump Supply ground

Note: Analog I/O supply by VDDA, and Digital I/O supply is VDDDB. Pins A6,A7, C6, D5 are connected to VDDA

Electrical Characteristics

Conditions: Shutdown Mode $V_{DDA} = V_{ddb} = V_{DDC} = 1.8V$; $V_{DDSPK} = V_{DDMIC} = 4.2V$.

$R_L(\text{Loudspeaker}) = 8\Omega + 68\mu H$, $R_L(\text{Headphone}) = 32\Omega$, $f = 1\text{kHz}$, $MCLK = 12.288\text{MHz}$, unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$

Symbol	Parameter	Conditions	Typical	Limit	Units (Limit)
ISD	Shutdown Current	V_{DDA}	0.2	1	μA
		V_{DDA} when $V_{DDC} = 1.2V$	18.2		
		V_{ddb}	0.2	1	
		V_{DDC}	2	10	
		V_{DDSPK}	0.2	1	
		V_{DDMIC}	0.2	1	
I_{DD}	Standby Mode	MCLK off, Jack Insertion IRQ enabled	5		μA
DAC Speaker Amplifier Output					
P_O	Output Power	DAC Input, $V_{DDSPK} = 4.2V$, $f = 1\text{kHz}$, 20kHz BW $R_L = 4\Omega$, THD+N = 1%	1.6		W
		$R_L = 8\Omega$, THD+N = 1%	.97		W
		$V_{DDSPK} = 5.0V$, $f = 1\text{kHz}$, 20kHz BW $R_L = 8\Omega$, THD+N = 1%	1.38		W
THD+N	Total Harmonic Distortion + Noise	$R_L = 8\Omega$, $f = 1\text{kHz}$, $P_O = 300\text{mW}$	0.013		%
SNR	Signal to Noise Ratio	$P_O = 1W$, $V_{DDSPK} = 4.2V$, DAC Input, $f = 1\text{kHz}$, A-Weighted	100		dB
PSRR	Power Supply Rejection Ratio	$f_{RIPPLE} = 217\text{Hz}$, $V_{RIPPLE} = 200\text{mV}_{PP}$ Input Referred, SPK_GAIN = 0dB DAC Input, DAC_Gain = 0dB, Ripple Applied to $V_{DDSPK} = 4.2V$	80		dB
η	Efficiency	$V_{DDSPK} = 4.2V$, at 1% THD, $R_L = 8\Omega$	86		%
X_{TALK}	Channel Crosstalk	Left Channel to Right Channel, $P_O = 500\text{mW}$, $f = 1\text{kHz}$	-100		dB
DAC Headphone Amplifier Output					
P_O	Output Power	Stereo $R_L = 32\Omega$, DAC Input, $CPV_{DD} = 1.8V$, $f = 1\text{kHz}$, 20kHz BW, THD+N = 1%	27		mW
P_c	Power consumption	MP3 Playback in Quiescent, $V_{DDC} = 1.2V$, $R_L = 32\text{ohm}$, $f_s = 44.1\text{KHz}$	6		mW
		MP3 Playback with 1mW/Channel, 1KHz Stereo Output, $V_{DDC} = 1.2V$, $R_L = 32\text{ohm}$, $f_s = 44.1\text{KHz}$	14.5		mW
THD+N	Total Harmonic Distortion + Noise	$R_L = 32\Omega$, $f = 1\text{kHz}$, $P_O = 20\text{mW}$	-77		dB
SNR	Signal to Noise Ratio	$V_{OUT} = 1V_{RMS}$, DAC Input, DAC_Gain = 0dB, HP_Gain = 0dB, Digital Zero Input, $f = 1\text{kHz}$, A-Weighted	103		dB
PSRR	Power Supply Rejection Ratio	$f_{RIPPLE} = 217\text{Hz}$, $V_{RIPPLE} = 200\text{mV}_{P-P}$ Input Referred, HP_GAIN = 0dB DAC Input, DAC_Gain = 0dB Ripple Applied to V_{DDA}	80		dB
V_{OS}	Output Offset Voltage	HP_Gain = 0dB, DAC_Gain = 0dB, DAC Input	± 0.25	± 1	mV
X_{TALK}	Channel Crosstalk	Left Channel to Right Channel, $P_O = 3\text{mW}$, $f = 1\text{kHz}$	-75		dB
	Loading Capacitance	External capacitance at HPL and HPR		<500	pF

Symbol	Parameter	Conditions	Typical	Limit	Units (Limit)
ADC					
THD+N	ADC Total Harmonic Distortion + Noise	MIC Input, MIC_GAIN = -3dB, VIN = 1Vrms, f = 1kHz, Fs = 48kHz	-85		dB
SNR	Signal to Noise Ratio	Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 0dB, fs = 8kHz, Mono Differential Input	99		dB
		Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 6dB, fs = 8kHz, Mono Differential Input	98		
		Reference = VOUT(0dBFS), A-Weighted, Stereo Input, Gain = 0dB, fs = 48kHz	100		dB
PSRR	Power Supply Rejection Ratio	V _{RIIPPLE} = 200mV _{PP} applied to V _{DDA} , f _{RIIPPLE} = 217Hz, Input Referred, MIC_GAIN = 0dB Differential Input	65		dB
FS _{ADC}	ADC Full Scale Input Level	V _{DDA} = 1.8V	1*		V _{RMS}

*Note: ADC path needs to add 2dB gain to achieve FS_{ADC}.

Digital I/O

Parameter	Symbol	Comments/Conditions	Min	Max	Units
Input LOW level	V _{IL}	V _{DDB} = 1.8V		0.33*V _{DDB}	V
		V _{DDB} = 3.3V		0.37*V _{DDB}	
Input HIGH level	V _{IH}	V _{DDB} = 1.8V	0.67*V _{DDB}		V
		V _{DDB} = 3.3V	0.63*V _{DDB}		
Output HIGH level	V _{OH}	I _{Load} = 1mA, V _{DDB} = 1.8V	0.9*V _{DDB}		V
		I _{Load} = 1mA, V _{DDB} = 3.3V	0.95*V _{DDB}		
Output LOW level	V _{OL}	I _{Load} = 1mA, V _{DDB} = 1.8V		0.1*V _{DDB}	V
		I _{Load} = 1mA, V _{DDB} = 3.3V		0.05*V _{DDB}	

Recommended Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Digital Supply Range	V _{DDC}	1.1	1.2	1.98	V
Digital Supply Range for FLL operation and for Fs > 48KHz	V _{DDC}	1.61	1.8	1.98	V
Digital I/O Supply Range	V _{ddb}	1.6	1.8	3.6	V
Analog Supply Range	V _{DDA}	1.6	1.8	2.0	V
Headphone Supply Range	V _{DDA}	1.6	1.8	2.0	V
Loudspeaker Supply Range	V _{DDSPK}	2.5	4.2	5.0	V
Microphone Bias Supply Voltage	V _{DDMIC}	2.5	4.2	5.0	V
Temperature Range	T _A	-40		+85	°C

CAUTION: The following conditions needed to be followed for regular operation: V_{DDMIC} > V_{DDA} -1.2V; V_{ddb} > V_{DDC} - 0.6V.

Absolute Maximum Ratings

Parameter	Min	Max	Units
Digital Supply Range	-0.3	2.2	V
Digital I/O Supply Range	-0.3	6.0	V
Analog Supply Range	-0.3	2.2	V
Headphone Supply Range	-0.3	2.2	V
Loudspeaker Supply Range	-0.3	6.0	V
Microphone Bias Supply Voltage	-0.3	6.0	V
Voltage Input Digital Range	DGND - 0.3	V _{DD} + 0.3	V
Voltage Input Analog Range	AGND - 0.3	V _{DD} + 0.3	V
Junction Temperature, T _J	-40	+150	°C
Storage Temperature	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

CAUTION: The following conditions need to be followed for maximum ratings: V_{DDMIC} > V_{DDA} -1.2V; V_{ddb} > V_{DDC} - 0.6V.

1 General Description

NAU88L24 is Nuvoton's generation of ultra-low power CODECs that have both analog and digital blocks operating at 1.8V and a digital core that is able to operate at 1.2V. This CODEC includes new DSP functions including DRC (Dynamic Range Compression), equalizer, notch filters, and high pass filters. The Loudspeaker and MIC bias supplies have also been upgraded to support higher voltages up to 5V.

1.1 Inputs

The NAU88L24 provides multiple analog inputs to acquire and process audio signals from microphones or other sources with high fidelity and flexibility. There is a left and right input path with four input pins each that can be used to capture signals from single-ended and differential sources. Each channel has a fully differential programmable gain amplifier (PGA), which can be configured to mix any combination of the four inputs. The outputs of the PGAs connect to the ADCs.

There are also four alternative digital microphone inputs that use the two stereo inputs MIC1+/- and MIC2+/- as DMCLK1/2 and DMDATA1/2, respectively. DMCLK outputs select between the stereo microphones depending on the phase of the clock that has a maximum frequency of 3.25MHz.

1.2 Outputs

NAU88L24 has two pairs of outputs: stereo Class D speaker outputs and ground-referenced Class G headphone outputs that are fed by two DACs. The stereo class D amplifier has a gain range from 0dB to 24dB, and the headphone amplifier has a gain range of -30dB to 6dB.

The Class D speaker amplifier is powered by a separate power supply VDDSPK, which can go up to 5V. This amplifier is capable of delivering up to 2.9W into a 4Ω load with a 5V supply.

The Class G headphone amplifier is powered by the charge pump output voltages CPOUTP and CPOUTN. When there is no loading the CPOUTP is equal to VDDA, and CPOUTN is equal to -VDDA.

1.3 ADC, DAC and Digital Signal Processing

The NAU88L24 has two independent high quality ADCs and DACs. These are high performance 24-bit sigma-delta converters, which are suitable for a very wide range of applications.

The ADCs and DACs have functions that individually support analog mixing and routing. The ADC and DAC blocks also support advanced digital signal processing subsystems that enable a very wide range of programmable signal conditioning and signal optimizing functions. All digital processing is done with 24-bit precision to minimize processing artifacts and maximize the audio dynamic range supported by the NAU88L24.

The ADCs and DACs can be enabled to support dynamic range compressors (DRC), high pass filters, and notch filters that are highly versatile. The DRC can be programmed to limit the maximum output level and/or boost a low output level. The high pass filters are intended for DC-blocking or low frequency noise reduction, such as reducing unwanted ambient noise or "wind noise" on a microphone input. The notch filter can also be programmed to greatly reduce a specific frequency band or frequency.

The digital signal processing subsystem also provides a 5-Band Equalizer that can be applied to either the ADC audio path or the DAC audio path, but not both simultaneously.

1.4 Digital Interfaces

Command and control of the device is accomplished by using a 2-wire serial control interface. This simple, but highly flexible interface is compatible with most commonly used command and control serial data protocols and host drivers.

The digital audio I/O data streams transfer separately from command and control using either I2S or PCM audio data protocols. When in PCM mode, the NAU88L24 can support time-division multiplexing (TDM) allowing for up to 4 concurrent PCM input and output channels.

These simple but highly flexible interface protocols are compatible with most commonly used serial data protocols, host drivers, and industry standard I2S and PCM devices.

2 Power Supply

This NAU88L24 has been designed to operate reliably using a wide range of power supply conditions and power-on/power-off sequences. However, because of existence of ESD protection diodes between the supplies, that will have impact on the application of the supplies. Because of these diodes, the following conditions need to be met:

VDDMIC > VDDA-1.2V and VDDDB > VDDC – 0.6V.

Application Notes:

- To reduce leakage, [GPIO_SEL_REG0X1A \[6\]](#) needs to set to 1'b.

2.1 Power on and off reset

The NAU88L24 includes a power on and off reset circuit on chip that resets the internal logic to its default state when the VDDA and VDDC supplies power up. This reset function will be automatically and internally generated when the power supplies are too low for reliable operation of the internal logic circuitry. VDDA and VDDC must drop below approximately 1.0Vdc and 0.55Vdc, respectively. Note that this is much lower than the required voltage for normal operation and the values here are mentioned only as general insight into the system design.

When VDDA and VDDC drop below their threshold values, the reset is held on until the power supplies return to a minimum voltage specified in the parameter table. Once these voltages are reached, the reset is held on for a minimum of 6 μ s and then it is released. At this point, the registers can be written to through the control interface. Note that it is recommended to write to register 0x00 twice upon power up. This will reset all registers to their default state.

An additional internal RC filter based circuit has been added to help the circuit respond to faster ramp rates ($\sim 10\mu$ s) and generate the desired reset period width ($\geq 6\mu$ s). This filter is also used to eliminate any supply glitches (typically 50ns) that could cause a false reset condition.

Application Notes:

- VDDA ramp up time for a guaranteed power on reset needs to be less than 50msec. The VDDA ramp down time for a guaranteed power off reset needs to be less than 125msec. If the ramp down rate is too slow (no pull down), then we can enable the minimum VREF impedance by [BIAS_ADJ.VMIDSEL_REG0X66\[5:4\]=11](#) with [BIAS_ADJ.VMIDEN_REG0X66\[6\]=1](#), before shutdown in order to discharge VDDA quickly.

3 Input Path Detailed Descriptions

The NAU88L24 provides multiple inputs to acquire and process audio signals from microphones or other sources with high fidelity and flexibility. There is a left and right input path with four input pins each, which can be used to capture signals from single-ended and differential sources. Each channel has a fully differential programmable gain amplifier (PGA), which can be configured to mix any combination of the four inputs. The outputs of the PGAs are then fed into the ADCs.

All inputs are maintained at a DC bias of approximately $\frac{1}{2}$ of the VDDA supply voltage. Connections to these inputs should be AC-coupled by means of DC blocking capacitors suitable for the device application.

The NAU88L24 features two low-noise and differential microphone input pairs that are connected to a PGA gain stage. This differential input structure is essential in noisy digital systems where amplification of low-amplitude analog signals is necessary such as in portable digital media devices and cell phones.

Differential inputs are very useful to reduce ground noise in systems in which there are ground voltage differs between different chips and other components. When properly implemented, the differential input architecture offers an improved power-supply rejection ratio (PSRR) and higher ground noise immunity.

3.1 Analog Microphone Inputs

The NAU88L24 Analog microphone inputs can be setup in five different configurations:

- Two differential analog microphones: MIC1+/MIC1- and MIC2+/MIC2-.
- One pair of stereo analog microphones: MIC1 $\pm$ and MIC2 $\pm$.
- Four single ended analog microphones: MIC1+, MIC1-, MIC2+, and MIC2-.
- One differential head set microphone (HSMIC+/HSMIC-), one MONO input or single-ended AUX_L, plus two differential analog microphones.
- Two single-ended head set microphones: HSMIC+ and HSMIC-.

The analog microphone inputs are followed by different attenuation stages before they are routed to the variable PGA (Programmable Gain Amplifier) stage. The analog microphone inputs MIC1 $\pm$ and MIC2 $\pm$ are routed through a 0dB or -6dB attenuation stage dependent on [PGA_GAIN.M6DBL_REG0X67\[8\]](#) and [PGA_GAIN.M6DBR_REG0X67\[0\]](#), respectively. The rest of the inputs are routed through a variable attenuation stage with a range from -46.5dB to 0dB dependent on [FEPGA_ATTENUATION.FEPGA_ATTNR_REG0X7A\[12:8\]](#) and [FEPGA_ATTNL.FEPGA_ATTNL_REG0X7A\[4:0\]](#). By default, both types of inputs are attenuated by 0dB.

After the attenuation stage, the inputs are routed through switches that can be set depending on application requirements. Once the signal is through the switches, all input configurations are routed through an input mixer and then to a programmable gain amplifier (PGA) that ranges from 0dB to 36dB in 2dB steps. This amplifier can be set using **FEPGA_II.FEPGA_GAINR REG0X78[9:5]** and **FEPGA_II.FEPGA_GAINL REG0X78[4:0]**.

Application Notes:

- Each input has an input impedance of about 12kΩ.
- If the application has single ended MIC inputs, then the inputs can be tied off to VREF as single ended inputs. **FEPGA_SE.FEPGASEL REG0X79[3:0]** and **FEPGA_SE.FEPGASER REG0X79[11:8]** are to set left and right channel, respectively.
- When using single ended inputs, they should be AC coupled to ground to have better common-mode noise rejection.
- If the application has large decoupling capacitors on the inputs, there is an option to pre-charge the capacitors to minimized pops and clicks during startup. Please see register **FEPGA_II.ADC_CTRL REG0X78[15:10]** for more details.
- Both MIC and Line inputs can be used simultaneously.

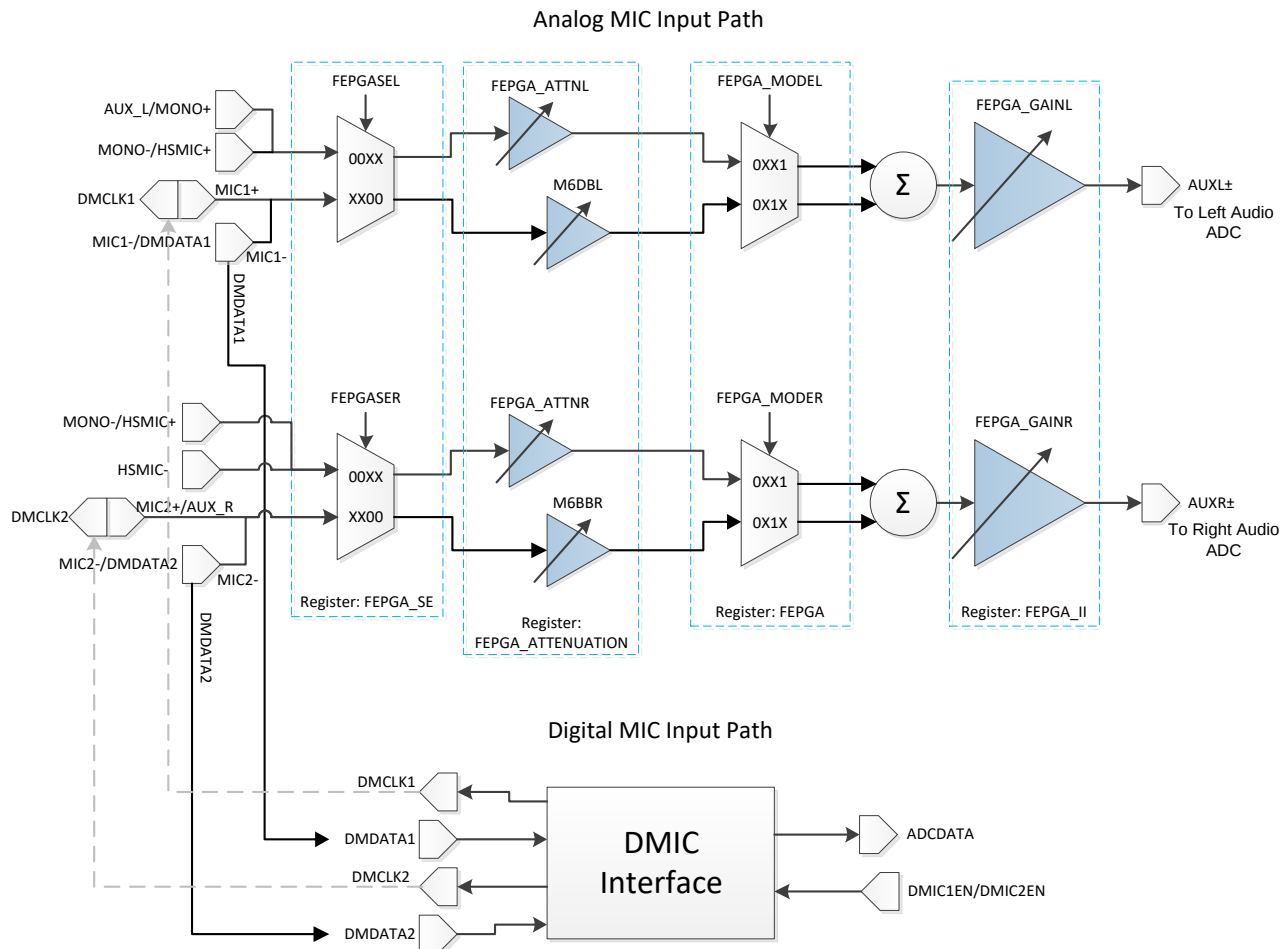


Figure 1: Microphone Input Block Diagram with Registers

3.1.1 VREF

The NAU88L24 includes a mid-supply, reference circuit that produces voltage close to $VDDA/2$ that is decoupled to VSS through the $VREF$ pin by means of an external bypass capacitor. Because $VREF$ is used as

a reference voltage for the majority of the NAU88L24, a large capacitance is required to achieve good power supply rejection at low frequency, typically 4.7 μ F is used.

VREF voltage can be enabled by setting [BIAS_ADJ.VMIDEN REG0X66\[6\]](#) and the output impedance can be set using [BIAS_ADJ.VMIDSEL REG0X66\[5:4\]](#).

Application Notes:

- Larger capacitances can be used but it will increase the rise time of VREF and delay the line output signal. However, a pre-charge circuit has been included to help reduce the rise time.
- Due to the high impedance of the VREF pin, it is important to use a low leakage capacitor.
- A pre-charge circuit has been implemented to reduce the VREF rise time. Once charged, this can be disabled using [BOOST.PVDMFST REG0X76\[13\]](#) to save power or prevent rapid changes in level due to fluctuations in VDDA.

VMIDSEL	VREF Resistor Selection	VREF Impedance
00	Open, no resistor selected	Open, no impedance installed
01	50kOhm	25kOhm
10	250kOhm	125kOhm
11	5kOhm	2.5kOhm

Table 1: VREF Impedance Selection

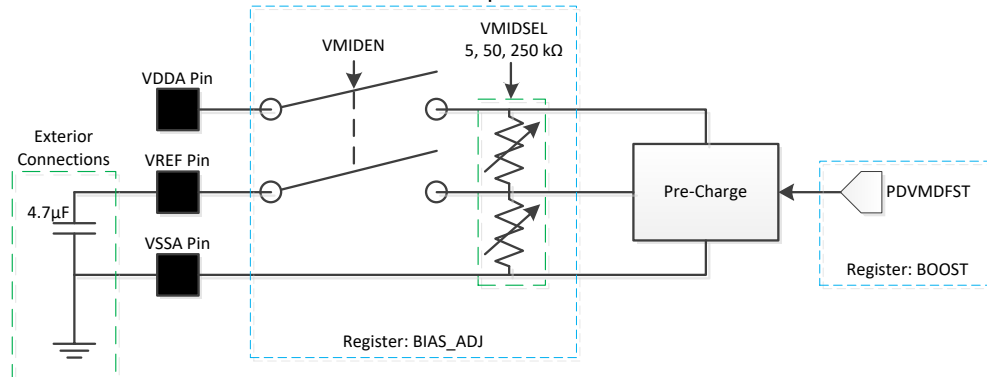


Figure 2: VREF Circuitry

3.1.2 MIC Bias

The NAU88L24 provides one MIC bias pin, which can be used to power electret and digital microphones. This pin can be enabled by using [MIC_BIAS.POWERUP REG0X74\[8\]](#) and the level can be set by using [MIC_BIAS.MICBIASLVL1 REG0X74\[2:0\]](#).

Application Notes:

- It is recommended that the microphones do not draw more than 4mA from the MICBIAS pin
- Low noise or low power mode can be enabled by setting [MIC_BIAS.LOWNOISE REG0X74\[10\]](#) to 1 or 0, respectively.
- There is an internal tie-off option that can save the need to install an external resistor for connecting the microphones. This can be enabled using [MIC_BIAS.INT2KB REG0X74\[14\]](#).
- If MICBIAS is used to power digital microphones, [MIC_BIAS.MICBIASLVL1 REG0X74\[2:0\]](#) set to 000 (VDDA) and the capacitor can be 100nF or 200nF. But then MICBIAS can only be used in low power mode. If MICBIAS is used to power analog microphones, it is possible to omit the capacitor, but then the [MIC_BIAS.NOCAP REG0X74\[6\]](#) bit has to be set high to ensure stability. If a capacitor is used, [MIC_BIAS.NOCAP REG0X74\[6\]](#) has to be low to ensure stability. In this case a capacitor value of 1 μ F to 4.7 μ F can be used.

3.2 Digital MIC Inputs

In addition to analog inputs, the NAU88L24 is setup to handle up to four digital MIC inputs using the DMCLK1/2 and DMDATA1/2 pins that are multiplexed with the MIC1/2+ and MIC1/2- pins, respectively. Both DMDATA inputs are able to handle two digital microphones by selecting them alternately for each half of the clock cycle.

Application Notes:

- The clock phase for the selection of the digital MIC is configurable using [ENA_CTRL.DMIC_LCH_EDGE_ADC_CH01 REG0X01\[14\]](#) and [ENA_CTRL.DMIC_LCH_EDGE_ADC_CH23 REG0X01\[15\]](#).
- The DMCLK rate can be selected using [CLK_DIVIDER.CLK_DMIC_SRC REG0X03\[12:10\]](#).
- Both digital MIC inputs can be used simultaneously. However, both digital MIC and analog MIC inputs cannot.

3.3 Line Inputs

In addition to the MIC inputs, the right and left ADC channels can be setup to accept line inputs in the following configurations:

- One pair of single ended stereo AUX inputs: AUX_L/AUX_R
- Two single ended MONO inputs: MONO+ and MONO-
- One differential MONO input: MONO±

The single ended operation and pre-charge option described in the analog MIC input section are also available for line inputs because they follow similar data paths to the MIC inputs. Exclusively AUX_R, the line inputs are routed through a variable attenuation stage with a range from -46.5dB to 0dB dependent on [FEPGA_ATTENUATION.FEPGA_ATTNR REG0X7A\[12:8\]](#) and [FEPGA_ATTENUATION.FEPGA_ATTNL REG0X7A\[4:0\]](#). By default, both channels are attenuated by 0dB.

Application Notes:

- Both Line and analog MIC inputs can be used simultaneously
- AUX shared with analog MIC inputs, its attenuation is -6dB or 0dB.

3.4 Programmable Gain Amplifier (PGA)

Each input channel (Left and Right) has a dedicated fully differential PGA amplifier used for signal conditioning before it is fed into the ADC. Both PGAs can be individually enabled or disabled using [POWER_UP_CONTROL.PUPR REG0X7F\[13\]](#) and [POWER_UP_CONTROL.PUPL REG0X7F\[12\]](#) and are controlled using [FEPGA.FEPGA_MODER REG0X77\[7:4\]](#) and [FEPGA.FEPGA_MODEL REG0X77\[3:0\]](#).

Application Notes:

- The PGA can accept either differential or single ended input configurations.
- The gain for the Right and Left PGA can be set using [FEPGA_II.FEPGA_GAINR REG0X78\[9:5\]](#) and [FEPGA_II.FEPGA_GAINL REG0X78\[4:0\]](#), respectively.
- The PGA can be set into a Low or High power mode using [BIAS_ADJ.BIASADJ REG0X66\[1:0\]](#).
- Both MIC and Line inputs can be connected to the PGA simultaneously.

4 ADC Digital Block

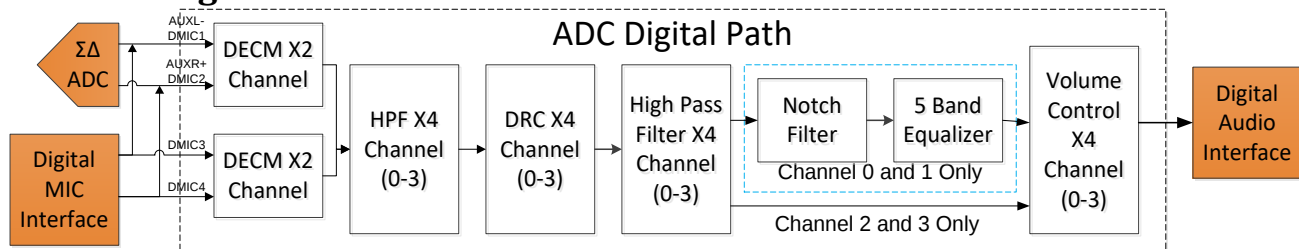


Figure 3: ADC Digital Path

The ADC digital block takes the output of the 24-bit Analog-to-Digital converter and preforms signal processing aimed at producing a high quality audio sample stream to the audio path digital interface. The figure above shows the various steps associated with the ADC digital path. This block can be enabled for channels 0 through 3 by using [ENA_CTRL.ADC_CH\(3/2/1/0\)_EN REG0X01\[3:0\]](#).

Oversampling is used to improve noise and distortion performance; however this does not affect the final audio sample rate. [ADC_FILTER_CTRL.ADC_RATE REG0X24\[1:0\]](#) can be used to set the ADC OSR and [ADC_FILTER_CTRL.SMPL_RATE REG0X24\[7:5\]](#) should be set to the value closest to the actual sample rate.

The polarity of either ADC output signal can be changed independently on either ADC logic output as a feature sometimes useful in management of the audio phase. This feature can help minimize any audio processing that may be otherwise required as the data is passed to other stages in the system.

Application Notes:

- The definitions for channel 0 through 3 can be seen below in the table below. Also note that for channel 0/1, each channel can only be used in either Analog mode or Digital mode, not both at the same time.
- The ADC coding scheme is in twos complement format.
- The full-scale input level is proportional to VDDA. For example, with a 1.8V supply voltage, the full-scale level is 1.0V_{RMS}.
- Four PDM microphones can be enabled using [ENA_CTRL.ADC_CH\(3/2/1/0\)_DMIC_MODE REG0X01\[9:6\]](#) for ADC channel 3 through 0, respectively.
- The polarity of the four digital microphones can be set using [ENA_CTRL.DMIC_LCH_EDGE_ADC_CH\(23/01\) REG0X01\[15:14\]](#). This can help minimize any unnecessary audio processing as data is passed to other stages in the system.
- ADC path connects with DAC path by setting [PORT0_I2S_PCM_CTRL_1.ADDAP REG0X1C\[7\]=1](#)
- ADCL out and ADCR out has one sample time difference

CH	Analog Inputs	Digital Inputs
0	MIC1±/AUX_L/MONO+	Digital MIC 0 (DMCLK1/DMDATA1)
1	MIC2±/AUX_R/MONO-/HSMIC±	Digital MIC 1 (DMCLK1/DMDATA1)
2		Digital MIC 2 (DMCLK2/DMDATA2)
3		Digital MIC 3 (DMCLK2/DMDATA2)

Table 2: ADC Channel Input Definitions

4.1 ADC Dynamic Range Compressor (DRC)

The NAU88L24 includes DRCs for the four channels in the ADC. However, to control the DRC, the four channels have been paired and denoted as CH01 or CH23 in the register map for channel 0/1 and channel 2/3, respectively. Similarly, the DAC left and right audio channel controls have been paired.

The DRC function consists of level estimation and static curve control.

4.1.1 Level Estimation

The NAU88L24 uses Peak level estimation that depends on the attack and decay time setting. The attack times settings are grouped to channel 0/1 and 2/3 and can be set by using

[DRC_ATKDCY_ADC_CH01.DRC_PK_COEF1_ADC_CH01 REG0X3B\[15:12\]](#) and [DRC_ATKDCY_ADC_CH23.DRC_PK_COEF1_ADC_CH23 REG0X3F\[15:12\]](#), respectively. The decay times are similarly set using [DRC_ATKDCY_ADC_CH01.DRC_PK_COEF2_ADC_CH01 REG0X3B\[11:8\]](#) and [DRC_ATKDCY_ADC_CH23.DRC_PK_COEF2_ADC_CH23 REG0X3F\[11:8\]](#), respectively.

Bits	DRC_PK_COEF1_ADC_CH##	DRC_PK_COEF2_ADC_CH##
0000	Ts	63*Ts
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4095*Ts
0111	255*Ts	8191*Ts

Table 3: ADC Level Estimation Attack and Decay Time Register Settings

Application Notes:

- Time constant Ts shown in the register map is the sampling time given by 1/(Sampling Frequency)

4.1.2 Static Curve

The DRC static curve supports five programmable sections and can be enabled by using

[DRC_KNEE_IP12_ADC_CH01.DRC_ENA_ADC_CH01 REG0X38\[15\]](#) and [DRC_KNEE_IP12_ADC_CH23.DRC_ENA_ADC_CH23 REG0X3C\[15\]](#) for channel 0/1 and 2/3, respectively. The figure below shows the five programmable sections.

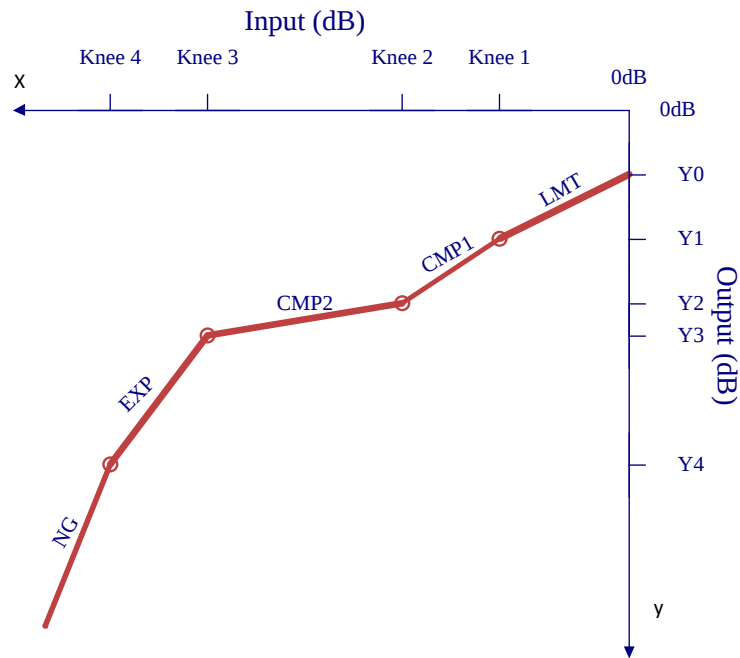


Figure 4: DRC Static Characteristics

Each of the sections labeled NG, EXP, CMP2, CMP1, and LMT are controlled by setting the slope and knee point values in the registers. The table below provides the corresponding registers and their locations.

Static Curve Section	CH	Slope	Knee Point
LMT	0/1	<u>DRC SLOPE ADC CH01.DRC LMT SLP</u> <u>ADC CH01 REG0X3A[2:0]</u>	
	2/3	<u>DRC SLOPE ADC CH23.DRC LMT SLP</u> <u>ADC CH23 REG0X3E[2:0]</u>	
CMP1	0/1	<u>DRC SLOPE ADC CH01.DRC CMP1 SLP</u> <u>ADC CH01 REG0X3A[5:3]</u>	<u>DRC KNEE IP12 ADC CH01.DRC KNEE1</u> <u>IP ADC CH01 REG0X38[4:0]</u>
	2/3	<u>DRC SLOPE ADC CH23.DRC CMP1 SLP</u> <u>ADC CH23 REG0X3E[5:3]</u>	<u>DRC KNEE IP12 ADC CH23.DRC KNEE1</u> <u>IP ADC CH23 REG0X3C[4:0]</u>
CMP2	0/1	<u>DRC SLOPE ADC CH01.DRC CMP2 SLP</u> <u>ADC CH01 REG0X3A[8:6]</u>	<u>DRC KNEE IP12 ADC CH01.DRC KNEE2</u> <u>IP ADC CH01 REG0X38[13:8]</u>
	2/3	<u>DRC SLOPE ADC CH23.DRC CMP2 SLP</u> <u>ADC CH23 REG0X3E[8:6]</u>	<u>DRC KNEE IP12 ADC CH23.DRC KNEE2</u> <u>IP ADC CH23 REG0X3C[13:8]</u>
EXP	0/1	<u>DRC SLOPE ADC CH01.DRC EXP SLP</u> <u>ADC01 REG0X3A[10:9]</u>	<u>DRC KNEE IP34 ADC CH01.DRC KNEE3</u> <u>IP ADC CH01 REG0X39[5:0]</u>
	2/3	<u>DRC SLOPE ADC CH23.DRC EXP SLP</u> <u>ADC23 REG0X3E[10:9]</u>	<u>DRC KNEE IP34 ADC CH23.DRC KNEE3</u> <u>IP ADC CH23 REG0X3D[5:0]</u>
NG	0/1	<u>DRC SLOPE ADC CH01.DRC NG SLP A</u> <u>DC01 REG0X3A[13:12]</u>	<u>DRC KNEE IP34 ADC CH01.DRC KNEE4</u> <u>IP ADC CH01 REG0X39[13:8]</u>
	2/3	<u>DRC SLOPE ADC CH23.DRC NG SLP A</u> <u>DC23 REG0X3E[13:12]</u>	<u>DRC KNEE IP34 ADC CH23.DRC KNEE4</u> <u>IP ADC CH23 REG0X3D[13:8]</u>

Table 4: ADC DRC Static Curve control registers

The output Y values can be determined based on the slopes and knee points selected. Y1 is always equal to Knee 1, as an initial and default condition.

$$Y1 = \text{Knee 1}$$

$$Y0 = Y1 - (\text{Knee 1}) * (\text{LMT Slope})$$

$$Y2 = (\text{Knee 2} - \text{Knee 1}) * (\text{CMP1 Slope}) + Y1$$

$$Y3 = (\text{Knee 3} - \text{Knee 2}) * (\text{CMP2 Slope}) + Y2$$

$$Y4 = (\text{Knee 4} - \text{Knee 3}) * (\text{EXP Slope}) + Y3$$

Application Notes:

- The Y axis distance adjusting along curve cannot exceed 36dB.
- Smooth Knee filter function can be enabled by using [DRC KNEE IP12 ADC CH01.DRC SMTH ENA ADC CH01 REG0X38\[7\]](#) and [DRC KNEE IP12 ADC CH23.DRC SMTH ENA ADC CH23 REG0X3C\[7\]](#) for channel 0/1 and 2/3, respectively.
- The gain values can also be individually read in decimal by using [DRC GAINL ADC0 REG0X40](#), [DRC GAINL ADC1 REG0X41](#), [DRC GAINL ADC2 REG0X42](#), and [DRC GAINL ADC3 REG0X43](#) for channel 0 through 3, respectively. [15:10] represents integer, and [9:0] represents fraction.
- The attack time can be set using [DRC ATKDCY ADC CH01.DRC ATK ADC CH01 REG0X3B\[7:4\]](#) and [DRC ATKDCY ADC CH23.DRC ATK ADC CH23 REG0X3F\[7:4\]](#) for channel 0/1 and 2/3, respectively.
- The decay time can be set using [DRC ATKDCY ADC CH01.DRC DCY ADC CH01 REG0X3B\[3:0\]](#) and [DRC ATKDCY ADC CH23.DRC DCY ADC CH23 REG0X3F\[3:0\]](#) for channel 0/1 and 2/3, respectively.

Bits	DRC ATK ADC CH##	DRC DCY ADC CH##
0000	Ts	63*Ts
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4905*Ts
0111	255*Ts	8191*Ts
1000	511*Ts	16383*Ts
1001	1023*Ts	32757*Ts
1010	2047*Ts	65535*Ts
1011	4095*Ts	
1100	8191*Ts	

Table 5: ADC Attack and Decay Time Register Settings

4.2 ADC Digital Volume Control

The digital volume control feature allows you to adjust the effective audio volume coming from each ADC using a two-stage volume control. This allows the gain to be adjusted from -128dB to +50dB. Also included is a mute value that will reduce the ADC output to 0. To adjust the channel volume controls, use

[ADC CH0 DGAIN CTRL.DGAIN ADC CH0 REG0X2D\[8:0\]](#), [ADC CH1 DGAIN CTRL.DGAIN ADC CH0 REG0X2E\[8:0\]](#), [ADC CH2 DGAIN CTRL.DGAIN ADC CH0 REG0X2F\[8:0\]](#), and [ADC CH3 DGAIN CTRL.DGAIN ADC CH3 REG0X30\[8:0\]](#) for channel 0 through 3, respectively.

4.3 ADC Programmable High Pass Filter

Each input ADC has its own HPF that can function in a default Audio mode or an Application Specific mode. In Audio mode, the filter functions as a simple first order DC blocking filter with a cutoff frequency of 3.7Hz. In the Application specific mode, the filter functions as a second order audio filter with a programmable cutoff frequency. To enable the HPF, use [ADC HPF FILTER.HPFEN ADC CH01 REG0X23\[4\]](#) and [ADC HPF FILTER.HPFEN ADC CH23 REG0X23\[12\]](#) for channel 0/1 and 2/3, respectively.

Application Notes:

- To set the cutoff frequency for the application mode use [ADC HPF FILTER.HPFCUT ADC CH01 REG0X23\[2:0\]](#) for channel 0/1 and [ADC HPF FILTER.HPFCUT ADC CH23 REG0X23\[10:8\]](#) for channel 2/3.
- The cutoff frequency for the HPF is scaled depending on the sampling frequency. Use the table below to determine the appropriate cutoff frequency.
- To enable the application specific mode, use register [ADC HPF FILTER.HPFAM ADC CH01 REG0X23\[3\]](#) for the channel 0/1 ADC and [ADC HPF FILTER.HPFAM ADC CH23 REG0X23\[11\]](#) for the channel 2/3 ADC.

HPFCUT_ADC _CH##	ADC FILTER CTRL.SMPL RATE REG0X23[7:5]					
	8 kHz	12 kHz	16 kHz	24 kHz	32 kHz	48kHz
000	82	122	82	122	82	122
001	102	153	102	153	102	153
010	131	156	131	156	131	156
011	163	245	163	245	163	245
100	204	306	204	306	204	306
101	261	392	261	392	261	392
110	327	490	327	490	327	490
111	408	612	408	612	408	612

Table 6: High Pass Filter Cut-off Frequencies in Hz

4.4 Programmable Notch Filter

In addition to the HPF filter described in section 4.3, channel 0 and 1 have an optional notch filter available in the ADC digital block. To enable this function, use **NOTCH_FILTER 1.NFEN REG0X27[14]** and to set the notch characteristics, use **NOTCH_FILTER 1.NFA0 REG0X27[13:0]** and **NOTCH_FILTER 2.NFA1 REG0X28[13:0]** according the table below.

Application Notes:

- The filter operation and settings are the same for both ADCs.
- NOTCH_FILTER 2.NOTCH_DLY_DIS REG0X28[14]** is an optional delay function to stabilize the signal path and reduce “ping” noise.
- It is possible to update A0 and A1 filter coefficients simultaneously by enabling **NOTCH_FILTER 1.NFU1 REG0X27[15]** and **NOTCH_FILTER 2.NFU2 REG0X28[15]**. By setting these bits to 1, any values in the A0 and A1 register positions are used. However, by setting the update bits to 0, any values entered into A0 and A1 are stored until the update bits are activated.

A ₀	A ₁	Notation	Register Value (DEC)
$1 - \tan \frac{2\pi f_b}{2f_s}$	$-(1 + A_0) \times \cos \frac{2\pi f_c}{f_s}$	f_c = center frequency (Hz) f_b = -3dB bandwidth (Hz) f_s = sample frequency (Hz)	NFCA0 = $-A_0 \times 2^{13}$ NFCA1 = $-A_1 \times 2^{12}$ Note: Values are rounded to the nearest whole number and converted to 2's complement
$1 + \tan \frac{2\pi f_b}{2f_s}$			

Table 7: Notch Filter Coefficient Equations

4.5 ADC Path Digital Mixer

The NAU88L24 implements a channel based digital mixer for ADC output that can select between input channels and I2S channels to mix for the four ADC channel outputs. The figure below shows a block diagram of how the mixer works along with the related registers.

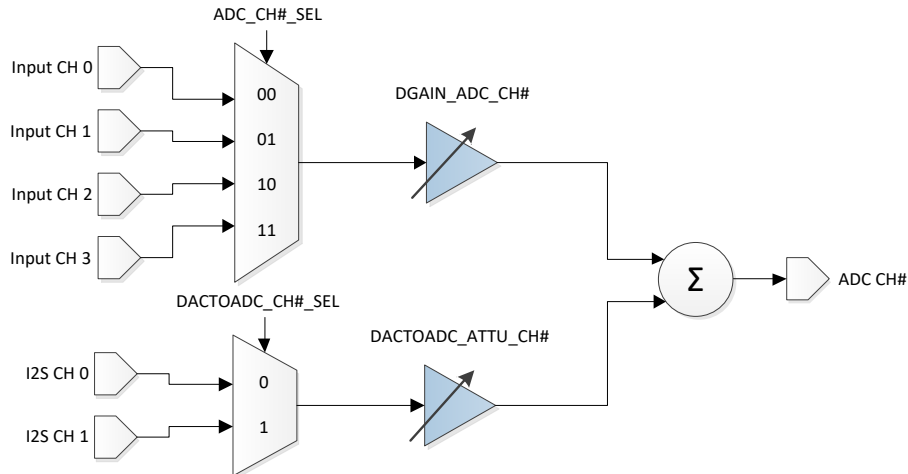


Figure 5: ADC Digital Mixer Block Diagram

Each of the register commands in the figure above can be found in [ADC_CH0_DGAIN_CTRL_REG0X2D](#) through [ADC_CH3_DGAIN_CTRL_REG0X30](#) for ADC channels 0 through 3, respectively.

CH	Register	Input Channel Select [10:9]	Input Channel Gain [8:0]	I2S Channel Select [11]	I2S Channel Gain [15:12]
0	ADC_CH0_DGAIN_CTRL_REG0X2D	ADC_CH0_SEL	DGAIN_ADC_CH0	DACTOADC_CH0_S	DACTOADC_ATTU_CH0
1	ADC_CH1_DGAIN_CTRL_REG0X2E	ADC_CH1_SEL	DGAIN_ADC_CH1	DACTOADC_CH1_S	DACTOADC_ATTU_CH1
2	ADC_CH2_DGAIN_CTRL_REG0X2F	ADC_CH2_SEL	DGAIN_ADC_CH2	DACTOADC_CH2_S	DACTOADC_ATTU_CH2
3	ADC_CH3_DGAIN_CTRL_REG0X30	ADC_CH3_SEL	DGAIN_ADC_CH3	DACTOADC_CH3_S	DACTOADC_ATTU_CH3

Table 8: ADC Digital Mixer Control Registers

Application Notes:

- [DACTOADC_ATTU_CH#](#) can be used to mute the I2S channel selected so it doesn't mix with the selected input channel.

4.6 5-Band Equalizer

The NAU88L24 includes a 5-band graphic equalizer with low distortion and noise, and wide dynamic range that applies to both channels simultaneously. This function can be enabled with [EQ1_LOW.EQON_REG0X29\[9\]](#).

The characteristics of the 5-band equalizer are determined by the cutoff/center frequency, bandwidth, and gain settings. The table below shows the associated registers for each band.

Band	Cutoff/Center Frequency Select	Bandwidth Select	Gain Select
1 (80Hz – 175Hz)	EQ1_LOW.EQ1C_REG0X29[6:5]	EQ1_LOW.EQ1BW_REG0X29[7]	EQ1_LOW.EQ1G_REG0X29[4:0]
2 (230Hz – 500Hz)	EQ2_EQ3.EQ2C_REG0X2A[6:5]	EQ2_EQ3.EQ2BW_REG0X2A[7]	EQ2_EQ3.EQ2G_REG0X2A[4:0]
3 (650Hz – 1.4kHz)	EQ2_EQ3.EQ3C_REG0X2A[14:13]	EQ2_EQ3.EQ3BW_REG0X2A[15]	EQ2_EQ3.EQ3G_REG0X2A[12:8]
4 (1.8kHz – 4.1kHz)	EQ4_EQ5.EQ4C_REG0X2B[6:5]	EQ4_EQ5.EQ4BW_REG0X2B[7]	EQ4_EQ5.EQ4G_REG0X2B[4:0]

5 (5.3kHz – 11.7kHz)	EQ4 EQ5.EQ5C REG0X2B[14:13]	EQ4 EQ5.EQ5BW REG0X2B[15]	EQ4 EQ5.EQ5G REG0X2B[12:8]
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Table 9: 5-Band Equalizer Setting Registers

Register Value	Equalizer Band Cutoff/Center frequency				
	EQ1C(High Pass)	EQ2C(Band Pass)	EQ3C (Band Pass)	EQ4C (Band Pass)	EQ5C (Low Pass)
00	80Hz	230Hz	650Hz	1.8kHz	5.3kHz
01	105Hz	300Hz	850Hz	2.4kHz	6.9kHz
10	135Hz	385Hz	1.1kHz	3.2kHz	9.0kHz
11	175Hz	500Hz	1.4kHz	4.1kHz	11.7kHz

Table 10: Equalizer Center/Cutoff Frequency Settings

Register Value	Gain
00000	+12db
00001	+11dB
Increments -1dB per step	
10111	-11dB
11000	-12dB

Table 11: Equalizer Gain Settings

Application Notes:

- This function can be setup to support either the ADC path or the DAC path but not both simultaneously. [EQ1 LOW.EQMODE REG0X29\[8\]](#) uses to select for ADC when it is 0, and uses for DAC when it is 1.
- Each band can adjust the gain by $\pm 12\text{dB}$

4.7 Companding

Companding is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates using non-linear algorithms. The NAU88L24 supports the two main telecommunications companding standards on both transmit and receive sides: A-law and μ -law. The A-law algorithm is primarily used in European communication systems and the μ -law algorithm is primarily used by North America, Japan, and Australia. For more information, see section 5.6 [COMPANDING](#).

4.8 Additional ADC Application Notes

- [CLK GATING ENA.CLK ADC PL REG0X02\[8\]](#) sets the ADC clock polarity.
- [CLK GATING ENA.CLK GAIN EN REG0X02\[5\]](#) enables clock gating for gain control.
- [CLK GATING ENA.CLK EQ EN REG0X02\[2\]](#) enables clock gating for the equalizer.
- [CLK DIVIDER.CLK ADC SRC REG0X03\[7:6\]](#) can reduce the clock speed.
- [TDM CTRL.ADC TXEN REG0X20\[3:0\]](#) allows ADC channels 0 through 3 to output on the I2S interface.
- [ADC FILTER CTRL.ADC ZC EN REG0X24\[15\]](#) enables zero crossing when changing the ADC volume.
- It is recommended to set [DAC FILTER CTRL 1.FILT SYNC REG0X25\[13\]](#) = 1 to set the filter reference start point based on the LRC.
- ADC path connects with DAC path by setting [PORT0 I2S PCM CTRL 1.ADDAP REG0X1C\[7\]](#)=1
- It is recommended to match [ADC FILTER CTRL.ADC RATE REG0X24\[1:0\]](#) with [CLK DIVIDER.CLK ADC SRC REG0X03\[7:6\]](#) according to the table below.

ADC RATE	CLK ADC SRC
00 (OSR=32)	11(CODEC 1/8)
01(OSR=64)	10(CODEC1/4)
10(OSR=128)	01(CODEC 1/2)
11(OSR=256)	00(CODEC CLK)

Table 12: ADC_RATE and CLK_ADC_SRC Pairs

5 DAC Digital Block

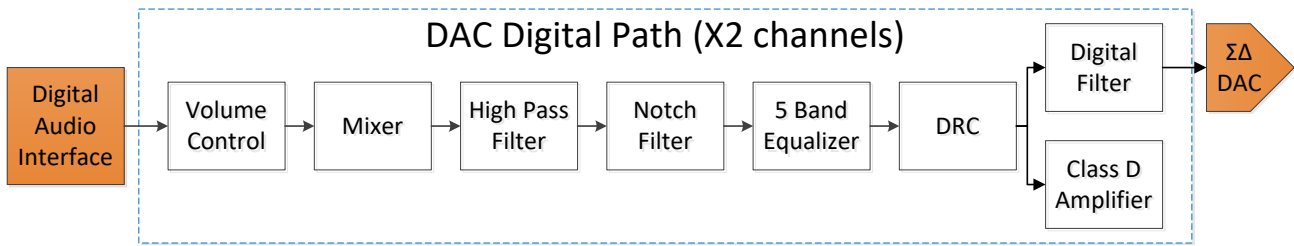


Figure 6: DAC Digital Path

The DAC digital block uses 24-bit signal processing to generate analog audio with a 16-bit digital sample stream input. This block consists of a sigma-delta modulator, digital decimator/filter, optional 5-band graphic equalizer, and a DRC. These two DAC channels are enabled by [ENA_CTRL.DAC_CH0_EN REG0X01\[4\]](#) and [ENA_CTRL.DAC_CH1_EN REG0X01\[5\]](#).

Application Notes:

- The DAC coding scheme is in twos complement format.
- The full-scale input level is proportional to VDDA. For example, with a 1.8V supply voltage, the full-scale level is 1.0V_{RMS}.
- The oversampling rate of the DAC can be changed up to 256x for improved audio performance at higher power consumption using [DAC_FILTER_CTRL_1.DAC_RATE REG0X25\[2:0\]](#).
- The DAC output signal polarity can be changed using [DAC_FILTER_CTRL_2.DACPL REG0X26\[3\]](#). This can help minimize any audio processing that may be required as the data is passed from other stages of the system.
- DAC input source from ADC by setting [PORT0_I2S_PCM_CTRL_1.ADDAP REG0X1C\[7\]=1](#)

5.1 DAC Dynamic Range Control (DRC)

The DAC DRC functions in the same way as the ADC DRC explained in Section 4.1. However, different control registers are used.

5.1.1 Level Estimation

To set the attack and decay times for the peak level estimation, use [DRC_ATKDCY_DAC.DRC_PK_COEF1_DAC REG0X48\[15:12\]](#) and [DRC_ATKDCY_DAC.DRC_PK_COEF2_DAC REG0X48\[11:8\]](#), respectively.

Bits	DRC_PK_COEF1_DAC	DRC_PK_COEF2_DAC
0000	Ts	63*Ts
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4095*Ts
0111	255*Ts	8191*Ts

Table 13: DAC Level Estimation Attack and Decay Time Register Settings

Application Notes:

- Time constant Ts shown in the register map is the sampling time given by 1/(Sampling Frequency)

5.1.2 Static Curve

The DRC static curve supports five programmable sections and can be enabled by using [DRC_KNEE_IP12_DAC.DRC_ENA_DAC REG0X45\[15\]](#). Figure 4 in section 4.1.2 shows the five programmable sections and the table below shows the related control registers.

Static Curve Section	Slope	Knee Point
LMT	DRC_SLOPE_DAC.DRC_LMT_SLP_DAC REG0X47[2:0]	
CMP1	DRC_SLOPE_DAC.DRC_CMP1_SLP_DAC REG0X47[5:3]	DRC_KNEE_IP12_DAC.DRC_KNEE1_IP_DAC REG0X45[13:8]

CMP2	DRC SLOPE DAC.DRC CMP2 SLP DAC REG0X47[8:6]	DRC KNEE IP12 DAC.DRC KNEE2 IP DAC REG0X45[4:0]
EXP	DRC SLOPE DAC.DRC EXP SLP DAC REG0X47[10:9]	DRC KNEE IP34 DAC.DRC KNEE3 IP DAC REG0X46[13:8]
NG	DRC SLOPE DAC.DRC NG SLP DAC REG0X47[13:12]	DRC KNEE IP34 DAC.DRC KNEE4 IP DAC REG0X46[5:0]

Table 14: DAC DRC Static Curve Control Registers

Application Notes:

- Smooth Knee function can be enabled by using [DRC KNEE IP12 DAC.DRC SMTH ENA DAC REG0X45\[7\]](#).
- The gain values can be individually read by using [DRC GAIN DAC CH0.DRC GAIN DAC CH0 REG0X49\[15:0\]](#) and [DRC GAIN DAC CH1.DRC GAIN DAC CH1 REG0X4A\[15:0\]](#) for DAC channel 0 and 1, respectively. The 16 bits represent decimal values; [15:10] represents integer, and [9:0] represents fraction.
- The attack time can be set using [DRC ATKDCY DAC.DRC ATK DAC REG0X48\[7:4\]](#).
- The decay time can be set using [DRC ATKDCY DAC.DRC DCY DAC REG0X48\[3:0\]](#).
- DRC needs to be carefully used combination with cross talk function because DRC is the last blocks in the path after mixer. Small cross-talk signal might be filtered out by DRC

Bits	DRC ATK DAC	DRC DCY DAC
0000	Ts	63*Ts
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4095*Ts
0111	255*Ts	8191*Ts
1000	511*Ts	16383*Ts
1001	1023*Ts	32757*Ts
1010	2047*Ts	65535*Ts
1011	4095*Ts	
1100	8191*Ts	

Table 15: DAC Static Curve Attack and Delay Time Register Settings

5.2 DAC Digital Volume Control

The digital volume control feature allows you to adjust the effective audio volume coming from the DAC using a volume control. This allows the gain to be adjusted from -128dB to +50dB with .5dB/step. Also included is a mute value that will reduce the DAC output to 0. To adjust the channel volume controls, use

[DAC CH0 DGAIN CTRL.DGAIN CH0 DAC REG0X32\[8:0\]](#),
[DAC CH1 DGAIN CTRL.DGAIN CH1 DAC REG0X33\[8:0\]](#).

Application Notes:

- Channel 0 gain can be increased an additional 0-24dB using the Class D amplifier control registers [CLASSD_GAIN_1.CLASSDGAIN1L REG0X6D\[4:0\]](#) and [CLASSD_GAIN_1.CLASSDGAIN2L REG0X6E\[4:0\]](#).
- Channel 1 gain can be increased an additional 0-24dB using the Class D amplifier control registers [CLASSD_GAIN_2.CLASSDGAIN1R REG0X6D\[12:8\]](#) and [CLASSD_GAIN_2.CLASSDGAIN2R REG0X6E\[12:8\]](#).

5.3 DAC Soft Mute

The soft mute function ramps the DAC digital volume down to zero when enabled by [DAC MUTE CTRL.SMUTE_EN REG0X31\[13\]](#). When disabled, the volume increases to the register specified volume level for each channel. This feature provides a tool that is useful for using the DAC without introducing pop and click sounds.

Also, an auto mute function will mute the DAC output audio any time there are 1024 consecutive audio samples with a zero value. The output signal unmutes whenever there is a non-zero sample value and the 1024 count will restart at 0. This function can be enabled with **DAC MUTE CTRL.AMUTE_EN REG0X31[15]**.

Application Notes:

- The AMUTE function, by default, requires that both DAC Ch0 and Ch1 have 1024 consecutive zero samples at the same time before the mute is enabled. To change this to require only one of the channels to have 1024 consecutive zero samples, use **DAC MUTE CTRL.AMUTE_CTRL REG0X31[14]**.

5.4 5-Band Equalizer

The NAU88L24 includes a 5-band graphic equalizer with low distortion and noise, and wide dynamic range that applies to both channels simultaneously. This function can be enabled with **EQ1 LOW.EQON REG0X29[9]**.

The characteristics of the 5-band equalizer are determined by the cutoff/center frequency, bandwidth, and gain settings. The table below shows the associated registers for each band.

Band	Cutoff/Center Frequency Select	Bandwidth Select	Gain Select
1 (80Hz – 175Hz)	<u>EQ1 LOW.EQ1C REG0X29[6:5]</u>	<u>EQ1 LOW.EQ1BW REG0X29[7]</u>	<u>EQ1 LOW.EQ1G REG0X29[4:0]</u>
2 (230Hz – 500Hz)	<u>EQ2 EQ3.EQ2C REG0X2A[6:5]</u>	<u>EQ2 EQ3.EQ2BW REG0X2A[7]</u>	<u>EQ2 EQ3.EQ2G REG0X2A[4:0]</u>
3 (650Hz – 1.4kHz)	<u>EQ2 EQ3.EQ3C REG0X2A[14:13]</u>	<u>EQ2 EQ3.EQ3BW REG0X2A[15]</u>	<u>EQ2 EQ3.EQ3G REG0X2A[12:8]</u>
4 (1.8kHz – 4.1kHz)	<u>EQ4 EQ5.EQ4C REG0X2B[6:5]</u>	<u>EQ4 EQ5.EQ4BW REG0X2B[7]</u>	<u>EQ4 EQ5.EQ4G REG0X2B[4:0]</u>
5 (5.3kHz – 11.7kHz)	<u>EQ4 EQ5.EQ5C REG0X2B[14:13]</u>	<u>EQ4 EQ5.EQ5BW REG0X2B[15]</u>	<u>EQ4 EQ5.EQ5G REG0X2B[12:8]</u>

Table 16: 5-Band Equalizer Setting Registers

Register Value	Equalizer Band Cutoff/Center frequency				
	EQ1C(High Pass)	EQ2C(Band Pass)	EQ3C (Band Pass)	EQ4C (Band Pass)	EQ5C (Low Pass)
00	80Hz	230Hz	650Hz	1.8kHz	5.3kHz
01	105Hz	300Hz	850Hz	2.4kHz	6.9kHz
10	135Hz	385Hz	1.1kHz	3.2kHz	9.0kHz
11	175Hz	500Hz	1.4kHz	4.1kHz	11.7kHz

Table 17: Equalizer Cutoff/Center Frequency Settings

Register Value	Gain
00000	+12db
00001	+11dB
Increments 1dB per step	
10111	-11dB
11000	-12dB

Table 18: Equalizer Gain Settings

Application Notes:

- This function can be setup to support either the ADC path or the DAC path but not both simultaneously.
- Each band can adjust the gain by ± 12 dB.
- Need to enable **CLK GATING_ENA.CLK_DACHPF_EN REG0x2[11]** for equalizer

5.5 DAC Path Digital Mixer with Side tone

The NAU88L24 implements a channel based digital mixer for DAC output that can select between ADC input channels, I2S channels and the opposing DAC output channel to mix into the output of the two DAC channels. The figure below shows a block diagram of how the mixer works along with the related registers.

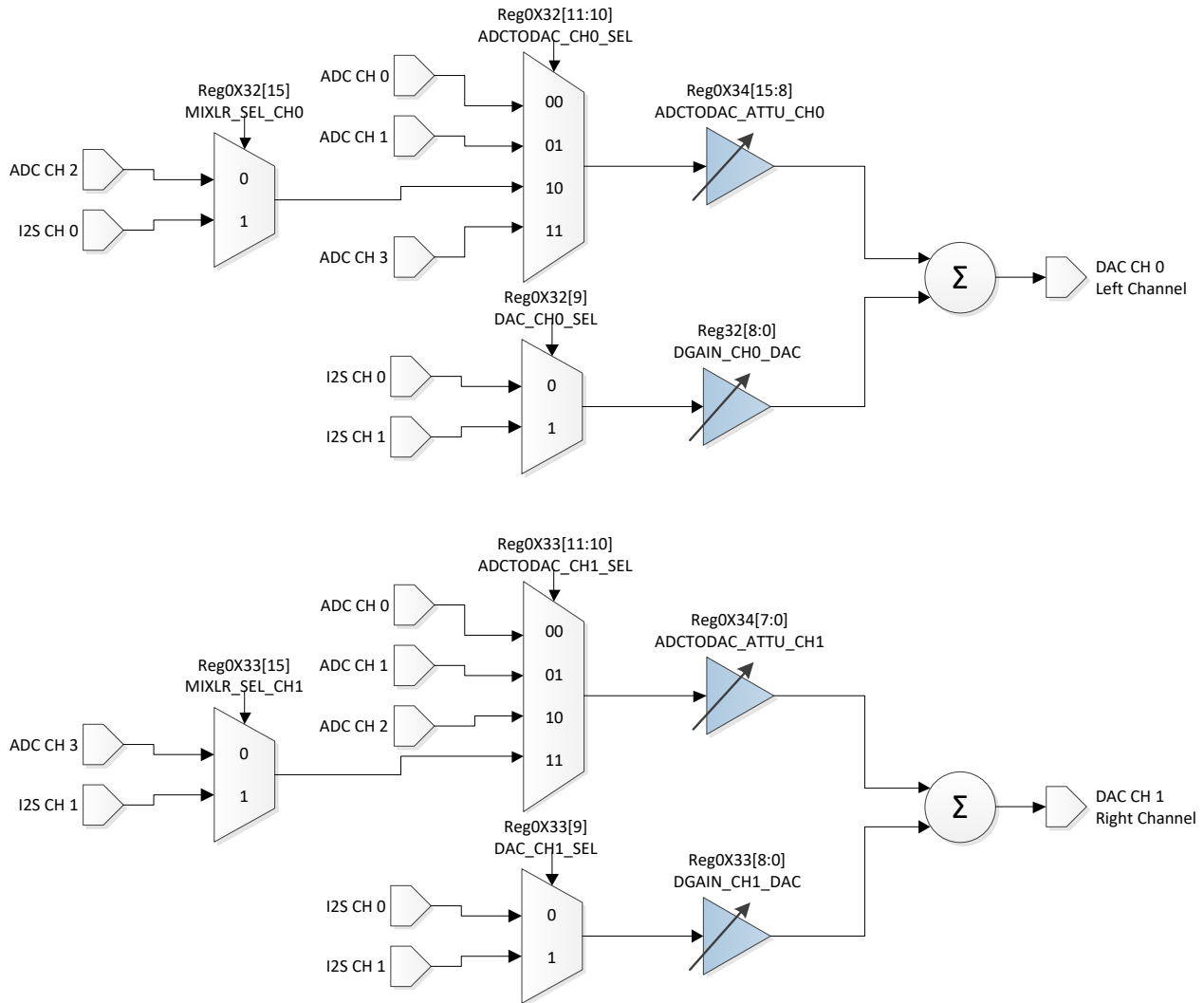


Figure 7: DAC Path Digital Mixer with Side tone

Each of the register commands in the figure above can be found in [DAC CH0 DGAIN CTRL REG0X32](#), [DAC CH1 DGAIN CTRL REG0X33](#), and [ADC TO DAC ST REG0X34](#) for DAC channels 0 and 1.

CH	DAC Output Mixer Select	ADC Channel Select	ADC Channel Gain	I2S Channel Select	I2S Channel Gain
0	MIXLR_SEL_CH0 REG0X32[15]	ADCTODAC_CH0_SEL REG0X32[11:10]	ADCTODAC_ATTU_CH0 REG0X34[15:8]	DAC_CH0_SEL REG0X32[9]	DGAIN_CH0_DAC REG0X32[8:0]
1	MIXLR_SEL_CH1 REG0X33[15]	ADCTODAC_CH1_SEL REG0X33[11:10]	ADCTODAC_ATTU_CH1 REG0X34[7:0]	DAC_CH1_SEL REG0X33[9]	DGAIN_CH1_DAC REG0X33[8:0]

Table 19: DAC Digital Mixer Control Registers

Application Notes:

- [MIXLR_SEL_CH#](#) will mix in the output of the other DAC channel's mixer when enabled. If they are not enable, ADC channel2 and channel 3 signals pass the mux.
- When initially [DAC_ZC_EN](#) is enabled with ADC to DAC side tone, DAC has data first to enable DAC path. When [DAC_ZC_EN](#) is disabled, ADC signal can pass through DAC path by side tone function without DACIN data.

5.6 Companding

Companding is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates using non-linear algorithms. The NAU88L24 supports the two main telecommunications companding standards on both transmit and receive sides: A-law and μ -law. The A-law algorithm is primarily used in European communication systems and the μ -law algorithm is primarily used by North America, Japan, and Australia.

Companding converts 14 bits (μ -law) or 13 bits (A-law) to 8 bits using non-linear quantization resulting in 1 sign bit, 3 exponent bits and 4 mantissa bits. This option can be enabled for the DAC and ADC using [PORT0_I2S_PCM_CTRL_1.DACCM REG0X1C\[15:14\]](#) and [PORT0_I2S_PCM_CTRL_1.ADCCM REG0X1C\[13:12\]](#), respectively. When the companding mode is enabled, [PORT0_I2S_PCM_CTRL_1.CMB8 REG0X1C\[10\]](#) must be enabled for 8 bit operation. This will disable the word length selection in [PORT0_I2S_PCM_CTRL_1.WLEN REG0X1C\[3:2\]](#) for this port and allow the companding functions to use an 8 bit word length.

Sections 5.6.1 and 5.6.2 contain the compression equations set by the ITU-T G.711 standard and implemented in the NAU88L24.

5.6.1 μ -law

$$F(x) = \frac{\ln(1 + \mu \times |x|)}{\ln(1 + \mu)}, \quad -1 < x < 1$$

$$\mu = 255$$

5.6.2 A-law

$$F(x) = \frac{A \times |x|}{(1 + \ln(A))}, \quad 0 < x < \frac{1}{A}$$

$$F(x) = \frac{(1 + \ln(A \times |x|))}{(1 + \ln(A))}, \quad \frac{1}{A} \leq x \leq 1$$

$$A = 87.6$$

5.7 Additional DAC Application Notes

- [CLK_GATING_ENA.CLK_DAC_PL REG0X02\[9\]](#) inverts the clock polarity.
- [CLK_GATING_ENA.CLK_GAIN_EN REG0X02\[5\]](#) enables clock gating for gain control.
- [CLK_GATING_ENA.CLK_EQ_EN REG0X02\[2\]](#) enables clock gating for the equalizer.
- [CLK_DIVIDER.CLK_DAC_SRC REG0X03\[5:4\]](#) can scale the clock speed.
- [TDM_CTRL.DAC_LSEL REG0X20\[7:6\]](#) selects DAC channel 0 slot number in I2C/PCM TDM mode.
- [TDM_CTRL.DAC_RSEL REG0X20\[5:4\]](#) selects DAC channel 1 slot number in I2C/PCM TDM mode.
- [DAC_FILTER_CTRL_1.DISABLE_DEM REG0X25\[15\]](#) disables DEM control to RateConvert2 module.
- [DAC_FILTER_CTRL_1.FILT_SYNC REG0X25\[13\]](#) sets the filter reference start point.
- [DAC_FILTER_CTRL_1.CICCLP_OFF REG0X25\[7\]](#) recommended set to 1.
- [DAC_FILTER_CTRL_1.CIC_GAIN_ADJ REG0X25\[6:4\]](#) sets the DAC CICI gain.
- [DAC_FILTER_CTRL_1.DAC_RATE REG0X25\[2:0\]](#) sets the DAC oversample rate.
- [DAC_FILTER_CTRL_2.DEM_DITHER REG0X26\[15:12\]](#) sets the probability of first order dynamic element matching dither.
- [DAC_FILTER_CTRL_2.DAC_STEP_SEL REG0X26\[6:4\]](#) sets the DAC output delay.
- [DAC_FILTER_CTRL_2.DAC_PL REG0X26\[3\]](#) sets the DAC output polarity.
- [DAC_FILTER_CTRL_2.DACIN_SRC REG0X26\[2:0\]](#) selects the DAC input source.
- [DAC_MUTE_CTRL.DAC_ZC_EN REG0X31\[11\]](#) enables zero crossing on the DAC output to reduce pops or clicks when changing the gain.
- [DAC_MUTE_CTRL.DAC_CH01_MIXER REG0X31\[1:0\]](#) enables half power mixing of the two DAC output channels.

6 Clocking and Sample Rates

The internal clocks for the NAU88L24 are derived from a common internal clock source, [CLK_DIVIDER.SYSCLOCK_SRC REG0X03\[15\]](#). This master system clock can set directly by the MCLK_PIN input or it can be generated from a Frequency Locked Loop (FLL) using the MCLK_PIN, BCLK or FS as a reference. While most of the common audio sample rates can be derived directly from typical MCLK

frequencies, the FLL provides additional flexibility for a wide range of MCLK inputs or as a free running clock in the absence of an external reference.

The figures below is a block diagram illustrating how the various register settings can be used to adjust/select the MCLK, BCLK, FS, and ADC_CLK clock frequency.

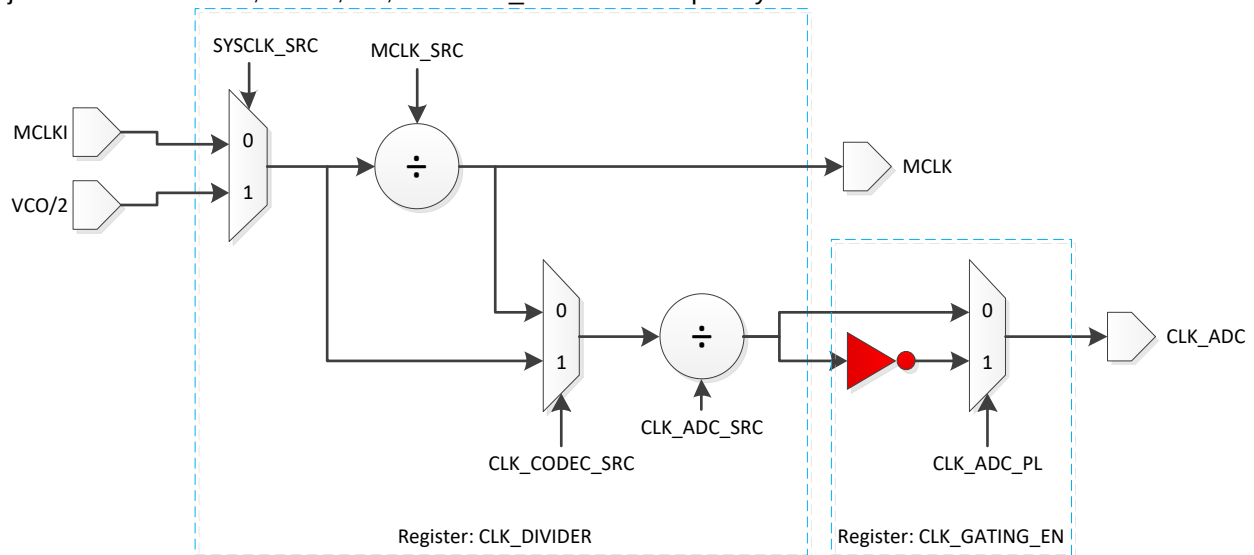


Figure 8: MCLK and ADC_CLK Frequency Selection

Bits	MCLK_SRC
0000	Divide by 1
0001	Invert
0010	Divide by 2
0011	Divide by 4
0100	Divide by 8
0101	Divide by 16
0110	Divide by 32
0111	Divide by 3
1001	Invert
1010	Divide by 6
1011	Divide by 12
1100	Divide by 24

Table 20: CLK_DIVIDER.MCLK_SRC REG0X03[3:0] Register Settings

Bits	CLK_ADC_SRC
00	Divide by 1
01	Divide by 2
10	Divide by 4
11	Divide by 8

Table 21: CLK_DIVIDER.CLK_ADC_SRC REG0X03[7:6] Register Settings

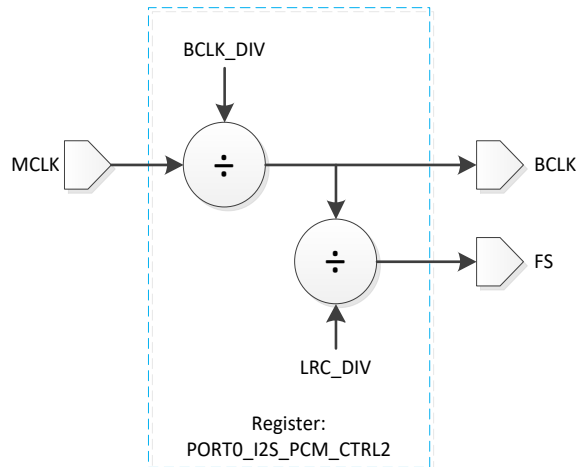


Figure 9: BCLK and FS Frequency Selection

Bits	BCLK_DIV
000	Divide by 1
001	Divide by 2
010	Divide by 4
011	Divide by 8
100	Divide by 16
101	Divide by 32

Table 22: PORT0_I2S_PCM_CTRL_2.BCLK_DIV REG0X1D[2:0] Register Settings

Bits	LRC_DIV
00	Divide by 256
01	Divide by 128
10	Divide by 64
11	Divide by 32

Table 23: PORT0_I2S_PCM_CTRL_2.LRC_DIV REG0X1D[13:12] Register Settings

Application Notes:

- To avoid audible glitches, all clock configurations must be setup before enabling playback.
- To ensure the best performance, MCLK must be running at 256x the desired sample rate (Fs).
- If MCLK is at a higher frequency than desired, CLK_DIVIDER.MCLK_SRC REG0X03[3:0] can be used to scale the MCLK frequency.
- The ADC clock frequency is set by CLK_DIVIDER.CLK_CODEC_SRC REG0X03[13] and CLK_DIVIDER.CLK_ADC_SRC REG0X03[7:6] registers and must remain smaller than 6.144MHz. For example, this device can support an OSR of 128 with Fs = 48k resulting in a clock frequency of 128 x 48k = 6.144MHz.
- The GPIO1 pin can be set to output a clock with frequency scaled by CLK_DIVIDER.CLK_GPIO_SRC REG0X03[9:8] and enabled using GPIO_SEL.GPIO1SEL REG0X1A[2:0].
- CLASSG.CLASSG_EN REG0X50[0] and CLASSG.CLASSG_CLK_SRC REG0X50[15:14] are used to enable a slower clock to de-bounce the button/accessory detect inputs and set the time period for volume updates when zero crossing is enabled.
- PORT0_I2S_PCM_CTRL_1.BCLK_DIV REG0X1D[2:0] sets BCLK from SYSCLK in master mode.
- PORT0_I2S_PCM_CTRL_1.LRC_DIV REG0X1D[13:12] and the BCLK are used to set the Fs.
- It is recommended to disable SYSCLK_SRC and then re-enable it after the entire setting shave been updated.

6.1 Frequency Locked Loop (FLL)

- $MCLK = 256 \times 48\text{kHz} = 12.288\text{MHz}$
- Using Equation 2:
- o $FDCO = (2 \times 12.288\text{MHz}) / \text{MCLK_SRC_REG0X03[3:0]}$
- For FDCO to remain between 90MHz – 100MHz, MCLK_SRC_REG0X03[3:0] must be chosen to be 1/4. This and other values for MCLK_SRC_REG0X03[3:0] can be seen on the register tables.
- o $FDCO = (2 \times 12.288\text{MHz}) / (1/4) = 98.304\text{MHz}$
- Using Equation 1:
- $\text{FLL_INTEGER_REG0X06[9:0]} \cdot \text{FLL_FRAC_REG0X05[15:0]} = FDCO / FREF \times \text{FLL_CLK_REF_DIV[11:10]}$
- o $\text{FLL_RATIO_REG0X04[6:0]} = 1$ because $FREF \geq 512 \text{ kHz}$. This and other values for FLL_RATIO_REG0X04[6:0] can be seen on the register tables.
- o $\text{FLL_INTEGER} \cdot \text{FLL_FRAC_REG0X06[15:0]} = 98.304\text{MHz} / (12\text{MHz} \times 1) = 8.192$
- $\text{FLL_INTEGER_REG0X06[9:0]} \cdot \text{FLL_FRAC_REG0X05[15:0]}$ represents an integer + decimal number.)
- o $\text{FLL_INTEGER_REG0X06[9:0]} = 8$
- o $\text{FLL_FRAC_REG0X05[15:0]} = 0.192$
- Now retrieve or convert the parameter values into their corresponding HEX values
- o $\text{FLL_RATIO_REG0X04[6:0]} = 7'h1$ (this value is taken from the register chart in $FREF \geq 512\text{kHz}$ condition.)
- o $\text{MCLK_SRC_REG0X03[3:0]} = 4'h3$ (this value is taken from the register chart for MCLK_SRC_REG0X03[3:0] = 1/4)
- o $\text{FLL_INTEGER_REG0X06[9:0]} = 8 = 10'h8$
- o $\text{FLL_FRAC_REG0X05[15:0]} = 0.192 \times 2^{16} = 12583 = 16'h3126$

Application Notes:

- FLL4.FLL_CLK_REF_DIV_REG0X07[11:10] can be used to reduce the reference frequency for SYSMCLK by dividing the input by 1, 2, 4, or 8. Use this to ensure the reference clock frequency is less than or equal to 13.5MHz.
- FLL3.GAIN_ERR_REG0X06[14:12] and FLL5.FLL_CLK_REF_DIV_4CHK_REG0X07[14:12] are used to control the gain and resolution, respectively. It is recommended that the default settings are used for these parameters.
- FDCO must be within the 90MHz – 100MHz or the FFL cannot be guaranteed across the full range of operation.
- FLL2.FLL_FRAC_REG0X05[15:0] must be set to 0 for low power mode.
- FLL6.SDM_EN_REG0X09[14] to create decimal part of frequency, if (DCO frequency)/(FLL input reference frequency) is not a integer. If the ratio is integer, it still can be on for lower noise output but higher power consumption.
- When FLL uses free running mode, NAU88L24 needs to be set as a master in PORT0_I2S_PCM_CTRL_2.MS0_REG0X1D[3]=1
- Set FLL6.CHB_FILTER_EN_REG0X08[14] = '1' to enable FLL Loop Filter. Select filter clock source by FLL6.CHB_FILTER_EN_REG0X08[13]. Select DCO input by FLL6.FILTER_SW_REG0X08[12]. FLL6.CUTOFF500_REG0X09[13] & FLL6.CUTOFF600_REG0X09[12] can be used to define FLL cutoff frequency at 500KHz or 600KHz. 500KHz will provide the best FLL performance but consume more power.
- set FLL6.FLL_FLTR_DITHER_SEL_REG0X09[7:6] = '01' or '10' or '11' as 1LSB / 2LSB / 3LSB random bits to Randomize the number of Filter Output Bits to average out output noise. If '00', there is no dither.

7 Control Interfaces

The NAU88L24 includes a serial control bus that provides access to all of the device control registers and may be configured as a 2-wire interface that conforms to industry standard implementations of the I2C serial bus.

7.1 2-Wire-Serial Control Mode (I²C Style Interface)

The 2-wire bus is a bidirectional serial bus protocol. This protocol defines any device that sends data onto the bus as a transmitter (or master), and the receiving device as the receiver (or slave). The NAU88L24 can function only as a slave device when in the 2-wire interface configuration.

7.2 2-Wire Protocol Convention

To initiate communication, all 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDIO while SCLK is HIGH.

Following a START condition, the master must output a device address byte consisting of a 7-bit device address, and a Read/Write control bit in the LSB of the address byte. To read from the slave device, the R/W bit must be set to 1. To initiate a write to the slave device, the R/W bit must be 0. If the device address matches the address of a slave device, the slave will output an acknowledgement bit.

An acknowledge (ACK), is a software convention used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDIO bus after transmitting eight bits and during the ninth clock cycle, the receiver (slave) pulls the SDIO line LOW to acknowledge the reception of the eight bits of data.

To terminate a read/write session, all 2-Wire interface operations must end with a STOP condition, which is a LOW to HIGH transition of SDIO while SCLK is HIGH. A STOP condition at the end of a read or write operation places the device in a standby mode.

Application Notes:

- The NAU88L24 is permanently programmed with “0011010” as the Device Address.

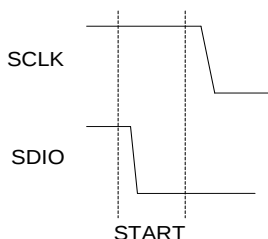


Figure 11: Valid START Condition

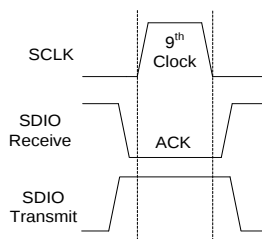


Figure 12: Valid Acknowledge

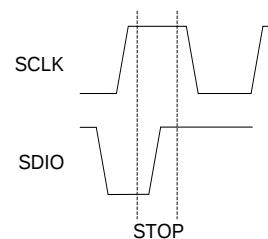


Figure 13: Valid STOP Condition

7.3 2-Wire Write Operation

A Write operation consists of a three-byte instruction followed by one or more data bytes as seen in Figure 14. These instructions consist of the Address byte and two Control Address bytes that precede the START condition and are followed by the STOP condition. Figure 15 shows the data bus and the corresponding clock cycles.

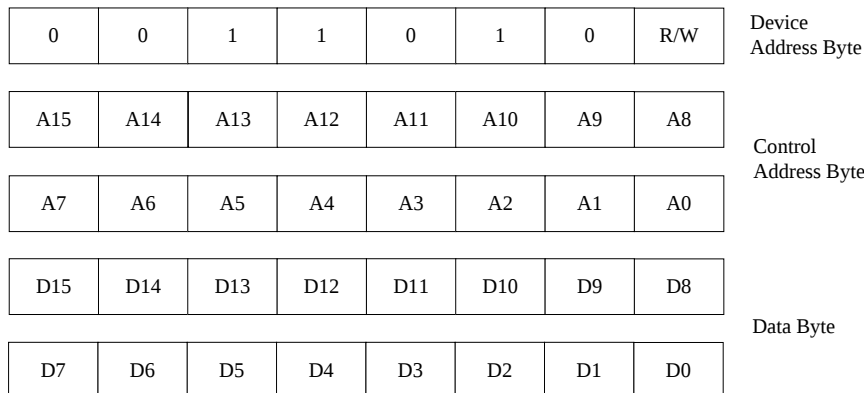


Figure 14: Slave Address Byte, Control Address Byte, and Data Byte

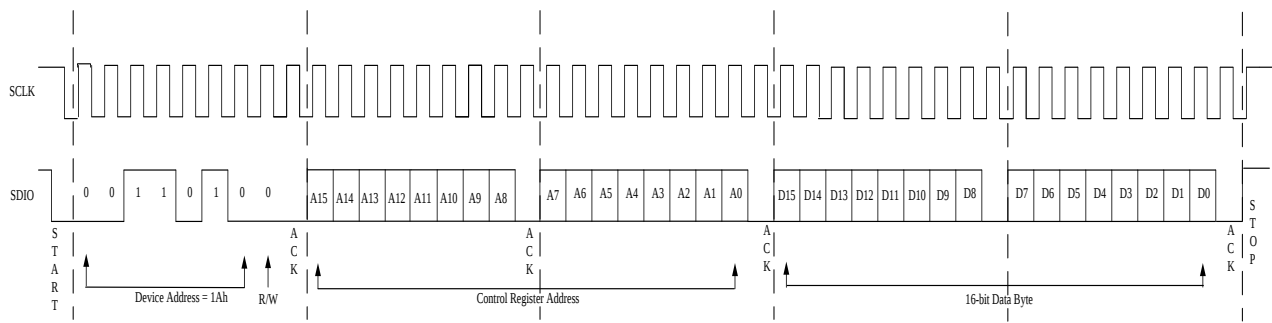


Figure 15: 2-Wire Write Sequence

7.4 2-Wire Read Operation

A Read operation consists of the three-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, Device Address byte with the R/W bit set to "0", and a Control Register Address byte. This indicates to the NAU88L24 which of its control registers is going to be accessed.

After this, the NAU88L24 will respond with an ACK as it accepts the Control Register Address that the master is transmitting to it. After the Control Register Address has been sent, the master will send a second START condition and Device address but with R/W = 1.

After the NAU88L24 recognizes its Device Address the second time, it will transmit an ACK followed by a two byte value containing the 16 bits of data in the NAU88L24 control registers requested by the master. During this phase, the master generates an ACK with each byte of data transferred.

After the two bytes have been transmitted, the master will send a STOP condition ending the read phase. If no STOP condition is received, the NAU88L24 will automatically increment the target Control Register Address and then start sending the two bytes of data for the next register in the sequence. This will continue as long as the master continues to send ACK signals. Once the target register reaches 0xFFFF, it will send the associated data then roll over to 0x0000 and continue as before.

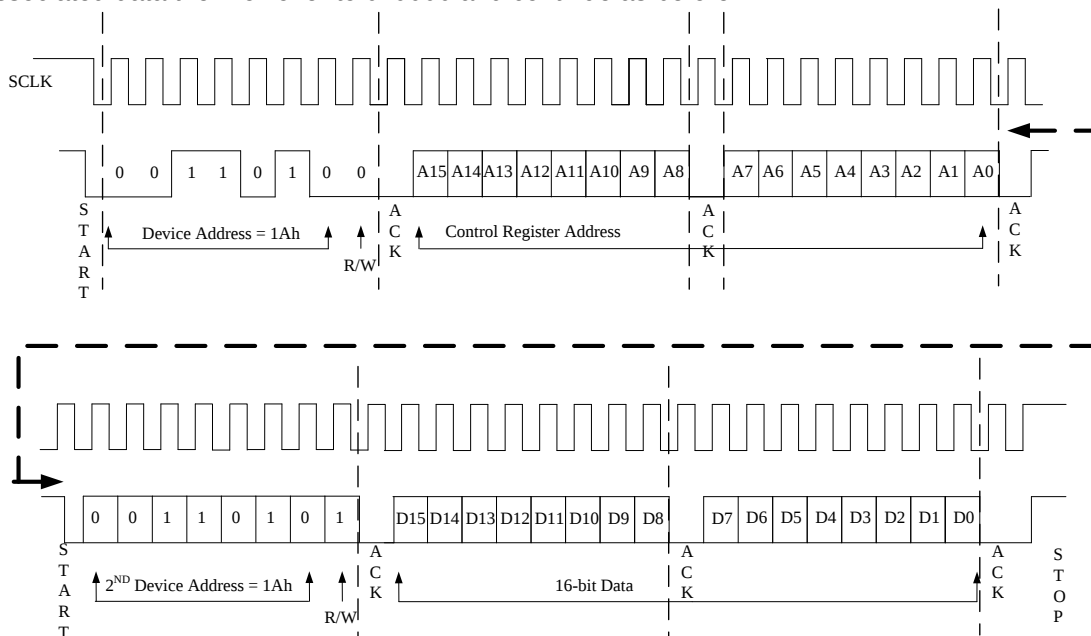


Figure 16: 2-Wire Read Sequence

7.5 Digital Serial Interface Timing

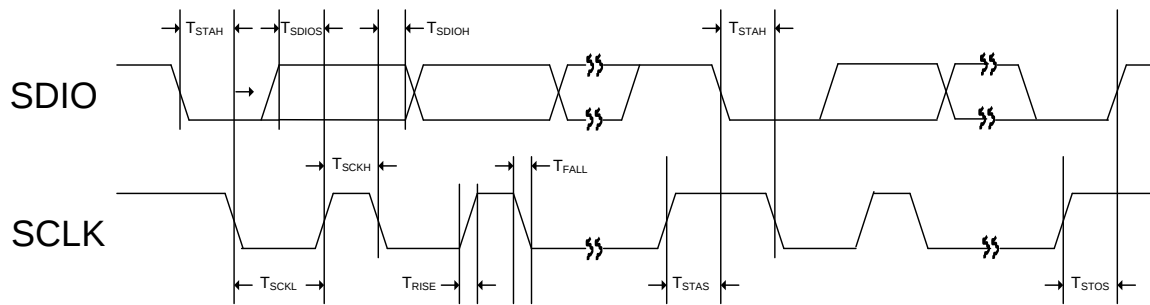


Figure 17: Two-wire Control Mode Timing

Symbol	Description	min	typ	max	unit
T _{STAH}	SDIO falling edge to SCLK falling edge hold timing in START / Repeat START condition	600	-	-	ns
T _{STAS}	SCLK rising edge to SDIO falling edge setup timing in Repeat START condition	600	-	-	ns
T _{STOS}	SCLK rising edge to SDIO rising edge setup timing in STOP condition	600	-	-	ns
T _{SCKH}	SCLK High Pulse Width	600	-	-	ns
T _{SCKL}	SCLK Low Pulse Width	1,300	-	-	ns
T _{RISE}	Rise Time for all 2-wire Mode Signals	-	-	300	ns
T _{FALL}	Fall Time for all 2-wire Mode Signals	-	-	300	ns
T _{SDIOS}	SDIO to SCLK Rising Edge DATA Setup Time	100	-	-	ns
T _{SDIOH}	SCLK falling Edge to SDIO DATA Hold Time	0	-	600	ns

7.1 Four-Wire SPI Control Interface

The 56-Ball WLCSP package of the NAU88L24 supports 4-Wire SPI Write and Read Control Interface Modes. For SPI Writes, only the CSB, SCLK, and SDIO pins are needed. During SPI Reads, an additional pin, GPIO4, is needed. The SPI 4-Wire Read/Write Modes are enabled when the NAU88L24 IFSEL pin is in a logical HIGH condition. In Read Mode, GPIO4 needs to be enabled by writing **REG0X19[7]**.

7.1.1 Four-Wire SPI Write Operation

The SPI 4-Wire Write operation is a full SPI data transaction. However, only three wires are needed, as this is a write-only operation with no return data. A fourth wire is needed only when there are bi-directional data. The CSB/GPIO1 pin on the NAU88L24 is used as the Chip Select function in an SPI transaction. Refer to **Figure 18**.

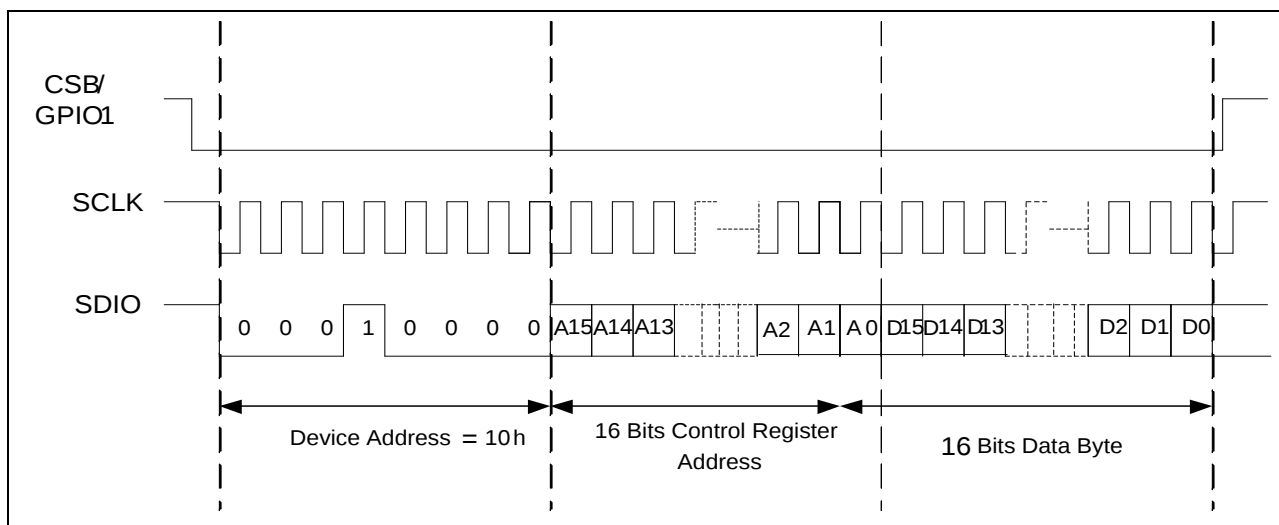


Figure 18 Four-Wire SPI Interface Write Operation

Note: The 4-wire SPI Interface is supported *only* when using the 42-Ball WLCSP package.

After CSB/GPIO1 is held in a logical LOW condition, data bits from SDIO are clocked into the NAU88L24 on every rising edge of SCLK. A Write operation is indicated by the value 0x10 (hexadecimal) placed in the Device Address byte of the transaction. This byte is followed by a 16-bit Control Register Address and a 16-bit data value packed into the next two bytes of a four-byte sequence. After the Least Significant Bit (LSB) of the 16-bit data is clocked into the NAU88L24, the 16-bit data value is automatically transferred to the NAU88L24 register addressed by the Control Register Address value.

If only a single register is to be written, CSB/GPIO1 must be put into a logical HIGH condition after the LSB of the Data Byte is clocked into the device. If CSB/GPIO1 remains in a logical LOW condition, the NAU88L24 will auto-index the Control Register Address value and the next two bytes will be clocked into the next sequential NAU88L24 register address. This will continue as long as CSB/GPIO1 is in the logical LOW condition. If the Control Register Address being indexed inside the NAU88L24 reaches the value 0x82 (hexadecimal), then after the value for this register is written, the index will roll over to 0x01 and the process will continue.

7.1.2 Four-Wire SPI Read Operation

The Four-Wire SPI Read Operation is a full SPI data transaction with a two-byte address phase and a two-byte data phase. The CSB/GPIO1 pin on the NAU88L24 is used as the Chip Select function in the SPI transaction. Refer to **Figure 19**.

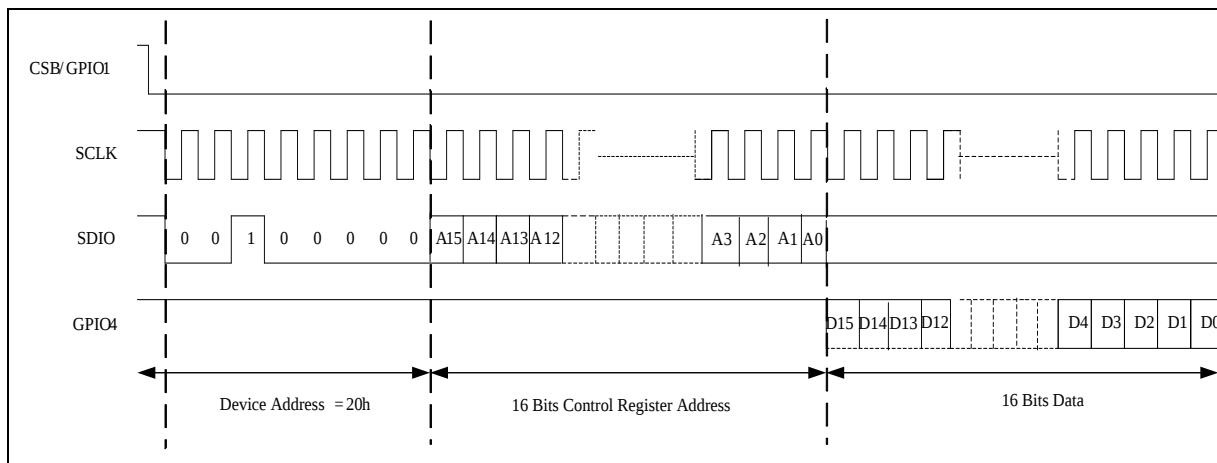


Figure 19 Four-Wire SPI Interface Read Operation

Note: The four-wire SPI Interface is supported *only* when using the 56-Ball WLCSP package.

After CSB/GPIO1 is held in a logical LOW condition, a Read operation is indicated by the value 0x20 (hexadecimal) placed in the Device Address byte of the transaction. This byte is followed by a 16-bit Control Register Address.

After the LSB of the Control Register Address is clocked, the NAU88L24 will begin outputting its 16-bit data on the GPIO4 pin, beginning with the very next SCLK rising edge provided by the Master. This data is transmitted in two bytes, which are transmitted Most Significant Bit (MSB) first.

If only a single register is to be read, CSB/GPIO1 must be put into a logical HIGH condition after the LSB of the 16-bit data is clocked from the NAU88L24. If CSB/GPIO1 remains in a logical LOW condition, the NAU88L24 will auto-index the Control Register Address value and the next two bytes will be clocked from the next sequential NAU88L24 register address. This will continue as long as CSB/GPIO1 is in the logical LOW condition. If the Control Register Address being indexed inside the NAU88L24 reaches the value 0x82 (hexadecimal), then after the value for this register is output, the index will roll over to 0x01 and the process will continue.

7.2 Software Reset

The NAU88L24 and all of its control registers can be reset to default initial conditions by writing any value to REG0X00 twice using any of the control interface modes. Writing to any other valid register address terminates the reset condition, but all registers will now be set to their power-on default values.

8 Digital Audio Interfaces

The NAU88L24 can be configured as either the master or the slave, by setting register **PORT0_I2S_PCM_CTRL_2.MS REG0X1D[3]**, to 1 for master mode and to 0 for slave mode. Slave mode is the default if this bit is not written. In master mode, NAU88L24 outputs both Frame Sync (FS) and the audio data bit clock (BCLK) and has full control of the data transfer. In the slave mode, an external controller supplies BCLK and FS. Data is latched on the rising edge of BCLK; SDO clocks out ADC data, while SDI clocks in data for the DACs. When FLL is set to free running mode, NAU88L24 is needed to set as a master. When not transmitting data, SDO pulls LOW in the default state. Depending on the application, the output can be configured to pull up or pull down. When the time slot function is enabled (see below), there are additional output state modes including controlled tri-state capability. NAU88L24 supports six audio formats; right justified, left justified, I2S, PCM A, PCM B, and PCM Time Slot.

PCM Mode	PORT0_I2S_PCM_CTRL_1.AIFMT REG0X1C[1:0]	PORT0_I2S_PCM_CTRL_1.LRP REG0X1C[6]	PORT0_I2S_PCM_CTRL_2.PCM_TS REG0X1D[10]
Right Justified	00	0	0
Left Justified	01	0	0
I ² S	10	0	0
PCM A	11	0	0
PCM B	11	1	0
PCM Time Slot	11	Don't care	1

Table 24: Digital Audio Interface Modes

8.1 Right-Justified Audio Data

In right-justified mode, the LSB is clocked on the last BCLK rising edge before FS transitions. When FS is HIGH, channel 0 data is transmitted and when FS is LOW, channel 1 data is transmitted. This can be seen in the image below.

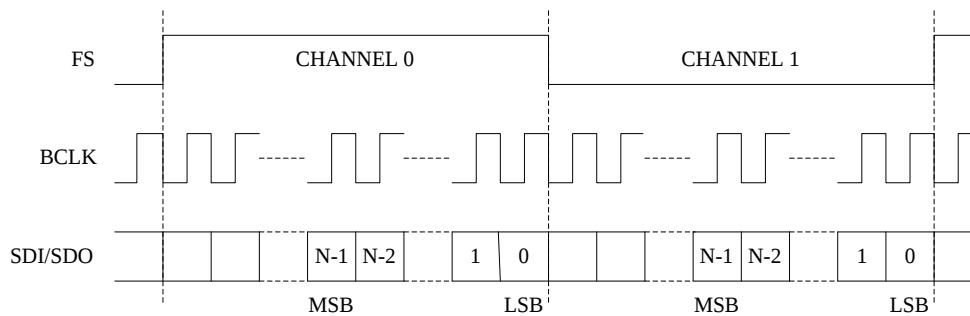


Figure 20: Right-Justified Audio Interface

8.2 Left-Justified Audio Data

In left-justified mode, the MSB is clocked on the first BCLK rising edge after FS transitions. When FS is HIGH, channel 1 data is transmitted and when FS is LOW, channel 0 data is transmitted. This can be seen in the figure below.

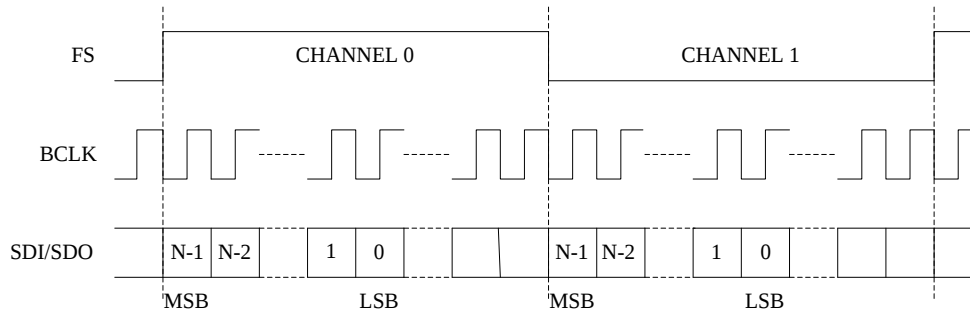


Figure 21: Left-Justified Audio Interface

8.3 I2S Audio Data

In I²S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, left channel data is transmitted and when FS is HIGH, right channel data is transmitted. This can be seen in the figure below.

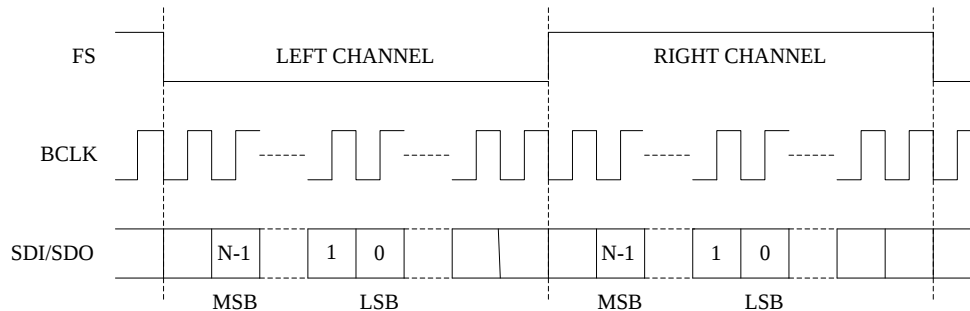


Figure 22: I2S Audio Interface

8.4 PCM A Audio Data

In the PCM A mode, channel 0 data is transmitted first followed immediately by channel 1 data. The channel 0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and channel 1 MSB is clocked on the next BCLK after the left channel LSB. This can be seen in the figure below.

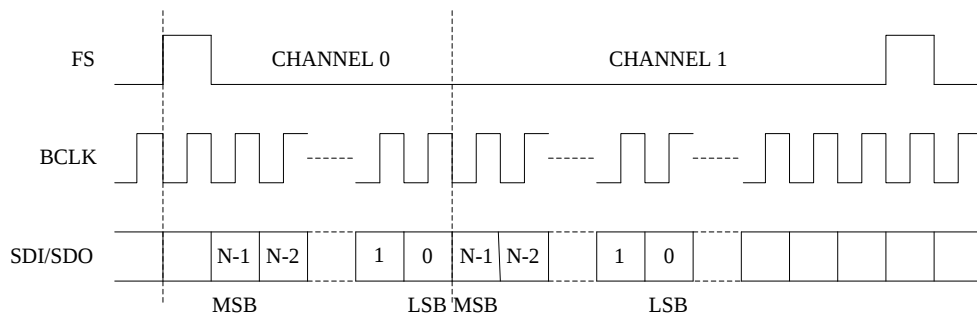


Figure 23: PCM A Audio Interface

8.5 PCM B Audio Data

In the PCM B mode, channel 0 data is transmitted first followed immediately by channel 1 data. Channel 0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and channel 1 MSB is clocked on the next BCLK after channel 0 LSB. This can be seen in the figure below.

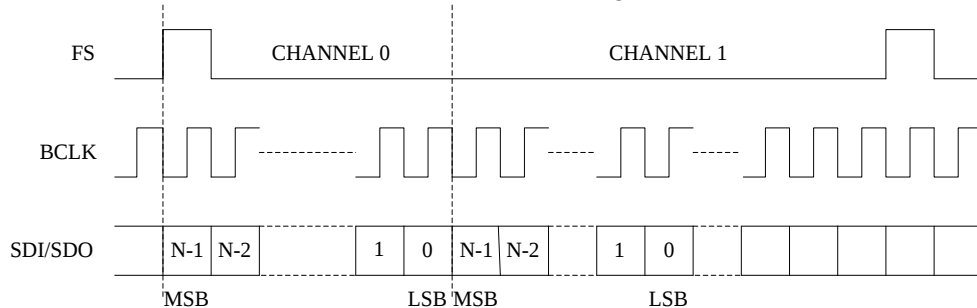


Figure 24: PCM-B Audio Interface

8.6 PCM Time Slot Audio Data

The PCM time slot mode is used to delay the time at which the DAC and/or ADC data are clocked. This can be useful when multiple NAU88L24 chips or other devices are sharing the same audio bus. This will allow each chip's audio to be delayed around each other without interference.

Normally, the DAC and ADC data are clocked immediately after the Frame Sync (FS), however, in the PCM time slot mode; the audio data can be delayed by [PORT0 LEFT TIME SLOT.TSLOT L REG0X1E\[9:0\]](#) and [PORT0 RIGHT TIME SLOT.TSLOT R REG0X1F\[9:0\]](#) for the left and right channel, respectively. [PORT0 I2S PCM CTRL 2.PCM TS REG0X1D\[10\]](#) needs to set to 1. These delays can be seen before the MSB in the figure below.

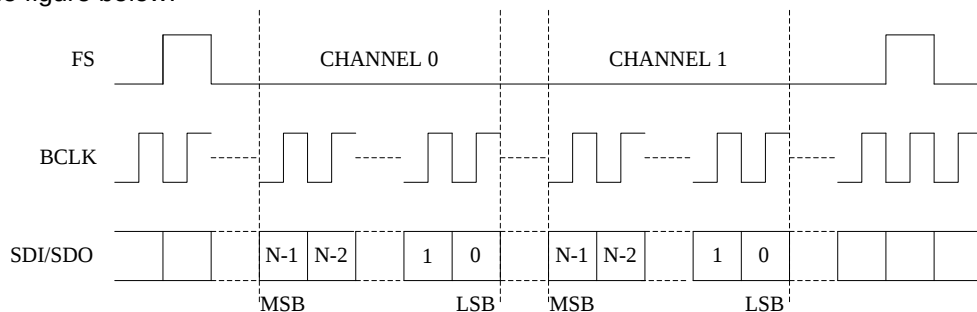


Figure 25: PCM Time Slot Audio Interface

Application Notes:

- This mode can be used to swap channel 0 and channel 1 audio or cause both channels to use the same data.
- When using the NAU88L24 with other driver chips, the SDO pin can be set to pull up or pull down by enabling [PORT0 I2S PCM CTRL 2.ADCDAT PE REG0X1D\[6\]](#) and selecting up or down with [PORT0 I2S PCM CTRL 2.ADCDAT PS REG0X1D\[5\]](#). This allows for wired-OR type bus sharing. If

both are set to 0, SDO is high impedance, except when transmitting channel audio data. Tri-stating on the negative edge allows the transmission of data by multiple sources in adjacent timeslots with reduced risk of bus driver contention.

- **PORT0 I2S PCM CTRL 2.ADCDAT OE REG0X1D[4]** by default actively drives the SDO pin (never in high impedance state). This needs to be disabled in order to share the data line.

8.7 TDM I2S Audio Data

In I2S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, channel 0 then channel 2 data is transmitted and when FS is HIGH, channel 1 then channel 3 channel data is transmitted. This is shown in the figure below.

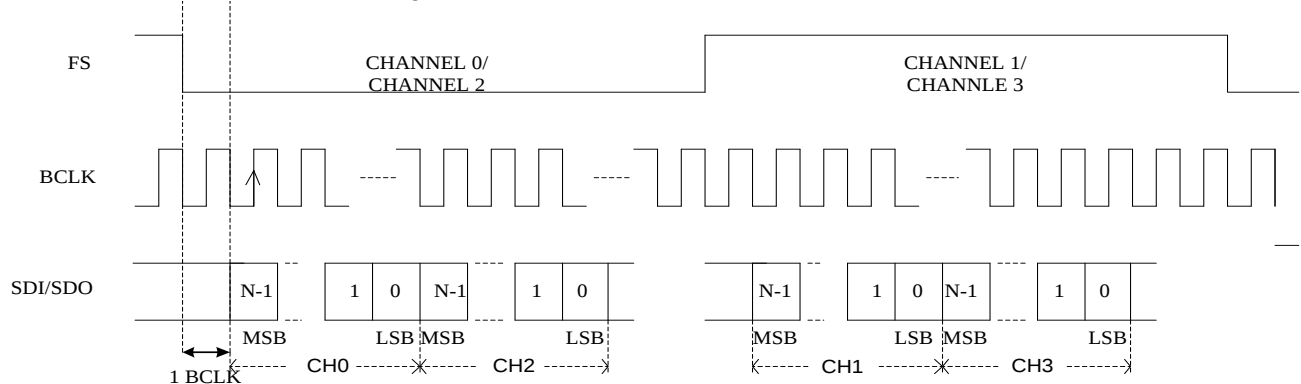


Figure 26: TDM I2S Audio Format

8.8 TDM PCM A Audio Data

In the PCM A mode, channel 0 data is transmitted first followed sequentially by channel 1, 2, and 3 immediately after. The channel 0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This is shown in the figure below.

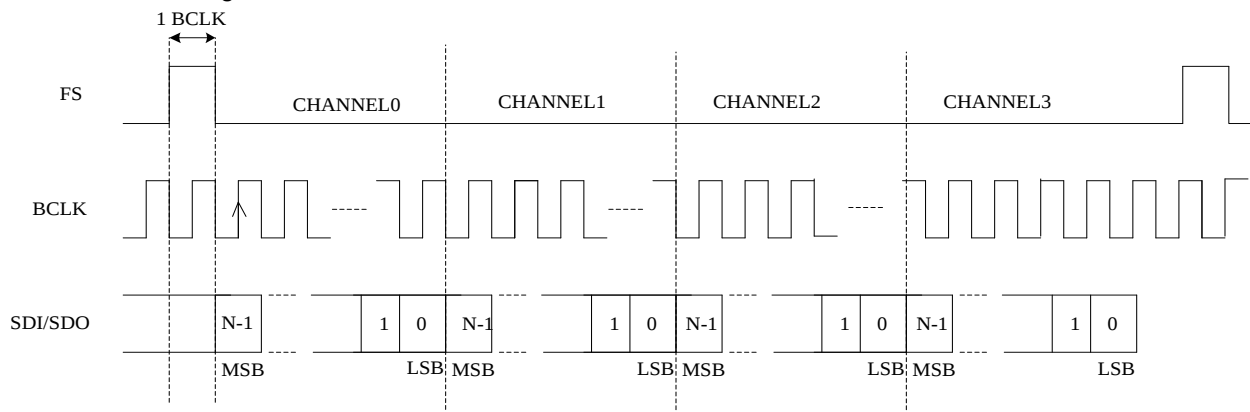


Figure 27: TDM PCM A Audio Format

8.9 TDM PCM B Audio Data

In the PCM B mode, channel 0 data is transmitted first followed immediately by channel 1 data. The channel 0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and channel 1 MSB is clocked on the next SCLK after channel 0 LSB.

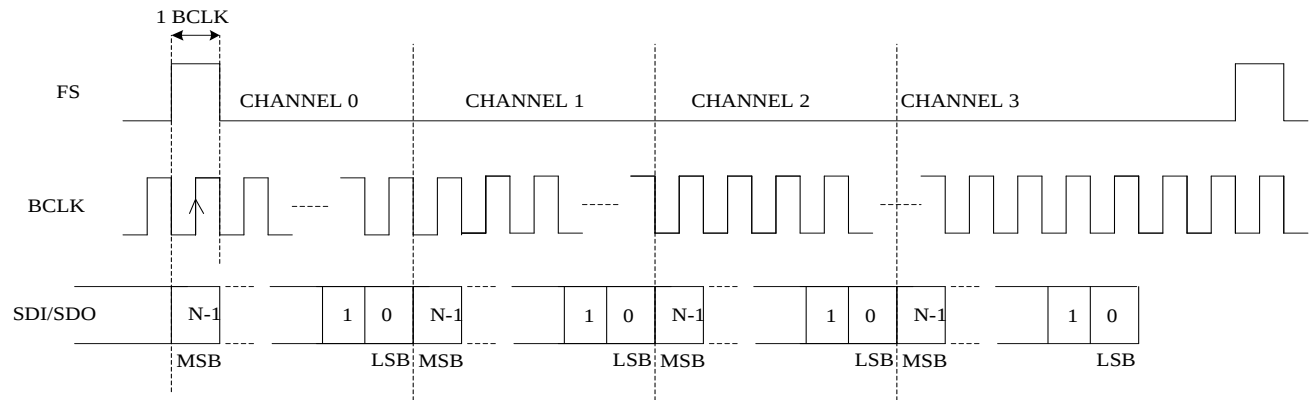


Figure 28: TDM PCM B Audio Format

8.10 TDM PCM Offset Audio Data

The PCM offset mode is used to delay the time at which the ADC data is clocked. This increases the flexibility of the NAU88L24 to be used in a wide range of system designs. One key application of this feature is to enable multiple NAU88L24 or other devices to share the audio data bus, thus enabling more than four channels of audio. This feature may also be used to swap channel data, or to cause multiple channels to use the same data. [TDM_CTRL.TDM_MODE REG0X20\[15\]](#) and [TDM_CTRL.TDM_PCM_TS_MODE REG0X20\[14\]](#) must be set to 1 for this application.

Normally, the ADC data are clocked immediately after the Frame Sync (FS). In this mode audio data is delayed by a delay count specified in the device control registers. The channel 0 MSB is clocked on the BCLK rising edge defined by the delay count set in [PORT0_LEFT_TIME_SLOT.TSLOT_L REG0X1E\[9:0\]](#). The subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This can be seen in the figure below.

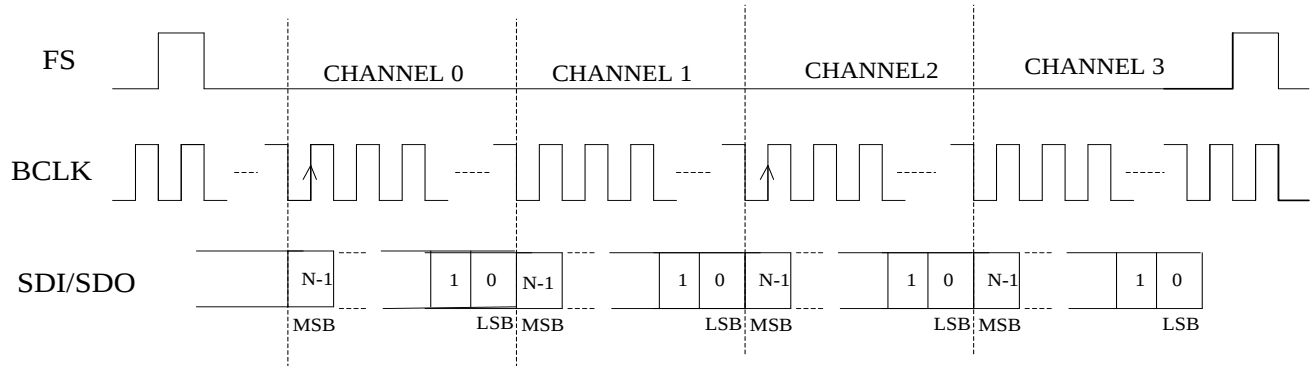


Figure 29: TDM PCM Offset Audio Format

Application Notes:

- When using [PORT0_LEFT_TIME_SLOT.TSLOT_L REG0X1E\[9:0\]](#) for time slot shift in TDM mode, the four channels will shift together for the same chip. The shift number should be $N \times \text{Word Length} + 1$, and available channels should be $> N + 4$, where N is desired channel width shift.

9 Outputs

The NAU88L24 provides two types of integrated output drivers. The stereo pair of high power, high quality Class D speaker drivers, which can support 3W each in stereo mode and a pair of Class G ground-reference headphone outputs.

9.1 Stereo Class D Speaker Outputs

The speaker driver is a stereo high efficiency filter-free Class-D audio amplifier, which is capable of driving an 8Ω load with up to 1.76W output power. These speaker drivers include features like 80dB PSRR, 86% efficiency, ultra-low quiescent current (i.e. 2.1mA at 3.7V for 2 channels) and superior EMI performance that make it ideal for portable applications.

To enable the speaker drivers use [CLASSD_GAIN_1.ENCLASSD_REG0X6D\[7\]](#) and the overall Class D gain can be set with [CLASSD_GAIN_1.GAINCLASSD_REG0X6D\[15:13\]](#). Individual channel output gain can also be set using [CLASSD_GAIN_1.CLASSDGAIN1L_REG0X6D\[4:0\]](#) and

[CLASSD_GAIN_1.CLASSDGAIN1R_REG0X6D\[12:8\]](#) for driver 1 and

[CLASSD_GAIN_2.CLASSDGAIN2L_REG0X6E\[4:0\]](#) and [CLASSD_GAIN_2.CLASSDGAIN2R_REG0X6E\[12:8\]](#) for driver 2.

Parameter	Symbol	Comments/Conditions		Typ	Units
Output Power (per channel)	P _{out}	Z _L = 4Ω + 33μH	VDDSPK = 5.0V	2.9	W
		THD + N = 10%	VDDSPK = 3.7V	1.53	
		Z _L = 4Ω + 33μH	VDDSPK = 5.0V	2.35	
		THD + N = 1%	VDDSPK = 3.7V	1.26	
		Z _L = 8Ω + 68μH	VDDSPK = 5.0V	1.71	
		THD + N = 10%	VDDSPK = 3.7V	0.92	
		Z _L = 8Ω + 68μH	VDDSPK = 5.0V	1.38	
		THD + N = 1%	VDDSPK = 3.7V	0.74	

Table 25: Class D Speaker Driver Output Power

Application Notes:

- The Class D driver can accept inputs from AUX or DAC paths.

9.1.1 Differential Mixer

The Stereo Class D amplifier uses a differential mixer to split the Output channel 0 and 1 digital signals into two differential audio outputs. The gain for each of the inputs to this mixer can be set with

[CLASSD_GAIN_1.CLASSDGAIN1L_REG0X6D\[4:0\]](#), [CLASSD_GAIN_1.CLASSDGAIN1R_REG0X6D\[12:8\]](#), [CLASSD_GAIN_2.CLASSDGAIN2L_REG0X6E\[4:0\]](#), and

[CLASSD_GAIN_2.CLASSDGAIN2R_REG0X6E\[12:8\]](#). The figure below shows how to use these registers to select the desired output levels.

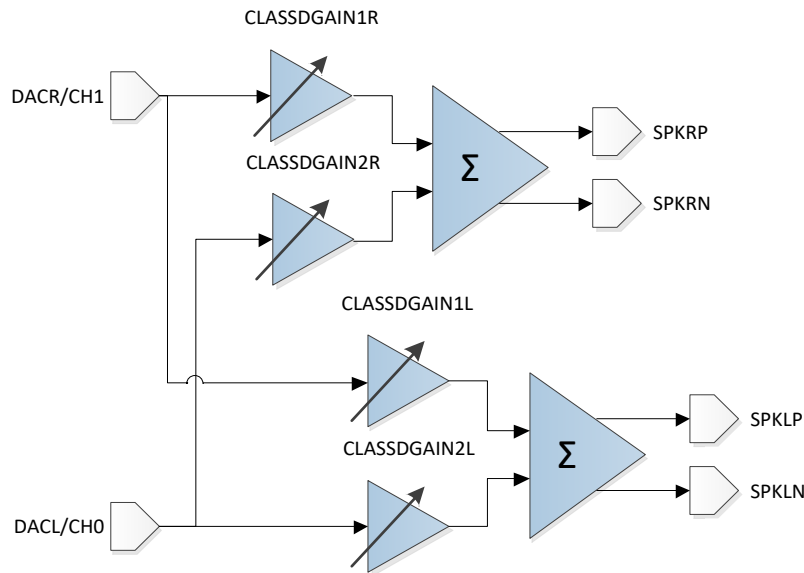


Figure 30: Class D Differential Mixer

9.1.2 Device Protection

The NAU88L24 includes device protection for the Class D outputs for three operating scenarios

1. Thermal Overload
2. Short circuit protection (It is also featured with NAU88L24 Class G.)
3. Supply under voltage

9.1.2.1 Thermal Overload Protection

When the device internal junction temperature reaches 130°C, the NAU88L24 will disable the output drivers. Once the device cools down to a safe operating temperature (115°C) for at least 47ms, the output drivers will be re-enabled.

9.1.2.2 Short Circuit Protection

If a short circuit is detected on any of the pull-up or pull-down devices on the output drivers for at least 14μs, the output drivers will be disabled for 47ms. The output drivers will then be re-enabled and checked for a short circuit again. If the short circuit is still present for another 14μs, the cycle will repeat until the short circuit has been fixed. The short circuit threshold is set at 2.1A.

9.1.2.3 Supply Under-Voltage Protection

If the V_{DDSPK} drops under 2.1V, the output drivers are disabled, however, the NAU88L24 control circuitry will still operate. This is useful to help avoid the battery supply voltage dropping before the host processor can safely shutdown the devices on the system. If the V_{DDSPK} drops below 1.0V, the internal power-on-reset will activate and put the class-D driver in power down state

9.1.3 Class D without filter

The NAU88L24 is designed for use without any filter circuits on the Class D output line so they can be connected directly to a speaker. This type of filter-less design is suitable for portable applications where the speaker is very close to the amplifier. The following figure shows how this can be done.

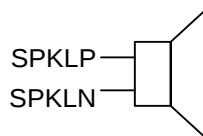


Figure 31: Speaker Outputs Connected to Speaker without Filter Circuit

9.1.4 Class D Filters

In some applications, the short trace lengths are not possible because of speaker size limitations or other design considerations. In these applications, the long traces will cause EMI issues. To reduce the EMI issues, typical filters like ferrite bead and LC can be used.

9.1.4.1 Ferrite Bead Filter

Ferrite bead filters can be used to reduce the high frequency emissions. The typical circuit diagram is shown in the figure below.

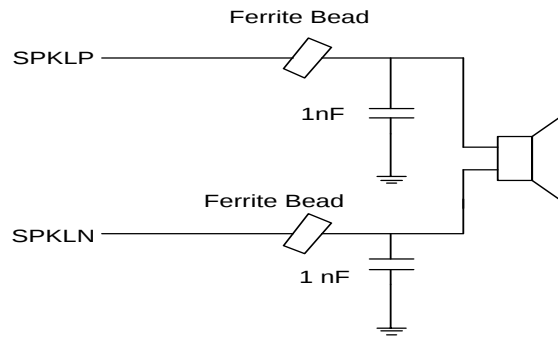


Figure 32: Speaker Outputs Connected to Speaker with Ferrite Bead Filters

These ferrite bead filters offer high impedance at high frequencies so that it will function as a low pass filter around the desired audio range.

9.1.4.2 LC filter

LC filters can be used to suppress the high frequency emissions. The typical circuit diagram is show in the figure below.

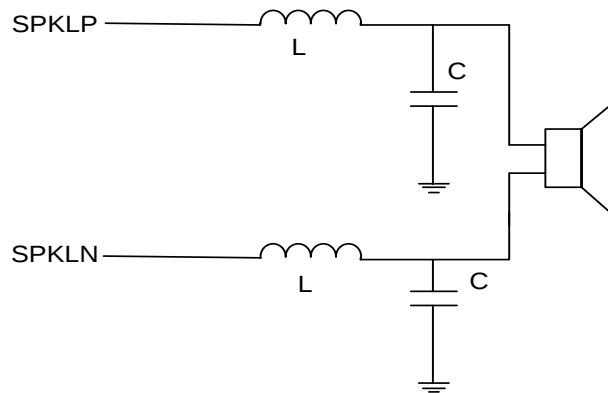


Figure 33: Speaker Outputs Connected to Speaker with LC Filter

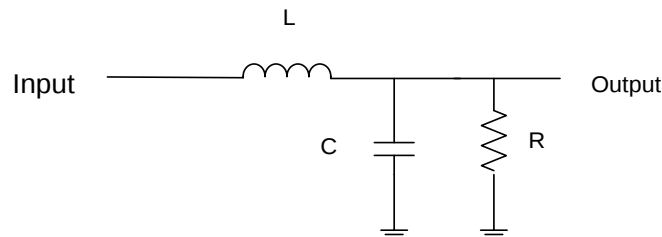


Figure 34: Standard Low Pass LCR filter

Using the standard LCR filter mode, the following are the equations for the critically damped ($\zeta = 0.707$) low pass LCR filter. To determine the LC values for the speaker filter, use the same LC values calculated for standard LCR LPF. For the resistance values in the standard model, use R_L (Speaker coil resistance) = $2R$ (LCR LPF resistance).

$$2\pi f_c = \frac{1}{\sqrt{LC}} \quad f_c \text{ is the cutoff frequency}$$

$$\zeta = 0.707 = \frac{1}{2R} * \sqrt{\frac{L}{C}}$$

9.1.5 NAU88L24 EMI performance

The NAU88L24 includes a spread spectrum oscillator to reduce EMI. This PWM oscillator frequency typically sweeps in a range of 300 kHz +/- 15 kHz in order to spread the energy of the PWM pulses over a larger frequency band. In addition, slew rate control on the output drivers allows the application of 'filter less' loads, while suppressing EMI at high frequencies.

9.2 Class G Headphone Driver and Charge Pump

The NAU88L24 uses Class G speaker drivers powered by a charge pump for the headphones. For typical operation with large and small signals the charge pump provides $\pm 1.8V$ and $\pm 0.9V$, respectively. These output drivers are driven by dedicated left and right DACs and can provide 30mW of power to a 32 Ω load. To enable the Class G driver and the charge pump, use [CLASSG.CLASSG_EN REG0X50\[0\]](#) and [CHARGE PUMP AND POWER DOWN CONTROL.RINN REG0X80\[5\]](#), respectively.

Application Notes:

- Three capacitors are needed to generate the negative voltage from the positive 1.8V. Typically, 2 μF ceramic capacitors are used.
- o The Fly Back capacitor is connected between pins CPCA and CPCB.
- o The Positive Output Decoupling capacitor is applied from pin CPVOUTP to ground (VSSCP).
- o The Negative Output Decoupling capacitor is applied from pin CPOUTN to ground (VSSCP).
- [CLASSG.CLASSG_CMP_EN REG0X50\[2:1\]](#) sets which DAC signals to monitor. All low is default, which gives the low voltage output. This is used for when the headphones have attenuated signals.
- [CLASSG.CLASSG_THRSLD REG0X50\[5:4\]](#) sets the threshold from 1/16 to 1/4 Full Scale.
- [CHARGE PUMP AND POWER DOWN CONTROL.SHCIRSEL1 REG0X80\[0\]](#) and [CHARGE PUMP AND POWER DOWN CONTROL.SHCIRSEL2 REG0X80\[1\]](#) select the short circuit setting for the high voltage charge up. When set at default, the protection mode is set for 1.7V and VDD can provide up to 150mA. When both are enabled, the protection mode is set to 1.4V and VDD can supply 500mA. Refer to the table below for setting values.
- [HS_VOLUME_CONTROL.MUTE_HSPGA2 REG0X75\[13\]](#) and [HS_VOLUME_CONTROL.MUTE_HSPGA1 REG0X75\[6\]](#) can be used to mute each of the headset channels.
- [ATT_PORT0.ATT0HSR REG0X7B\[12:8\]](#) and [ATT_PORT1.ATT1HSR REG0X7C\[12:8\]](#) control the gain for the Right headset output. [ENABLE_LO.ENHSR REG0X6B\[3:2\]](#) needs to enable coordinately.
- [ATT_PORT0.ATT0HSL REG0X7B\[4:0\]](#) and [ATT_PORT1.ATT1HSL REG0X7C\[4:0\]](#) control the gain for the Left headset output. [ENABLE_LO.ENHSL REG0X6B\[1:0\]](#) needs to enable coordinately.
- [CHARGE PUMP INPUT READ REG0X81](#) is read only and shows the various statuses of the charge pump's current running conditions. See the register map for more detail.
- To enable CPVDD = 0.9V for small signals
- o Set [CLASSG.CLASSG_CMP_EN REG0X50\[1\]](#) = 1'b0
- o Set [CLASSG.CLASSG_EN REG0X50\[0\]](#) = 1'b0 to force ClassG Mode 0
- To enable CPVDD = 1.8V for full scale signals
- o Set [CLASSG.CLASSG_CMP_EN REG0X50\[1\]](#) = 1'b1
- o Set [CLASSG.CLASSG_EN REG0X50\[0\]](#) = 1'b0 to force ClassG Mode 1

SHCIRSEL2	SHCIRSEL1	Short Circuit Select voltage
0	0	1.7 volts
0	1	1.6 volts
1	0	1.5 volts
1	1	1.4 volts

Table 26: Charge Pump Short Circuit Settings

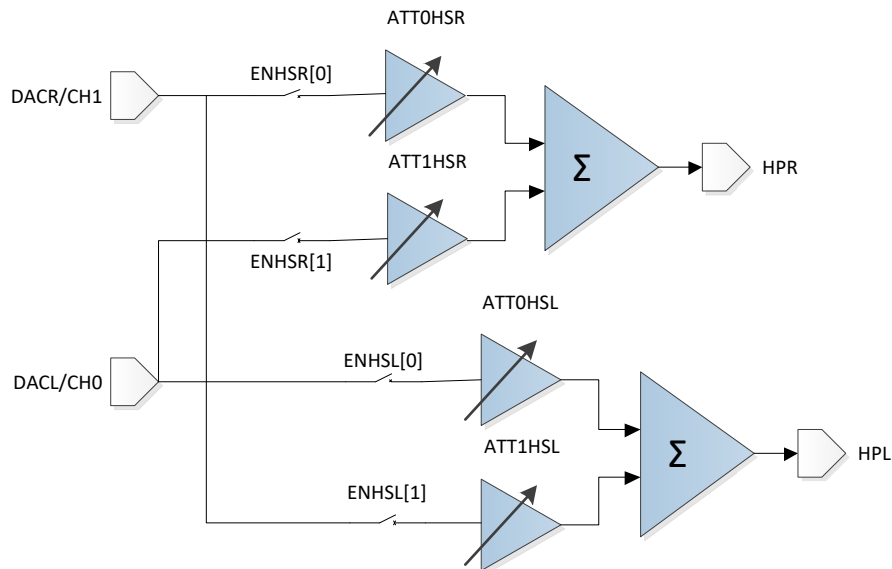


Figure 35: DAC to Headphone out path diagram

10 Headset Detection

The NAU88L24 includes an extensive set of detection features to support various types of headsets for global compatibility.

1. Headset jack insertion detection:
2. This feature detects when a headset is inserted into the external headset jack. Headset jack ejection detection:
 - This feature detects when a headset is ejected from the external headset jack.
3. Headset Microphone detection:
 - This feature detects the presence of headset microphone.
4. Headset Key detection:
 - This feature allows software programmable support for user defined actions such as play, record, and accept call. This supports up to eight distinct input levels and one key release level can be detected at the microphone pin. It also supports Long and Short button press detection and each key can activate an interrupt on the IRQ pin.

Each sequence associated with these detection mechanisms can be executed manually by the host processor or sequenced automatically, depending on the settings in the headset support execution register settings.

10.1 Jack Detection

This feature detects when a headset is inserted into or ejected from the external headset jack using the JKDET pin to detect a voltage at this pin to trigger sequences associated with headset support.

Application Notes:

- **JACK_DET.JKDET_PL REG0X0D[1]** sets the Jack Insertion status polarity.
- The Jack Insertion de-bounce time is 1ms.
- **JACK_DET_CTRL.EJECT_DT REG0X0D[3:2]** sets the Jack Ejection de-bounce time.
- **JACK_DET_CTRL.JKDET_LOGIC REG0X0D[0]** can change the detection logic from OR to AND.
- **ENA_CTRL.SLEEP4JACK REG0X01[10]** allows the Jack Detect to bypass the de-bounce filter in order to go straight to the IRQ pin without clock. **INTERRUPT_SETTING_1.JK_EJECT_INTP_MASK REG0XF[9]** or **INTERRUPT_SETTING_1.JK_DET_INTP_MASK REG0XF[8]** need to be enabled.

- It is recommended that the host checks for the IRQ to be consistently valid within 10ms in order to avoid false detection due to glitches. Once the host validates the jack detect, the host needs to initiate the power up sequence and headset support sequences.

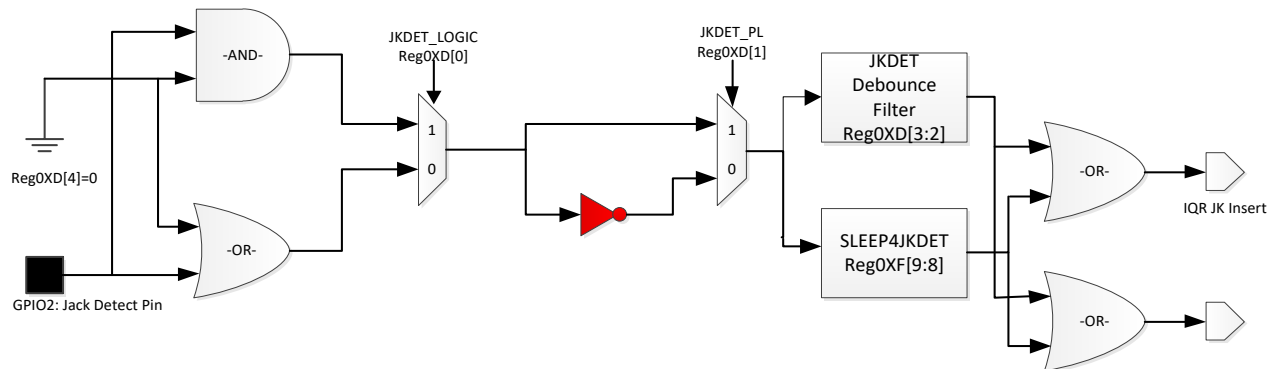


Figure 36: Jack Detection

10.2 Microphone Detection

This feature detects the presence of a microphone. Using an internal SAR ADC, the presence of a microphone can be detected by measuring the DC voltage on the microphone pin after jack insertion. Without jack insertion, jack detection is not valid, and **SARADC_DOUT** reads 0xFF value. When microphone presents after jack insertion, jack detection is valid, and **SAR_ADC_DATA_OUT.SARADC_DOUT** has a value between 0xFF and 0x00. If the jack doesn't have microphone, the value is equal to 0x00.

10.3 Key/Button Detection

This feature allows software programmable support of user defined actions such as play, record, and accept call. This feature supports up to eight distinct input levels (keys) to be detected at the microphone pin and a long key press and short key press can activate an interrupt on the IRQ pin. The block diagram below shows how the headset buttons are detected.

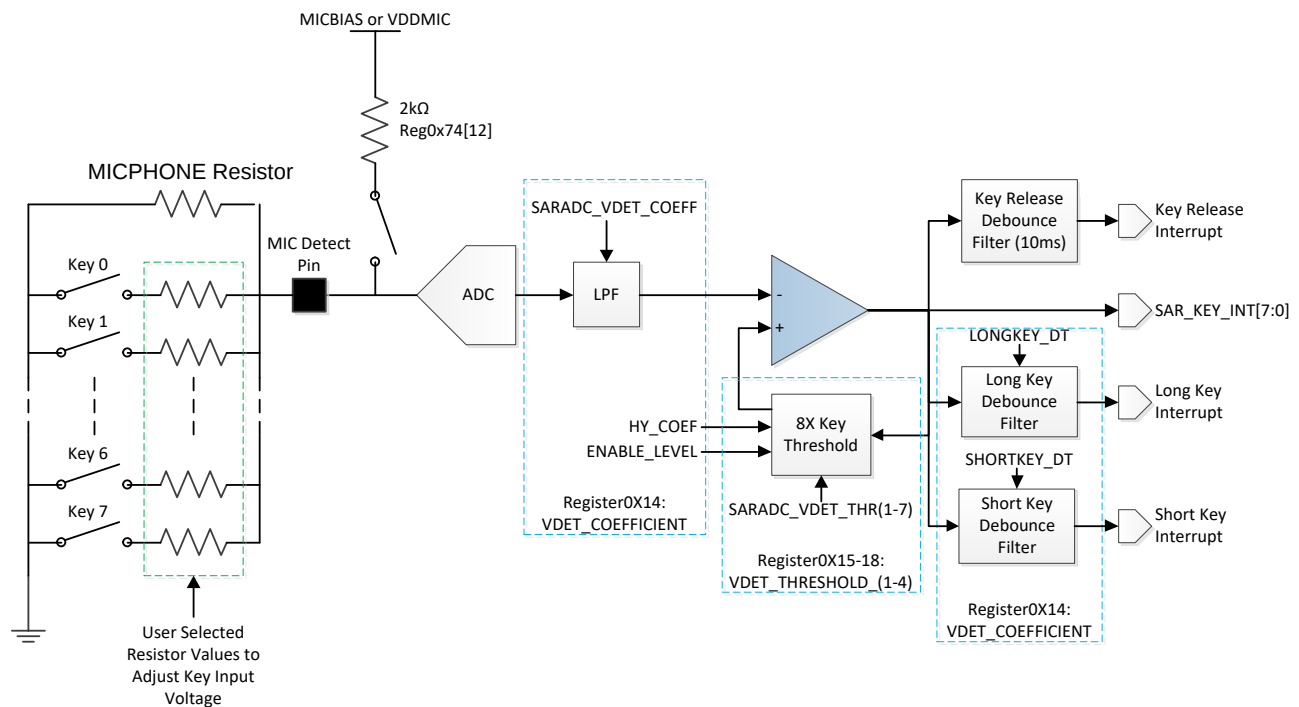


Figure 37: Key Detection

Each of these output signals from the eight comparators go through three de-bounce filters not shown in the block diagram. After each of press key signals are received through the de-bounce filters, the associated interrupts are triggered and can be read from **INTERRUPT_SETTING REG0X11**. The table below shows the options for changing the long and short key de-bounce filter times.

VDET_COEFFICIENT.LONGKEY_DT REG0X14[7]	Long Key De-bounce Time
0	500ms
1	1 sec
VDET_COEFFICIENT.SHORTKEY_DT REG0X14[4]	Short Key De-bounce Time
00	30ms
01	40ms
10	100ms
11	x

Table 27: Key De-bounce Time Setting

The DC level changes at the MIC input pin are converted into a digital representation through a SAR ADC and the decimal value of **SAR_ADC_DATA_OUT.SARADC_DOUT REG0X59[7:0]** can be determined with the equation below. The different reference voltage levels are derived from the VDDA voltage supply. If the headset Microphone bias voltage is tied to the MICBIAS pin, then the SAR ADC digital output signal decimal representation can be described as:

$$SAR\ ADC = 255 \times Amb \times Asar \times Rp / (Rmb + Rp)$$

- Amb is the MIC bias factor given by **MIC_BIAS.MICBIASLVL1 REG0X74[2:0]**
- Asar is the gain of the SAR ADC, which is $1/(VDDA \times \text{SAR_ADC.SAR_TRACKGAIN REG0X13[10:8]})$
- Rmb is the MIC bias series resistor, which is typically 2kΩ .
- Rp is the parallel resistance of the Microphone and the resistance of the button that is pressed.

The SAR ADC output is filtered by a programmable low pass filter allowing glitches and audio content to be removed from the ADC output data. The result can be read at any time through the I2C register at **SAR_ADC_DATA_OUT.SARADC_DOUT REG0X59[7:0]**. The equation of the digital low pass filter is as following:

$$Yn = \alpha Xn + (1 - \alpha)Yn - 1$$

- α is the coefficient of the low pass filter, $\alpha=(1/2)^n$
- n is controlled by **VDET_COEFFICIENT.SARADC_VDET_COEFF REG0X14[7:4]**.

The SAR ADC output signal is fed into 8 comparators with each a unique programmable threshold level and common high and low hysteresis levels. These 8 comparators will generate 8 distinct output signals as determined by the threshold levels and external DC voltage at the Microphone pin.

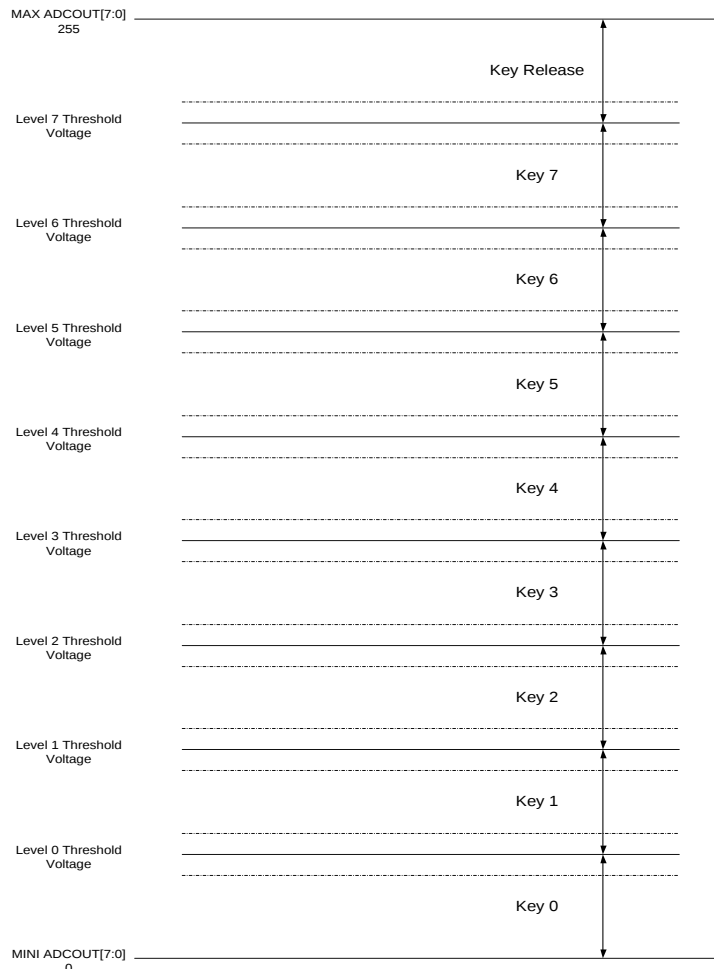


Figure 38: Keys Region

The figure above shows the eight threshold voltages and nine different Key regions. The lowest SARADC output range indicates when Key 0 is pressed, the second when Key 1 is pressed, and so on. The highest region indicates when no key has been pressed.

Example:

- 1) A headphone has three buttons. MICBIAS voltage is set to $1.53 \times VDDA$ at $VDDA=1.8V$ by **MIC_BIAS.MICBIASLVL1** and **SAR_TRACKGAIN** set according to **Table 29**. Microphone resistance is 10k Ohm. If no button is pressed, the **SARADC_DOUT** decimal output is:

$$\text{SARADC_DOUT} = 255 \times 1.53 \times 1.8 \times 1 / (1.53 \times 1.8) \times 10k / (2k + 10k) = 212$$
- 2) When a button with 4k Ohm series resistance is pressed, the **SARADC_DOUT** output becomes:

$$\text{SARADC_DOUT} = 255 \times 1.53 \times 1.8 \times 1 / (1.53 \times 1.8) \times 10k / (4k / (2k + 10k / 4k)) = 150$$
- 3) When the second button with 2k Ohm series resistance is pressed, the **SARADC_DOUT** output becomes:

$$\text{SARADC_DOUT} = 255 \times 1.53 \times 1.8 \times 1 / (1.53 \times 1.8) \times 10k / (2k / (2k + 10k / 2k)) = 116$$
- 4) The last button with 1k Ohm series resistance is pressed, the **SARADC_DOUT** output becomes:

$$\text{SARADC_DOUT} = 255 \times 1.53 \times 1.8 \times 1 / (1.53 \times 1.8) \times 10k / (1k / (2k + 10k / 1k)) = 80$$
- 5) According to Figure 35, three threshold voltage levels for Key2 level could be set by **ENABLE_LEVEL=010**. First threshold voltage could be 98, the middle of 116 and 80 from 3) and 4). Hysteresis value can be set to 15, less than 50% of difference 116 and 80.
SARADC_VDET_THR0=98=8'b01100010,
HY_COEFF[3:0]=15=4'b1111
- 6) The second threshold voltage could be 133, the middle of 150 and 116 from 2) and 3). Hysteresis value can

be set to 15, less than 50% of difference 150 and 116.

SARADC_VDET_THR1=133=8'b10000101,

HY_COEFF[3:0]=15=4'b1111

- 7) The third threshold voltage could be 181, the middle of 150 and 212 from 1) and 2). Hysteresis value can be set to 15, less than 50% of difference 116 and 212.

SARADC_VDET_THR2=150=8'b10010110

HY_COEFF[3:0]=15=4'b1111

Combining 5), 6), and 7), a single HY_COEFF[3:0]=15=4'b1111

Application Notes:

- **VDET_COEFFICIENT.HY_COEFF_REG0X14[3:0]** can be used to change the hysteresis range. The SARADC voltage needs to be lower than the hysteresis range to go into the lower level Key. On the other hand, voltage needs to be higher than the hysteresis range to go into a higher level key. This is shown by the dashed lines in Figure 35. If the voltage sampled is in the hysteresis range, the level needs to be compared to the previous state. For example, if the previous stat is Key 2 and the new sample is in the Key 1 hysteresis range, the logic will claim the status is still Key 2.
- **VDET_COEFFICIENT.ENABLE_LEVEL_REG0X14[10:8]** selects the number of keys being used. This means that if **ENABLE_LEVEL_REG0X14[10:8]** is set to 3'b010, only three keys, Key0, Key1, and Key2, will be supported. Threshold voltages are needed to set up to SARADC_VDET_THR2. Any voltage sampled above the level 2 threshold will be considered as Key Release.

10.3.1 SAR ADC

The SAR ADC is a simple ADC used to detect the voltage level on the MIC input pin to determine which of the 8 Keys have been pressed.

Once the SAR ADC has been enabled using **SAR_ADC.SAR_ENA_REG0X13[12]**, the SAR ADC enters a sampling phase. During this phase, the voltage level on the MIC input is sampled at a speed determined by **SAR_ADC.SAMPLE_SPEED_REG0X13[1:0]**. This time can be adjusted from 2μs to 16μs, doubling each step. During the sampling phase, the sample signal will be high together with the MSB and low with the LSB. It should be noted that the maximum input current of the ADC can be reduced by selecting a bigger input resistor in series with the sampling capacitor. The value of the input resistor can track the sampling time.

SAR_ADC.RES_SEL REG0X13[6:4]	Resistor value [Ohm]
000	35k
001	70k
010	170k
011	360k
1xx	short

Table 28: SAR ADC Current Limit Resistor Selection

After the sampling phase, the ADC enters a conversion phase that consists of eight compare cycles. Each of these compare cycles can last from 500ns to 4μs, doubling each step. To adjust the compare time use **SAR_ADC.COMP_SPEED_REG0X13[3:2]**.

It should be noted that **SAR_ADC.HV_SEL_REG0X13[7]** can be used to set the voltage of the 5V PMOS in the track & hold part of the ADC. Setting this register makes the back gate voltage equal to MICBAIS (0) or MICVDD (1). It is also important to set the gain setting in **SAR_ADC.SAR_TRACKGAIN_REG0X13[10:8]**. Because the output of MICBIAS is adjustable, the input voltage range of the ADC has to track the output voltage of MICBIAS. The table below shows how to set this register.

MIC_BIAS.MICBIASLVL1 REG0X74[2:0]	MICBIAS Level	SAR_TRACKGAIN REG0X13[10:8]
000	1.0*VDDA	000
001	1.0*VDDA	001
010	1.1*VDDA	010
011	1.2*VDDA	011
100	1.3*VDDA	100
101	1.4*VDDA	101
110	1.53*VDDA	110
111	1.53*VDDA	111

Table 29: SAR ADC MICBIAS Gain Tracking Settings

10.4 Jack Interrupt Sequence

The NAU88L24 includes an interrupt sequence feature that can detect various types of interrupts and trigger associated sequences. This system works by continually waiting for an interrupt to occur. Once an interrupt occurs, the x10 register is read to determine the type of interrupt while the x11 register is reset to prepare for further interrupts.

10.4.1 Jack Insert

This feature detects when a headset is inserted into the external headset jack interrupt and clears the x11 register to reset for further interrupts. The impedance measurement mode is setup to read the impedance of the headset and the successive approximation register is read to determine whether or not both the headphone and microphone need to be enabled. It then resumes waiting for further interrupts.

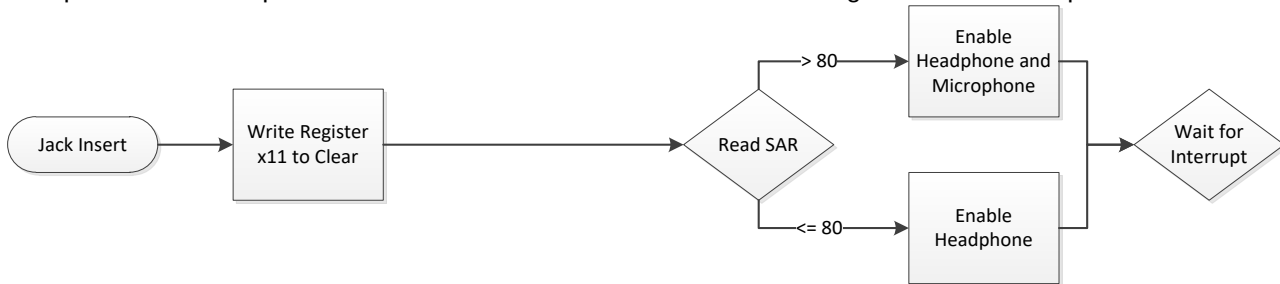


Figure 37: Jack Insert Flowchart

10.4.2 Jack Eject

This feature detects when a headset is ejected from the external headset jack interrupt and clears the x11 register to reset for further interrupts. The headphone and microphone are disabled accordingly and it resumes waiting for further interrupts.

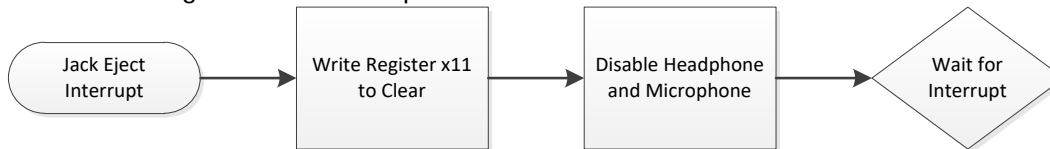


Figure 38: Jack Eject Flowchart

10.4.3 Short Key Press

This feature detects the software programmable user defined actions as short or long key press interrupts and clears the x11 register to reset for further interrupts after reading the key. The feature then waits for a second interrupt and clears the x11 register to reset for further interrupts and reads the x10 register to determine the type of key press. The associated sequence is then triggered and it resumes waiting for further interrupts.

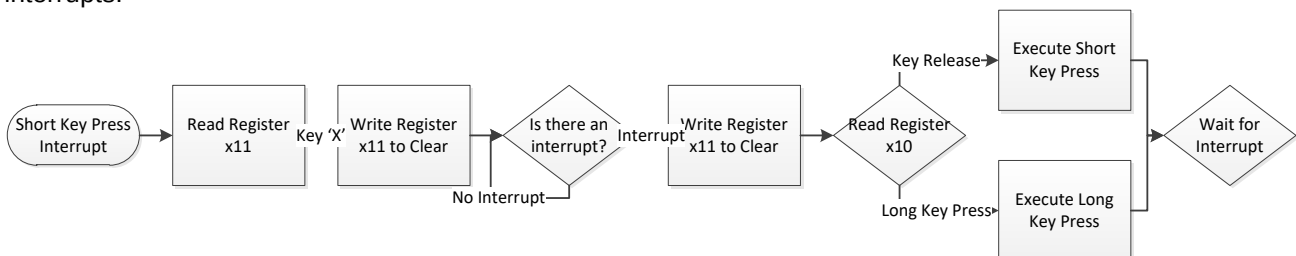


Figure 39: Short Key Press Flowchart

10.4.4 Key Release

This feature detects the edge case where the key press interrupt is not followed by a release interrupt until later on in the sequence and clears the x11 register to prepare for further interrupts.



Figure 40: Key Release Flowchart

11 Basic Register Sequences

The following register sequences are general guides to help setup the NAU88L24.

11.1 To enable V_{REF} and General Bias

1. Reset all registers by writing anything to register 0x00 twice
2. Set GPIO_SEL_REG0X1A[6]=1
3. Enable V_{REF} in high impedance mode by setting BIAS_ADJ.VMIDEN_REG0X66[6] = 1 and BIAS_ADJ.VMIDSEL_REG0X66[5:4] = 10
4. Wait for 2ms
5. Set BOOST.BIASEN_REG0X76[12] = 1
6. Set BOOST.PDVMDFAST_REG0X76[13] = 1
7. The chip is now ready to enable analog block functions.

11.2 Enable/Disable Input PGA

To Enable

1. Set PGA_GAIN.MUTEL_REG0X67[14] and PGA_GAIN.MUTER_REG0X67[6] = 1
2. Set POWER_UP_CONTROL.PUPR_REG0X7F[12] and POWER_UP_CONTROL.PUPR_REG0X7F[13] = 1
3. Select the input using FEPGA.FEPGA_MODEL_REG0X77[3:0] and FEPGA.FEPGA_MODER_REG0X77[7:4]
4. Set FEPGA_II.ACDC_CTRL_REG0X78[15:10] to the inputs used
5. Set BOOST.DISCHRG_REG0X76[11] = 1
6. Wait 1ms
7. Set BOOST.DISCHRG_REG0X76[11] = 0
8. Set FEPGA_II.ACDC_CTRL_REG0X78[15:10] = 0
9. Set FEPGA_ATTENUATION.FEPGA_ATTNL_REG0X7A[4:0], FEPGA_ATTENUATION.FEPGA_ATTNR_REG0X7A[12:8], FEPGA_II.FEPGA_GAINL_REG0X78[4:0], and FEPGA_II.FEPGA_GAINL_REG0X78[9:5]
10. Wait 10ms (or more depending on pop)
11. Set PGA_GAIN.MUTEL_REG0X67[13] and PGA_GAIN.MUTER_REG0X67[6] = 0

To Disable

12. Set PGA_GAIN.MUTEL_REG0X67[13] and PGA_GAIN.MUTER_REG0X67[6] = 1
13. Set POWER_UP_CONTROL.PUPR_REG0X7F[12] and POWER_UP_CONTROL.PUPR_REG0X7F[13] = 0

11.3 Enable analog ADC

1. Set ANALOG_ADC_2.PDNOTR_REG0X72[7] and ANALOG_ADC_2.PDNOTL_REG0X72[6] = 1
2. Set ANALOG_ADC_2.LFSRRESETN_REG0X72[5] = 0
3. Set ANALOG_ADC_2.LFSRRESETN_REG0X72[5] = 1 on next I2C command

11.4 Enable/Disable FLL

- It is assumed that V_{REF} , boost.BIASEN_REG0X76[12], and System Master Clock are running

To Enable

1. Set FLL_DCO_RSV.DCO_EN_REG0X09[15] = 0
2. Set FLL1.SYSCLK_SRC_REG0X03[15] = 0
3. Program the remaining FLL registers from FLL2_REG0X04 through FLL_DCO_RSV_REG0X09
4. Set FLL1.SYSCLK_SRC_REG0X03[15] = 1

To Disable

1. Set FLL_DCO_RSV.DCO_EN REG0X09[15] = 0
2. Set FLL1.SYSCLK_SRC REG0X03[15] = 0

To Enable Free Running Mode

1. Set FLL_DCO_RSV.DCO_EN REG0X09[15] = 0
2. Set FLL1.SYSCLK_SRC REG0X03[15] = 0
3. Set FLL_DCO_RSV.DCO_EN REG0X09[15] = 1
4. Set FLL1.SYSCLK_SRC REG0X03[15] = 1

To Enable Free Running Mode with Reference Clock

1. Set FLL_DCO_RSV.DCO_EN REG0X09[15] = 0
2. Set FLL1.SYSCLK_SRC REG0X03[15] = 0
3. Program the remaining FLL registers from FLL2 REG0X04 through FLL_DCO_RSV REG0X09
4. Set FLL1.SYSCLK_SRC REG0X03[15] = 1
5. Wait for the FLL to lock by monitoring the CSB pin
6. Disable/Remove reference clock

11.5 Enable/Disable DAC

To Enable

1. Setup the I2S to DAC paths
2. Set RDAC.CLK_DAC_EN REG0X73[9:8] = 11
3. Set RDAC.DACVREFSELLO REG0X73[3:2] = 10
4. Set RDAC.DAC_EN REG0X73[13:12] = 11
5. Set CHARGE PUMP AND POWER DOWN CONTROL.PD_DAC REG0X80[9:8] = 00

To Disable

1. Set RDAC.CLK_DAC_EN REG0X73[9:8] = 00
2. Set RDAC.DACVREFSELLO REG0X73[3:2] = 00
3. Set RDAC.DAC_EN REG0X73[13:12] = 00
4. Set CHARGE PUMP AND POWER DOWN CONTROL.PD_DAC REG0X80[9:8] = 11
5. Disable the I2S to DAC3 and DAC4 paths

11.6 Enable/Disable Class D Driver

- It is assumed that V_{REF}, BOOST.BIASEN REG0X76[12], System Master Clock, and the DAC are running

To Enable

6. Select an input by setting CLASSD_GAIN_2.CLASSDGAIN2L REG0X6E[4:0] and CLASSD_GAIN_1.CLASSDGAIN1R REG0X6D[12:8] = 0dB
7. Set ANALOG_CONTROL_2.ANALOG_CONTROL2 REG0X6A[3] = 1
8. Set CLASSD_GAIN_1.ENCLASSD REG0X6D[7] = 1
9. Ramp CLASSD_GAIN_2.CLASSDGAIN2L REG0X6E[4:0] and CLASSD_GAIN_1.CLASSDGAIN1R REG0X6D[12:8] to 12dB in 120ms by incrementing the gain by 1dB every 10ms

To Disable

6. Ramp CLASSD_GAIN_2.CLASSDGAIN2L REG0X6E[4:0] and CLASSD_GAIN_1.CLASSDGAIN1R REG0X6D[12:8] from 12dB to 0dB in 120ms by decrementing the gain by 1dB every 10ms
7. Set CLASSD_GAIN_1.ENCLASSD REG0X6D[7] = 0

11.7 Enable/Disable Headphone

- It is assumed that V_{REF}, BOOST.BIASEN REG0X76[12], System Master Clock, and the DAC are running

To Enable

1. Set CHARGE PUMP AND POWER DOWN CONTROL.RNIN REG0X80[5] = 1 (Charge pump on.)
2. Set CHARGE PUMP AND POWER DOWN CONTROL.PULL_SPKR_DWN REG0X80[13:12] = 11 (HS R&L speaker power down.)
3. Set ENABLE_LO.TESTDAC REG0X6B[15:14] = 11 (Force HS R&L DAC 0.)

4. Set ATT_PORT0.ATT0HSL REG0X7B[4:0] and ATT_PORT0.ATT0HSR REG0X7B[12:8] = -30dB (Adjust RDAC and LDAC HS attenuation to -30dB)
5. Set ENABLE_LO.ENHSL REG0X6B[1:0] and ENABLE_LO.ENHSR REG0X6B[3:2] = 01(enable DAC right to right headphone output, DAC left input to left headphone output.)
6. Set BOOST.NAMP_THRSHLD REG0X76[1:0] and BOOST.PAMP_THRSHLD REG0X76[3:2] = 11 (adjust HS boost p/n driver current; 11 for minimum current.)
7. Set TRIM_SETTINGS.DRV_IBCTRHS REG0X68[15] = 1 (enable HS current trim.)
8. Set POWER_UP_CONTROL.PUP_DRV_INSTG REG0X7F[3:2] = 11 (power up output driver.)
9. Set POWER_UP_CONTROL.PUP_MAIN_DRV REG0X7F[1:0] = 11 on next I2C command (Power up main driver.)
10. Set CHARGE_PUMP_AND_POWER_DOWN_CONTROL.PULL_SPKR_DWN REG0X80[13:12] = 00 on next I2C command (HS R&L speaker power up.)
11. Set ENABLE_LO.TESTDAC REG0X6B[15:14] = 00 on next I2C command. (HS R&L DAC power up.)
12. ATT_PORT0.ATT0HSL REG0X7B[4:0] and ATT_PORT0.ATT0HSR REG0X7B[12:8] to 0dB in 300ms by incrementing the gain 1dB every 10ms

To Disable

1. Ramp ATT_PORT0.ATT0HSL REG0X7B[4:0] and ATT_PORT0.ATT0HSR REG0X7B[12:8] from 0dB to -30dB in 300ms by decrementing the gain 1dB every 10ms
 2. Set ENABLE_LO.TESTDAC REG0X6B[15:14] = 11 on next I2C command
 3. Set POWER_UP_CONTROL.PUP_MAIN_DRV REG0X7F[1:0] = 00 and CHARGE_PUMP_AND_POWER_DOWN_CONTROL.PULL_SPKR_DWN REG0X80[13:12] = 11 on next I2C command
 4. SET POWER_UP_CONTROL.PUP_DRV_INSTG REG0X7F[3:2] = 00 on next I2C command
- The disable sequence is only necessary when a headset is connected. If the headset is disconnected, everything can be powered down at once.

11.8 Enable DAC to Headphone Low Power MP3 Playback Mode

- It is assumed that the DAC to headphone path is running and the System Clock is running. VDDC needs to be set to 1.2V for lowest power, FS = 44.1kHz, 16 bits

1. Set TRIM_SETTINGS.DRV_IBCTRHS REG0X68[15] = 0
2. Set TRIM_SETTINGS.DRV_ICUTHS REG0X68[14] = 1
3. Set BOOST.BOOSTDIS REG0X76[8] = 1
4. Set RDAC.DACVREFSELLO REG0X73[3:2] = 00
5. Set BIAS_ADJ.BIASADJ REG0X66[1:0] = 10
6. Set DAC_FILTER_CTRL_1.DAC_RATE REG0X25[2:0] = 100
7. Set FLL1.CLK_DAC_SRC REG0X03[5:4] = 11
8. Set DAC_FILTER_CTRL_1.DISABLE_DEM REG0X25[15] = 1

11.9 Enable DAC to Class D Low Power MP3 Playback Mode

- It is assumed that the DAC to headphone path is running and the System Clock is running. VDDC needs to be set to 1.2V and VDDSPK needs to be set to 2.5V for lowest power, FS = 44.1kHz, 16 bits

1. Set RDAC.DACVREFSELLO REG0X73[3:2] = 00
2. Set BIAS_ADJ.BIASADJ REG0X66[1:0] = 10
3. Set DAC_FILTER_CTRL_1.DAC_RATE REG0X25[2:0] = 100
4. Set FLL1.CLK_DAC_SRC REG0X03[5:4] = 11
5. Set DAC_FILTER_CTRL_1.DISABLE_DEM REG0X25[15] = 1

11.10 Jack Detection

- It is assumed not in sleep mode
1. Set bias circuit by BIAS_ADJ.VMID REG0X66[6] =1 and BIAS_ADJ.VMIDSEL[1:0] REG0X66[5:4] =1, after 2mS

2. Set enable global analog bias by BOOST.BIASEN REG0X76[12] =1 and VMID pre-charge disabled by BIAS_ADJ.PVDMDFST REG0X76[13] =1
3. Set MIC bias output =VDDA by MIC_BIAS.MICBIASLVL1[2:0] REG0x74[2:0] =0, then turn on mic bias MIC_BIAS.POWERUP REG74[8]=1
4. Set jack ejection de-bounce time =10ms by JACK_DET_CTRL.EJECT_DT[1:0] REG0XD[3:2] =2;
5. Optimize SARADC by following settings; SAR_ADC.RES_SEL[2:0] REG0X13[6:4]=1;
SAR_ADC.COMP_SPEED[1:0] REG0X13[3:2]=1; SAR_ADC.SAMPLE_SPEED[1:0] REG0X13[1:0]=1
6. Enable SAR ADC clock by CLK_GATING_ENA.CLK_SAR_EN REG0x2[3]=1

12 Control and Status Registers

REG	Function
1	ENA_CTRL
2	CLK GATING ENA
3	CLK DIVIDER
4	FLL1
5	FLL2
6	FLL3
7	FLL4
8	FLL5
9	FLL6
A	FLL DCO RSV
D	JACK DET CTRL
F	INTERRUPT SETTING 1
10	IRQ STATUS
11	CLEAR INT REG
12	INTERRUPT SETTING
13	SAR_ADC
14	VDET COEFFICIENT
15	VDET THRESHOLD 1
16	VDET THRESHOLD 2
17	VDET THRESHOLD 3
18	VDET THRESHOLD 4
1A	GPIO_SEL
1C	PORT0 I2S PCM CTRL 1
1D	PORT0 I2S PCM CTRL 2
1E	PORT0 LEFT TIME SLOT
1F	PORT0 RIGHT TIME SLOT
20	TDM_CTRL
23	ADC HPF_FILTER
24	ADC FILTER CTRL
25	DAC FILTER CTRL 1
26	DAC FILTER CTRL 2
27	NOTCH FILTER 1
28	NOTCH FILTER 2
29	EQ1 LOW
2A	EQ2 EQ3
2B	EQ4 EQ5
2D	ADC CH0 DGAIN_CTRL
2E	ADC CH1 DGAIN_CTRL
2F	ADC CH2 DGAIN_CTRL
30	ADC CH3 DGAIN_CTRL
31	DAC MUTE_CTRL
32	DAC CH0 DGAIN_CTRL
33	DAC CH1 DGAIN_CTRL
34	ADC TO DAC ST
38	DRC KNEE IP12 ADC CH01
39	DRC KNEE IP34 ADC CH01
3A	DRC SLOPE ADC CH01
3B	DRC ATKDCY ADC CH01
3C	DRC KNEE IP12 ADC CH23

REG	Function
3D	DRC KNEE IP34 ADC CH23
3E	DRC SLOPE ADC CH23
3F	DRC ATKDCY ADC CH23
40	DRC GAINL ADC0
41	DRC GAINL ADC1
42	DRC GAINL ADC2
43	DRC GAINL ADC3
45	DRC KNEE IP12 DAC
46	DRC KNEE IP34 DAC
47	DRC SLOPE DAC
48	DRC ATKDCY DAC
49	DRC GAIN DAC CH0
4A	DRC GAIN DAC CH1
4C	MODE
4D	MODE1
4E	MODE2
50	CLASSG
51	OPT_EFUSE
53	OTPDOUT1
54	OTPDOUT2
55	MISC_CTRL
56	I2C TIMEOUT
57	TEST MODE
58	I2C DEVICE ID
59	SAR_ADC DATA OUT
66	BIAS_ADJ
67	PGA_GAIN
68	TRIM SETTINGS
69	ANALOG CONTROL 1
6A	ANALOG CONTROL 2
6B	ENABLE LO
6C	GAIN LO
6D	CLASSD GAIN 1
6E	CLASSD GAIN 2
71	ANALOG_ADC 1
72	ANALOG_ADC 2
73	RDAC
74	MIC_BIAS
75	HS VOLUME CONTROL
76	BOOST
77	FEPGA
78	FEPGA_II
79	FEPGA_SE
7A	FEPGA ATTENUATION
7B	ATT_PORT0
7C	ATT_PORT1
7F	POWER UP CONTROL
80	CHARGE PUMP AND POWER DOWN CONTROL
81	CHARGE PUMP INPUT READ

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	HARDWARE_RST	HARDWARE_RESET																	Hardware Reset (Write any value once to reset all the registers.)
1	ENA_CTRL	DMIC_LCH_E DGE_ADC_C H23																	DMIC Signal Phase For CH23 0 = (DEFAULT - Left on falling & Right on rising) 1 = (Left on rising & Right on falling)
		DMIC_LCH_E DGE_ADC_C H01																	DMIC Signal Phase For CH01 0 = (DEFAULT - left on falling & right on rising) 1 = (Left on rising & right on falling)
		ADC_OP_OFF																	ADC Filter Enable Control 0 = Enable (DEFAULT) 1 = Disable
		SLEEP4JACK																	Interrupt Sleep Mode For Jack Detection 0 = Jack detection without MCLK (DEFAULT) 1 = Jack detection with MCLK
		ADC_CH3_D MIC_MODE																	ADC Path CH3 DMIC Mode Enable Control 0 = Disable (DEFAULT) 1 = Enable
		ADC_CH2_D MIC_MODE																	ADC Path CH2 DMIC Mode Enable Control 0 = Disable (DEFAULT) 1 = Enable
		ADC_CH1_D MIC_MODE																	ADC Path CH1 DMIC Mode Enable Control 0 = Disable (DEFAULT) 1 = Enable
		ADC_CH0_D MIC_MODE																	ADC Path CH0 DMIC Mode Enable Control 0 = Disable (DEFAULT) 1 = Enable
		DAC_CH1_EN																	DAC Path CH1 Enable Control 0 = Disable (DEFAULT) 1 = Enable
		DAC_CH0_EN																	DAC Path CH0 Enable Control 0 = Disable (DEFAULT) 1 = Enable
		ADC_CH3_EN																	ADC Path CH3 Enable Control 0 = Disable (DEFAULT) 1 = Enable
		ADC_CH2_EN																	ADC Path CH2 Enable Control 0 = Disable (DEFAULT) 1 = Enable
		ADC_CH1_EN																	ADC Path CH1 Enable Control 0 = Disable (DEFAULT) 1 = Enable
		ADC_CH0_EN																	ADC Path CH0 Enable Control 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
2	CLK_GATING_ENA	CLK_ADC_CH 23_EN																	ADC CH23 Clock Gating Enable Control 0 = Disable (DEFAULT) 1 = Enable
		CLK_ADC_CH 01_EN																	ADC CH01 Clock Gating Enable Control 0 = Disable (DEFAULT) 1 = Enable
		CLK_DAC_CH 1_EN																	DAC CH1 Clock Gating Enable Control 0 = Disable (DEFAULT) 1 = Enable
		CLK_DAC_CH 0_EN																	DAC CH0 Clock Gating Enable Control 0 = Disable (DEFAULT) 1 = Enable
		CLK_DACHPF_EN																	DAC High Pass Filter / DAC Equalizer Clock Gating Enable Control 0 = Disable (DEFAULT) 1 = Enable
		RESERVED																	RESERVED
		CLK_DAC_PL																	DAC Clock Polarity 0 = Non-inverted (DEFAULT) 1 = Inverted

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		CLK_ADC_PL																	ADC Clock Polarity 0 = Non-inverted (DEFAULT) 1 = Inverted
		CLK_I2S_EN																	I2S Clock Gating Enable Control (For master mode) 0 = Disable (DEFAULT) 1 = Enable
		CLK_GAIN_EN																	Gain Control Clock Gating Enable Control 0 = Disable (DEFAULT) 1 = Enable
		CLK_OTP_EN																	OTP Clock Gating Enable Control (When MCLK present, HP trimmed part needs to turn it on.) 0 = Disable (DEFAULT) 1 = Enable
		CLK_SAR_EN																	SAR Clock Gating Enable Control 0 = Disable (DEFAULT) 1 = Enable
		CLK_EQ_EN																	EQ / Notch Filter Clock Gating Enable Control (Need CLK_DACHPF_EN on.) 0 = Disable (DEFAULT) 1 = Enable
		CLK_DM_EN																	DMIC Clock Gating Enable Control 0 = Disable (DEFAULT) 1 = Enable
		CLK_DRC_EN																	DRC Clock Gating Enable Control 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
3	CLK DIVIDER	SYSCLK_SRC																	Master Clock Source Select 0 = MCLK_PIN (DEFAULT) 1 = 1/2 DCO_CLK
		CLK_CODEC_SRC																	ADC & DAC Clock Source Select 0 = From internal MCLK (DEFAULT) 1 = From MCLK_PIN or 1/2 DCO_CLK
		CLK_DMIC_SRC																	Scaling Divider For DMIC Clock From MCLK 000 = 1 (DEFAULT) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 1/32
		CLK_GPIO_SRC																	Scaling Divider For GPIO Clock From MCLK 00 = 1/8 (DEFAULT) 01 = 1 10 = 1/2 11 = 1/4
		CLK_ADC_SRC																	Scaling Divider For ADC Clock From CODEC_SRC 00 = 1 (DEFAULT) 01 = 1/2 10 = 1/4 11 = 1/8
		CLK_DAC_SRC																	Scaling Divider For DAC Clock From CODEC_SRC 00 = 1 (DEFAULT) 01 = 1/2 10 = 1/4 11 = 1/8
		MCLK_SRC																	Scaling Divider For MCLK From SYSCLK_SRC 0000 = 1 (DEFAULT) 0001 = Inverted 0010 = 1/2 0011 = 1/4 0100 = 1/8 0101 = 1/16 0110 = 1/32 0111 = 1/3 1000 = 1 1001 = Inverted 1010 = 1/6 1011 = 1/12 1100 = 1/24 1101 = 1/48 1110 = 1/96 1111 = 1/5
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
4	FLL1	FLLISELDAC																	Increase Drive Strength Of FLL DAC 000 = (DEFAULT)

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		ICTRL_LATCH																	FLL Latch Drive Strength Multiplier (When FLL running at high frequency with long decimal number, DSP needs to operate at high speed. By adjusting ICTRL_LATCH, FLL DSP can optimize between performance and power consumption (111 has highest power consumption for FLL DSP.) On the other hand, (DCO frequency)/(FLL input reference frequency)=integer, default setting can be used to reduce power. This register is using thermometer coding.) 000 = (DEFAULT) 001 = 1x 011 = 2x 111 = 3x
		ICTRL_V2I																	Amp Half Bias-Current Select (Amp bias current must be reduced to 50% of its nominal value.) 00 = No power reduction (DEFAULT) 01 = Half bias current on FLL_BIAS_AMP2X 10 = Half bias current on FLL_BIAS_AMP 11 = Half current on both amps
		FLL_LOCK_BP																	Manual Force of FLL Lock Enable Control 0 = Disable (DEFAULT) 1 = Enable
		FLL_RATIO																	Input Clock Frequency Select 0000001 = For input clock frequency ≥ 512KHz 0000010 = For input clock frequency ≥ 256KHz 0000100 = For input clock frequency ≥ 128KHz 0001000 = For input clock frequency ≥ 64KHz 0010000 = For input clock frequency ≥ 32KHz 0100000 = For input clock frequency ≥ 8KHz 1000000 = For input clock frequency ≥ 4KHz
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
5	FLL2	FLL_FRAC																	FLL 16-bit Fractional Input
		DEFAULT	0	0	1	1	0	0	0	1	0	0	1	0	0	1	1	0	0x3126
6	FLL3	RESERVED																	RESERVED
		GAIN_ERR																	FLL Gain Error (The threshold is comparison between DCO and target frequency. 1111 has the most accurate DCO to target frequency. However, the gain error setting conditionally and inversely depends on FLL input reference clock rate. Higher FLL reference input frequency can only set lower gain error, such as 0000 for input reference from MCLK=12.288MHz. On the other side, if FLL reference input is from Frame sync, 48KHz, higher error gain can apply such as 1111.) 000 = x1 (DEFAULT) 001 = x2 010 = x4 011 = x8 100 = x16 101 = x32 110 = x64
		FLL_CLK_REF_SRC																	FLL Reference CLK Source Select 00 = MCLK pin (DEFAULT) 01 = MCLK pin 10 = BCLK pin 11 = FS pin
		FLL_INTEGER																	FLL 10-bit Integer Input
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0x0008
7	FLL4	RESERVED																	RESERVED
		FLL_CLK_REF_DIV_4CHK																	FLL CLK_REF Divider For Accurate Lock Detection 000 = 1 (DEFAULT) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 1/32
		FLL_CLK_REF_DIV																	FLL Pre-Scale Divider 00 = 1 (DEFAULT) 01 = 1/2 10 = 1/4 11 = 1/8

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		FLL_N2																	FLL 10-bit Integer DCO Divider For FLL Filter Clock (The value is in orders of 2. When 0x8[13]=1, it selects DCO clock as FLL filter clock. The filter clock rate needs to be less than 1Mhz. With setting proper value, filter clock can be divided down from DCO clock. For example, DCO runs at 96MHz, by setting value 0x60=96, filter clock becomes 1MHz.)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0x0010
8	FLL5	PD_DACICTRL																	FLL DAC Drive Strength Enable Control 0 = Disable 1 = Enable (DEFAULT)
		CHB_FILTER_EN																	FLL Loop Filter To Reduce FLL Output Noise Enable Control (Especially, (DCO frequency)/(FLL input reference frequency) is not an integer.) 0 = Disable 1 = Enable (DEFAULT - by REG0x09[13:12])
		CLK_FILTER_SW																	Select Filter Clock Source Select 0 = Select REFCLK (DEFAULT) 1 = Select divided DCO clock based on register FLL_N2
		FILTER_SW																	FLL Loop Filter Output Select 0 = Select accumulator output (DEFAULT) 1 = Select filter output
		FLL_LOCK_LENGTH																	Set FLL Lock-In Length (Set the time that FLL must stay within the lock-in range before lock signal goes high.)
		DEFAULT	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0xC000
9	FLL6	DCO_EN																	FLL Free-running Mode Enable Control (Need to enable 0x76[12] BIASEN) 0 = Disable (DEFAULT) 1 = Enable
		SDM_EN																	FLL Sigma-Delta Modulator Enable Control (To create decimal part of frequency, if (DCO frequency)/(FLL input reference frequency) is not a integer. If the ratio is integer, it still can be on for lower noise output but higher power consumption.) 0 = Disable 1 = Enable (DEFAULT)
		CUTOFF500																	FLL 500KHz Cut-off Frequency Enable Control (If 0x8[14]=1, it sets loop filter cutoff frequency at 600Khz. It will give the best FLL performance with the highest power consumption.) 0 = Disable 1 = Enable (DEFAULT)
		CUTOFF600																	FLL 600KHz Cut-off Frequency Enable Control (If 0x8[14]=1, it sets loop filter cutoff frequency at 600Khz. It will give a moderate FLL performance with moderate power consumption.) 0 = Disable (DEFAULT) 1 = Enable
		RESERVED																	RESERVED
		DLR																	FLL Dynamic Lock Range 0000 = (DEFAULT)
		DEFAULT	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0x6000
A	FLL_DCO_RSV	DOUT2DCO_RSV																	FLL DCO Frequency Free-running Mode
		DEFAULT	1	1	1	1	0	0	0	1	0	0	1	1	1	1	0	0	0XF13C
D	JACK_DE_T_CTRL	RESERVED																	RESERVED
		EJECT_DT																	Ejection De-bounce Time 00 = 0s (DEFAULT) 01 = 1ms 10 = 10ms

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		JKDET_PL																	Jack Insertion/ Detection Logic Polarity 0 = Falling edge (DEFAULT) 1 = Rising edge
		JKDET_LOGIC																	Jack Detection Logic Control 0 = OR gate (DEFAULT) 1 = AND gate
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
F	INTERRUPT_SETTING_1	RESERVED																	RESERVED
		JK_EJECT_INTP_MASK																	Jack Ejection Mask Flag Enable Control (Ejection IRQ in Sleep4JACK Mode) 0 = Disable (DEFAULT) 1 = Enable
		JK_DET_INTP_MASK																	Jack Insertion Mask Flag Enable Control (Insertion IRQ in Sleep4JACK Mode) 0 = Disable (DEFAULT) 1 = Enable
		ANALOG_INTP_EN																	Analog 8-bit Interrupt Signal Enable Control Bit0 = When set to 1, generates an interrupt when the left side Class-D driver is shutting down due to an over current or high temperature condition Bit1 = When set to 1, generates an interrupt when the right side Class-D driver is shutting down due to an over current or high temperature condition Bit2 = RESERVED Bit3 = RESERVED Bit4 = When set to 1, generates an interrupt as soon as a temperature alarm occurs in the Class-D drivers Bit5 = RESERVED Bit6 = RESERVED Bit7 = RESERVED
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
10	IRQ_STATUS	APR_EMERG_SHTDWN																	APR Emergency Short Circuit Shutdown IRQ Status
		RMS_INT																	Impedance Measurement Interrupt IRQ Status
		KEY_RELEASE_INT																	Key Release For Key Detection IRQ Status
		LONG_KEY_INT																	Long Key Detection IRQ Status
		SHORT_KEY_INT																	Short Key Detection IRQ Status
		RESERVED																	RESERVED
		JACK_EJCT																	Jack Ejection IRQ Status 00 = Cleared state 01 = Jack ejection detected 10 = A jack eject interrupt was cleared due to a jack insertion 11 = Undefined
		JACK_DET																	Jack insertion IRQ status 00 = Cleared state 01 = Jack insertion detected 10 = A jack insert interrupt was cleared due to a jack ejection 11 = Undefined
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	READ ONLY

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
11	CLEAR_INT_REG	CLR_REG10_INT_SIG																	Write Operation (Write bits[15:0] clear corresponding REG10 [15:0] Write 1s to bits that you want to reset to 0, except) Bit0 or Bit1 = clear Jack insertion interrupt Bit2 or Bit3 = clear Jack ejection interrupt Read Operation (REG11[7:0] - RD_SAR level, key detection status for each key) Bit 0 = Key 0 Bit 1 = Key 1 Bit 2 = Key 2 Bit 3 = Key 3 Bit 4 = Key 4 Bit 5 = Key 5 Bit 6 = Key 6 Bit 7 = Key 7
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	READ/WRITE
12	INTERRUPT_SETTING	IRQ_POLARITY																	IRQ Pin Logic Select 0 = Active low 1 = Active high (DEFAULT)
		IRQ_PS																	IRQ Pin Pull Select 0 = Pull down (DEFAULT) 1 = Pull up
		IRQ_PE																	IRQ Pin Pull Enable Control 0 = Disable (DEFAULT) 1 = Enable
		IRQ_DS																	IRQ Pin Drive Current Select 0 = Low drive current (DEFAULT) 1 = High drive current
		IRQ_OE																	IRQ Pin Output Enable Control 0 = Disable (DEFAULT) 1 = Enable
		KEY0_RELEASE_INT_DIS																	Key0 Release Interrupt Disable Control 0 = Enable (DEFAULT) 1 = Disable
		LONG_KEY0_INT_DIS																	Key0 Long Key Interrupt Disable Control 0 = Enable (DEFAULT) 1 = Disable
		SHRT_SHTDWN_INT_DIS																	APR Emergency Short Circuit Shutdown Interrupt Disable Control 0 = Enable interrupt; interrupt status read from register or IRQ pad (DEFAULT) 1 = Disable interrupt and IRQ pad
		RMS_INT_DIS																	RMS Impedance Measurement Interrupt Disable Control 0 = Enable interrupt; interrupt status read from register or IRQ pad (DEFAULT) 1 = Disable interrupt and IRQ pad
		KEY_RELEASE_INT_DIS																	Key Release Interrupt Disable Control 0 = Enable interrupt; interrupt status read from register or IRQ pad (DEFAULT) 1 = Disable interrupt and IRQ pad
		LONG_KEY_INT_DIS																	Long Key Interrupt Disable Control 0 = Enable interrupt; interrupt status read from register or IRQ pad (DEFAULT) 1 = Disable interrupt and IRQ pad
		SHORT_KEY_INT_DIS																	Long Key Interrupt Disable Control 0 = Enable interrupt; interrupt status read from register or IRQ pad (DEFAULT) 1 = Disable interrupt and IRQ pad
		MIC_DET_INT_DIS																	MIC Detection/Headset Configuration Interrupt Disable Control 0 = Enable interrupt; interrupt status read from register or IRQ pad (DEFAULT) 1 = Disable interrupt and IRQ pad
		JACK_EJECT_INT_DIS																	Jack Ejection Interrupt Disable Control 0 = Enable interrupt; interrupt status read from register or IRQ pad (DEFAULT) 1 = Disable interrupt and IRQ pad

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		JACK_DET_INT_DIS																	Jack Insertion/Detection Interrupt Disable Control 0 = Enable interrupt; interrupt status read from register or IRQ pad (DEFAULT) 1 = Disable interrupt and IRQ pad
		DEFAULT	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0x1000
13	SAR_ADC	SAR_OUT_INVERT																	SAR Inverted Output Enable Control 0 = Disable (DEFAULT) 1 = Enable
		SAR_ENA																	SAR Enable Control 0 = Disable (DEFAULT) 1 = Enable
		INPUT_SEL																	SAR Output/Input Select 0 = Output (DEFAULT) 1 = Input
		SAR_TRACK_GAIN																	Same As MIC_BIAS.MICBIASLVL1 (See SAR_ADC for more information)
		HV_SEL																	High Voltage Select 0 = Disable (DEFAULT - supply from MICBIAS) 1 = Enable (supply from VDDMIC)
		RES_SEL																	SAR Series Resistor Select 00 = 35k Ohms 001 = 70k Ohms (DEFAULT) 010 = 170k Ohms 011 = 360k Ohms 1XX = Short
		COMP_SPEED																	Compare Cycle Time Select (The total conversion has 8 compare cycles.) 00 = 500ns 01 = 1us (DEFAULT) 10 = 2us 11 = 4us
		SAMPLE_SPEED																	Sampling Phase Time Select 00 = 2us 01 = 4us (DEFAULT) 10 = 8us 11 = 16us
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0x0015
14	VDET_COEFFICIENT	RESERVED																	RESERVED
		LONGKEY_DT																	Long Key Detection De-bounce Time 0 = 500ms (DEFAULT) 1 = 1s
		SHORTKEY_DT																	Short Key Detection De-bounce Time 00 = 30ms (DEFAULT) 01 = 50ms 10 = 100ms
		RESERVED																	RESERVED
		ENABLE_LEVEL																	Enable Digital Threshold Level Control 000 = Enable until key 0 threshold level 001 = Enable until key 1 threshold level (DEFAULT) 010 = Enable until key 2 threshold level 011 = Enable until key 3 threshold level 100 = Enable until key 4 threshold level 101 = Enable until key 5 threshold level 110 = Enable until key 6 threshold level 111 = Enable until key 7 threshold level
		SARADC_VOLT_COEFF																	Digital Low Pass Filter Voltage Detection Coefficient $Y_n = \alpha X_n + (1-\alpha)Y_{n-1}$ $\alpha = 1/(2)coeff$

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		HY_COEFF																	Hysteresis Coefficient ($\Delta = \text{HY_COEFF}$) Coefficient ranges from 0-15 matching the binary value. SAR ADC Level is from Low to High Voltage: Level 0 is the lowest voltage. Each Level Threshold Voltage would add hysteresis. Threshold_ON = SARADC_VDET_THRx - Δ Threshold_OFF = SARADC_VDET_THRx + Δ X is the number from 0 to 7.)
		DEFAULT	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0x0110
15	VDET_TH RESHOL D_1	SARADC_VDET_THR0																	Key 0 SAR ADC Threshold Level Control (Binary values from 0 to 255 - lowest voltage)
		SARADC_VDET_THR1																	Key 1 SAR ADC Threshold Level Control (Binary values from 0 to 255)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
16	VDET_TH RESHOL D_2	SARADC_VDET_THR2																	Key 2 SAR ADC Threshold Level Control (Binary values from 0 to 255)
		SARADC_VDET_THR3																	Key 3 SAR ADC Threshold Level Control (Binary values from 0 to 255)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
17	VDET_TH RESHOL D_3	SARADC_VDET_THR4																	Key 4 SAR ADC Threshold Level Control (Binary values from 0 to 255)
		SARADC_VDET_THR5																	Key 5 SAR ADC Threshold Level Control (Binary values from 0 to 255)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
18	VDET_TH RESHOL D_4	SARADC_VDET_THR6																	Key 6 SAR ADC Threshold Level Control (Binary values from 0 to 255)
		SARADC_VDET_THR7																	Key 7 SAR ADC Threshold Level Control (Binary values from 0 to 255 - highest voltage)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
1A	GPIO_SEL	RESERVED																	RESERVED
		GPIO1POL																	GPIO1 Polarity 0 = Non-inverted (DEFAULT) 1 = Inverted logic of the CSB/GPIO1 function output selected by GPIO1SEL
		GPIO1SEL																	CSB/GPIO1 Function Select 000 = Input as MODE pin#33 input logic level (DEFAULT) 001 = RESERVED 010 = RESERVED 011 = DAC auto mute condition (logic 1 = one or both DACs auto muted) 100 = Output divided FLL clock 101 = FLL locked condition (logic 1 = PLL locked) 110 = Output as logic 1 condition 111 = Output as logic 0 condition
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
1C	PORT0_I2S_PCM_CTRL_1	DACCM																	DAC Companding Mode Select 00 = Off (DEFAULT - Normal linear operation) 01 = RESERVED 10 = μ -law companding 11 = A-law companding
		ADCCM																	ADC Companding Mode Select 00 = Off (DEFAULT - Normal linear operation) 01 = RESERVED 10 = μ -law companding 11 = A-law companding
		ADDAP																	ADC Output Data Stream Directly Routed To DAC Input Data Path Enable Control 0 = Disable (DEFAULT) 1 = Enable

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		CMB8																	8-bit Word For Companding Mode Of Operation Enable Control 0 = Normal operation (DEFAULT - No companding) 1 = 8-bit operation for companding mode
		UA_OFF																	uLaw Offset Select 0 = 1's complement (DEFAULT) 1 = 2's complement
		BCP																	Bit Clock Phase Inversion Option For BCLK 0 = Non-inverted (DEFAULT) 1 = Inverted
		LRP																	PCMA & PCMB Left/right Word Ordering Select 0 = Right Justified/Left Justified/I2S/PCMA mode (DEFAULT) 1 = PCMB Mode Enable: MSB is valid on 1st rising edge of BCLK after rising edge of FS
		DACPHS																	DAC Audio Data Left-right Ordering Select 0 = Left DAC data in left phase of LRP (DEFAULT) 1 = Left DAC data in right phase of LRP (left-right reversed)
		WLEN																	Word Length of Audio Data Stream Select 00 = 16-bit word length 01 = 20-bit word length 10 = 24-bit word length (DEFAULT) 11 = 32-bit word length
		AIFMT																	Audio Interface Data Format Select 00 = Right justified 01 = Left justified 10 = Standard I2S format 11 = PCMA or PCMB audio data format option (DEFAULT)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0x000B
1D	PORT0_I2S_PCM_CTRL_2	I2S_TRI																	I2S Tri State Enable Control 0 = Normal mode (DEFAULT) 1 = Output high Z
		I2S_DRV																	I2S Drive Enable Control 0 = Normal mode (DEFAULT) 1 = Always out
		LRC_DIV																	LRC(FS) Divider From BCLK Frequency 00 = 1/256 (DEFAULT) 01 = 1/128 10 = 1/64 11 = 1/32
		PCM_TS																	PCM Time Slot Function Enable Control (Only PCM_A_MODE or PCM_B_MODE-STEREO Only can be used when PCM Mode is selected.) 0 = Disable time slot function for PCM mode (DEFAULT) 1 = Enable time slot function for PCM mode
		TRI																	Without TDM Mode 0 = Drive the full clock of LSB (DEFAULT) 1 = Tri-state the 2nd half of LSB
		PCM8BIT																	8-Bit PCM Select 0 = Use PORT0_I2S_PCM_CTRL_1.WLEN to select word length (DEFAULT) 1 = PCM select 8-bit word length
		ADCDAT_PE																	ADCDAT IO Pull Enable Control 0 = Disable (DEFAULT) 1 = Enable
		ADCDAT_PS																	ADCDAT IO Pull Up/Down Enable Control 0 = Pull down (DEFAULT) 1 = Pull up
		ADCDAT_OE																	ADCDAT IO Pull Up/Down Enable Control 0 = Pull down 1 = Pull up (DEFAULT)
		MS																	ADCDAT IO Output Enable Control 0 = ADCDAT not always out (DEFAULT - when no data out, ADCOUT pin becomes high.) 1 = ADCDAT always out

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		BCLKDIV																	Master/Slave Mode Enable Control 0 = Slave mode (DEFAULT) 1 = Master mode
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0x0010
1E	PORT0_LEFT_TIME_SLOT																		RESERVED
		TSLOT_L																	Left Channel PCM Time Slot Start Value (When PCM_TS =1, both TSLOT_L and TSLOT_R need to set different values: N*WordLength+1 Or PCM TDM Offset Mode Slot start value when in TDM_CTRL both TDM and PCM_OFFSET_MODE_CTRL both are 1 Shift value= N*WordLength+1. 4 channels will shift together and need have enough channels available > 4 channels.)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
1F	PORT0_RIGHT_TIME_SLOT	FS_ERR_CMP_SEL																	Triggers Short Frame Sync Signal Select (If frame sync is less than) 00 = 252 x MCLK 01 = 253 x MCLK (DEFAULT) 10 = 254 x MCLK 11 = 255 x MCLK
		DIS_FS_SHORT_DET																	Short Gram Sync Detection Logic Enable Control 0 = Enable (DEFAULT) 1 = Disable
		TSLOT_R																	Right Channel PCM Time Slot Start Value (When PCM_TS =1 both TSLOT_L0 and TSLOT_R0 need to set different values: N*WordLength+1 And unused for PCM TDM Offset Mode)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
20	TDM_CTRL	TDM_MODE																	TDM Enable Control 0 = Disable (DEFAULT) 1 = Enable
		TDM_PCM_TS_MODE																	PCM Offset In TDM Enable Control 0 = Non-inverted (DEFAULT) 1 = Inverted
		DAC_LSEL																	DAC Left Channel Source Under TDM Mode (TDM = 1 & PCM_OFFSET_MODE_CTRL = 0) I2S: 00 = Slot 0 of right (DEFAULT) 01 = Slot 1 of right 10 = RESERVED 11 = RESERVED PCM: 00 = From slot 0 (DEFAULT) 01 = From slot 1 10 = From slot 2 11 = From slot 3
		DAC_RSEL																	DAC Right Channel Source Under TDM Mode (TDM = 1 & PCM_OFFSET_MODE_CTRL = 0) I2S: 00 = Slot 0 of right (DEFAULT) 01 = Slot 1 of right 10 = RESERVED 11 = RESERVED PCM: 00 = From slot 0 (DEFAULT) 01 = From slot 1 10 = From slot 2 11 = From slot 3

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		ADC_TXEN																	ADC Data Source Under TDM/I2S Mode 00 = From slot 0 (DEFAULT) 01 = From slot 1 10 = From slot 2 11 = From slot 3
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
23	ADC_HPF_FILTER	HPFEN_ADC_CH23																	ADC CH23 HPF Enable Control 0 = Disable (DEFAULT) 1 = Enable
		HPFAM_ADC_CH23																	ADC CH23 HPF Application Mode 0 = Disable (DEFAULT) 1 = Enable
		HPFCUT_ADC_CH23																	ADC CH23 HPF Application Mode Cutoff Frequency Select (See HPFCUT_TABLE for more information)
		HPFEN_ADC_CH01																	ADC CH01 HPF Enable Control 0 = Disable (DEFAULT) 1 = Enable
		HPFAM_ADC_CH01																	ADC CH01 HPF Application Mode 0 = Disable (DEFAULT) 1 = Enable
		HPFCUT_ADC_CH01																	ADC CH01 HPF Application Mode Cutoff Frequency Select (See HPFCUT_TABLE for more information)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
24	ADC_FILTER_CTRL	ADC_ZC_EN																	ADC Gain Zero Crossing Update Enable Control 0 = Disable (DEFAULT) 1 = Enable
		RESERVED																	RESERVED
		SMPL_RATE																	Audio Data Sample Rate Indication 000 = 48KHz (DEFAULT) 001 = 32KHz 010 = 24KHz 011 = 16KHz 100 = 12KHz 101 = 8KHz 110 = 96KHz 111 = RESERVED
		ADC_RATE																	ADC SINC Down Select 00 = Down 32 01 = Down 64 10 = Down 128 (DEFAULT) 11 = Down 256
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0x0002
25	DAC_FILTER_CTRL_1	DISABLE_DEM																	Dynamic Element Matching Disable Control 0 = Disable (DEFAULT) 1 = Enable (to disable DEM control of RateConvert2 module)
		FILT_SYNC																	Filter Reference Start Point Select 0 = Based on REG1[5:0] start point (DEFAULT) 1 = Based on LRC
		HPFEN_DAC																	DAC HPF Enable Control 0 = Disable (DEFAULT) 1 = Enable
		HPFAM_DAC																	DAC HPF Application Mode 0 = Disable (DEFAULT) 1 = Enable
		HPFCUT_DAC																	DAC HPF Application Mode Cutoff Frequency Select (See HPFCUT_TABLE for more information)
		RESERVED																	RESERVED
		DAC_RATE																	DAC Oversample Rate Select 000 = 64 (DEFAULT) 001 = 256 010 = 128 100 = 32
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
26	DAC_FILTER_CTRL_2	DEM_DITHER																	First Order Dynamic Element Matching Dithering Select (Set probability of first order DEM dithering.) (Step size is 1/16.) 0000 = No dithering (DEFAULT) 0001 = 1/16 0010 = 2/16 0011 = 3/16 0100 = 4/16 0101 = 5/16 0110 = 6/16 0111 = 7/16 1000 = 8/16 1001 = 9/16 1010 = 10/16 1011 = 11/16 1100 = 12/16 1101 = 13/16 1110 = 14/16 1111 = 15/16
		SDMOD_DITHER																	Bit Numbers Of Dithering On SD Modulator (Step size is 1bit.) 0000 = No dithering (DEFAULT) 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 0110 = 6 0111 = 7 1000 = 8 1001 = 9 1010 = 10 1011 = 11 1100 = 12 1101 = 13 1110 = 14 1111 = 15
		DAC_STEP_SEL																	DAC Output Step Select 0XX = Use internal step (DEFAULT) 100 = Clock DAC 101 = Delay 1 cycle of MCLK 110 = Delay 2 cycles of MCLK 111 = Delay 3 cycles of MCLK
		DACPL																	DAC Output Polarity 0 = Non-inverted (DEFAULT) 1 = Inverted
		DACIN_SRC																	DAC Source Select 000 = From DRC OUT (DEFAULT) 001 = From HPF/EQ/NF OUT 010 = From SIN OUT 011 = From U/A Decode OUT 100 = From Mixer OUT
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
27	NOTCH_FILTER_1	NFU1																	Notch Filter 1 Update Bit 0 = (DEFAULT) Register write causes new value to be pending an update bit event on REG28(NOTCH FILTER2) 1 = Register write operation will load new REG27(NOTCH FILTER1) value and any pending value in REG28(NOTCH FILTER2) to be effective
		NFEN																	Notch Filter Enable Control 0 = Disable (DEFAULT) 1 = Enable
		NFA0																	Notch Filter A0 Coefficient LSB
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
28	NOTCH_FILTER_2	NFU2																	Notch Filter 2 Update Bit 0 = (DEFAULT) Register write causes new value to be pending an update bit event on REG27(NOTCH FILTER1) 1 = Register write operation will load new REG28(NOTCH FILTER2) value and any pending value in REG27(NOTCH FILTER1) to be effective
		NOTCH_DLY_DIS																	Notch Filter Delay Enable Control 0 = Enable (DEFAULT - Inserts 512 samples delay when the notch filter is turned on, to reduce "ping noise") 1 = Disable
		NFA1																	Notch Filter A1 Coefficient LSB
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
29	EQ1_LOW	FS_ERR_FLUSH																	Filter Value Reset Control 0 = (DEFAULT) 1 = Reset
		RESERVED																	RESERVED
		EQON																	EQ Enable Control 0 = Disable (DEFAULT) 1 = Enable
		EQMODE																	EQ Block Assignment Mode Select 0 = EQ block assigned on ADC 1 = EQ block assigned on DAC (DEFAULT)
		EQ1BW																	EQ1 Bandwidth Control 0 = Narrow bandwidth (DEFAULT) 1 = Wide bandwidth
		EQ1C																	EQ1 Band-pass Center Frequency Select 00 = 80KHz 01 = 105KHz (DEFAULT) 10 = 135KHz 11 = 175KHz
		EQ1G																	EQ1 Digital Gain Control (Step size is 1dB.) 0x00 = +12dB 0x01 = +11dB ▼ 0x0C = 0dB (DEFAULT) ▼ 0x17 = -11dB 0x18 = -12dB
		DEFAULT	0	0	0	1	0	0	0	1	0	0	1	0	1	1	0	0	0x112C
2A	EQ2_EQ3	EQ3BW																	EQ3 Bandwidth Control 0 = Narrow bandwidth (DEFAULT) 1 = Wide bandwidth
		EQ3C																	EQ3 Band-pass Center Frequency Select 00 = 650KHz 01 = 850KHz (DEFAULT) 10 = 1.1KHz 11 = 1.4KHz
		EQ3G																	EQ3 Digital Gain Control (Step size is 1dB.) 0x00 = +12dB 0x01 = +11dB ▼ 0x0C = 0dB (DEFAULT) ▼ 0x17 = -11dB 0x18 = -12dB
		EQ2BW																	EQ2 Bandwidth Control 0 = Narrow bandwidth (DEFAULT) 1 = Wide bandwidth
		EQ2C																	EQ2 Band-pass Center Frequency Select 00 = 230KHz 01 = 300KHz (DEFAULT) 10 = 285KHz 11 = 500KHz

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		EQ2G																	EQ2 Digital Gain Control (Step size is 1dB.) 0x00 = +12dB 0x01 = +11dB ▼ 0x0C = 0dB (DEFAULT) ▼ 0x17 = -11dB 0x18 = -12dB
		DEFAULT	0	0	1	0	1	1	0	0	0	0	1	0	1	1	0	0	0x2C2C
2B	EQ4_EQ5	EQ5BW																	EQ5 Bandwidth Control 0 = Narrow bandwidth (DEFAULT) 1 = Wide bandwidth
		EQ5C																	EQ5 -3dB Cut-off Frequency Select 00 = 5.3KHz 01 = 6.9KHz (DEFAULT) 10 = 9.0KHz 11 = 11.7KHz
		EQ5G																	EQ5 Digital Gain Control (Step size is 1dB.) 0x00 = +12dB 0x01 = +11dB ▼ 0x0C = 0dB (DEFAULT) ▼ 0x17 = -11dB 0x18 = -12dB
		EQ4BW																	EQ4 Bandwidth Control 0 = Narrow bandwidth (DEFAULT) 1 = Wide bandwidth
		EQ4C																	EQ4 Band-pass Center Frequency Select 00 = 1.8KHz 01 = 2.4KHz (DEFAULT) 10 = 3.2KHz 11 = 4.1KHz
		EQ4G																	EQ4 Digital Gain Control (Step size is 1dB.) 0x00 = +12dB 0x01 = +11dB ▼ 0x0C = 0dB (DEFAULT) ▼ 0x17 = -11dB 0x18 = -12dB
		DEFAULT	0	0	1	0	1	1	0	0	0	0	1	0	1	1	0	0	0x2C2C
2D	ADC_CH0_DGAIN_CTRL	DACTOADC_ATTU_CH0																	DAC To ADC CH0 Attenuation Control (Step size is 3dB.) 0x00 = Mute 0x02 = -128dB 0x03 = -36dB 0x04 = -33dB ▼ 0x0E = -3dB 0x0F = 0dB
		DACTOADC_CH0_SEL																	DAC To ADC CH0 Source Select 0 = CH0 (DEFAULT) 1 = CH1
		ADC_CH0_SEL																	ADC Mixer Source Select 00 = ADC CH0 (DEFAULT) 01 = ADC CH1 10 = ADC CH2 11 = ADC CH3

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DGAIN_ADC_CH0																	ADC CH0 Digital Gain Control (Step size is 0.5dB.) 0x000 = -128dB 0x001 = -127.5dB ▼ 0x100 = 0dB (DEFAULT) ▼ 0x163 = +49.5dB 0x164 = +50dB
		DEFAULT	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0x0100
2E	ADC_CH1_DGAIN_CTRL	DACTOADC_ATTU_CH1																	DAC To ADC CH1 Attenuation Control (Step size is 3dB.) 0x00 = Mute 0x02 = -128dB 0x03 = -36dB 0x04 = -33dB ▼ 0x0E = -3dB 0x0F = 0dB
		DACTOADC_CH1_SEL																	DAC To ADC CH1 Source Select 0 = CH0 (DEFAULT) 1 = CH1
		ADC_CH1_SE_L																	ADC Mixer Source Select 00 = ADC CH0 (DEFAULT) 01 = ADC CH1 10 = ADC CH2 11 = ADC CH3
		DGAIN_ADC_CH1																	ADC CH1 Digital Gain Control (Step size is 0.5dB.) 0x000 = -128dB 0x001 = -127.5dB ▼ 0x100 = 0dB (DEFAULT) ▼ 0x163 = +49.5dB 0x164 = +50dB
		DEFAULT	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0x0100
2F	ADC_CH2_DGAIN_CTRL	DACTOADC_ATTU_CH2																	DAC To ADC CH2 Attenuation Control (Step size is 3dB.) 0x00 = Mute 0x02 = -128dB 0x03 = -36dB 0x04 = -33dB ▼ 0x0E = -3dB 0x0F = 0dB
		DACTOADC_CH2_SEL																	DAC To ADC CH2 Source Select 0 = CH0 (DEFAULT) 1 = CH1
		ADC_CH2_SE_L																	ADC Mixer Source Select 00 = ADC CH0 (DEFAULT) 01 = ADC CH1 10 = ADC CH2 11 = ADC CH3
		DGAIN_ADC_CH2																	ADC CH2 Digital Gain Control (Step size is 0.5dB.) 0x000 = -128dB 0x001 = -127.5dB ▼ 0x100 = 0dB (DEFAULT) ▼ 0x163 = +49.5dB 0x164 = +50dB
		DEFAULT	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0x0100

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
30	ADC_CH3_DGAIN_CTRL	DACTOADC_ATTU_CH3																	DAC To ADC CH3 Attenuation Control (Step size is 3dB.) 0x00 = Mute 0x02 = -128dB 0x03 = -36dB 0x04 = -33dB ▼ 0x0E = -3dB 0x0F = 0dB
		DACTOADC_CH3_SEL																	DAC To ADC CH3 Source Select 0 = CH0 (DEFAULT) 1 = CH1
		ADC_CH3_SE L																	ADC Mixer Source Select 00 = ADC CH0 (DEFAULT) 01 = ADC CH1 10 = ADC CH2 11 = ADC CH3
		DGAIN_ADC_CH3																	ADC CH3 Digital Gain Control (Step size is 0.5dB.) 0x000 = -128dB 0x001 = -127.5dB ▼ 0x100 = 0dB (DEFAULT) ▼ 0x163 = +49.5dB 0x164 = +50dB
		DEFAULT	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0x0100
31	DAC_MUTE_CTRL	AMUTE_EN																	Auto Mute Enable Control (Generate null output to analog circuitry when 1024 consecutive zeros are detected. De-assert as soon as first non-zero sample is detected.) 0 = Disable (DEFAULT) 1 = Enable
		AMUTE_CTRL																	Auto Mute Control 0 = Both DAC channels must have 0 values for 1024 samples before AMUTE turns on (DEFAULT) 1 = Either Ch0 or Ch1 must have 1024 consecutive zero samples
		SMUTE_EN																	Soft Mute Enable Control 0 = increase DAC volume to volume register setting (DEFAULT) 1 = Gradually lower DAC volume to zero
		SMUTE_CTRL																	DAC Limiter Output Enable Control 0 = (DEFAULT) 1 = (When soft mute is enabled, DAC limiter output is also muted to remove any DC offset produced by the audio processing block.)
		DAC_ZC_EN																	DAC Zero Crossing Enable Control 0 = Disable (DEFAULT) 1 = Enable
		DAC_CH01_MIXER																	DAC CH01 Data Mixing Control 0 = Normal (DEFAULT) 1 = 1/2(L+R)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
32	DAC_CH0_DGAIN_CTRL	MIXLR_SEL_CH0																	DAC CH1 Data Mixing Control 0 = No mix, pass ADC CH2 signal (DEFAULT) 1 = Mix I2S left channel
		ADCTODAC_CH0_SEL																	ADC To DAC CH0 Source Select 00 = ADC CH0 (DEFAULT) 01 = ADC CH1 10 = ADC CH2 11 = ADC CH3 or I2S left channel
		DAC_CH0_SE L																	DAC CH0 Source Select 0 = From I2S left channel (DEFAULT) 1 = From I2S right channel

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DGAIN_CH0_DAC																	DAC CH0 Digital Gain Control (Step size is 0.5dB.) 0x000 = -128dB 0x001 = -127.5dB ▼ 0x100 = 0dB (DEFAULT) ▼ 0x163 = +49.5dB 0x164 = +50dB
		DEFAULT	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0x0100
33	DAC_CH1_DGAIN_CTRL	MIXLR_SEL_CH1																	DAC CH1 Data Mixing Control 0 = No mix, pass ADC CH3 signal (DEFAULT) 1 = Mix I2S right channel
		ADCTODAC_CH1_SEL																	ADC To DAC CH1 Source Select 00 = ADC CH0 (DEFAULT) 01 = ADC CH1 10 = ADC CH2 11 = ADC CH3 or I2S right channel
		DAC_CH1_SEL																	DAC CH1 Source Select 0 = From I2S left channel (DEFAULT) 1 = From I2S right channel
		DGAIN_CH1_DAC																	DAC CH1 Digital Gain Control (Step size is 0.5dB.) 0x000 = -128dB 0x001 = -127.5dB ▼ 0x100 = 0dB (DEFAULT) ▼ 0x163 = +49.5dB 0x164 = +50dB
		DEFAULT	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0x0100
34	ADC_TO_DAC_ST	ADCTODAC_ATTU_CH0																	CH0 Sidetone Attenuation Control (Step size is 0.5dB.) 0x00 = -127.5dB (DEFAULT) 0x01 = -127dB ▼ 0xFF = -0.5dB 0xFE = 0dB
		ADCTODAC_ATTU_CH1																	CH1 Sidetone Attenuation Control (Step size is 0.5dB.) 0x00 = -127.5dB (DEFAULT) 0x01 = -127dB ▼ 0xFF = -0.5dB 0xFE = 0dB
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
38	DRC_KNEE_IP12_ADC_CH01	DRC_ENA_ADC_CH01																	DRC ADC CH01 Enable Control 0 = Disable (DEFAULT) 1 = Enable
		DRC_KNEE2_IP_ADC_CH01																	DRC ADC CH01 Knee Point 2 Select (Step size is 1dB.) 0x00 = 0dB 0x01 = -1dB ▼ 0x14 = -20dB (DEFAULT) ▼ 0x3E = -62dB 0x3F = -63dB
		DRC_SMOOTH_CH01																	DRC ADC CH01 Smooth Filter Enable Control 0 = Disable 1 = Enable (DEFAULT)

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DRC_KNEE1_IP_ADC_CH01																	DRC ADC CH01 Knee Point 1 Select (Step size is 1dB.) 0x00 = 0dB 0x01 = -1dB ▼ 0x06 = -6dB (DEFAULT) ▼ 0x1E = -30dB 0x1F = -31dB
		DEFAULT	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1	0	0x1486
39	DRC_KNEE_IP34_ADC_CH01	DRC_KNEE4_IP_ADC_CH01																	DRC ADC CH01 Knee Point 4 Select (Step size is 1dB.) 0x00 = -35dB 0x01 = -36dB ▼ 0x0F = -50dB (DEFAULT) ▼ 0x1E = -97dB 0x1F = -98dB
		DRC_KNEE3_IP_ADC_CH01																	DRC ADC CH01 Knee Point 3 Select (Step size is 1dB.) 0x00 = -18dB 0x01 = -19dB ▼ 0x12 = -36dB (DEFAULT) ▼ 0x1E = -80dB 0x1F = -81dB
		DEFAULT	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	0x0F12
3A	DRC_SLOPE_ADC_CH01	DRC_NG_SLP_ADC01																	DRC ADC CH01 Noise Gate Slope 00 = 1:1 01 = 2:1 10 = 4:1 (DEFAULT) 11 = 8:1
		DRC_EXP_SLP_ADC01																	DRC ADC CH01 Expansion Slope 00 = 1:1 01 = 2:1 10 = 4:1 (DEFAULT) 11 = RESERVED
		DRC_CMP2_SLP_ADC_CH01																	DRC ADC CH01 Compressor Slope (Lower Region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = RESERVED 111 = 1 (DEFAULT)
		DRC_CMP1_SLP_ADC_CH01																	DRC ADC CH01 Compressor Slope (Higher Region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = RESERVED 111 = 1 (DEFAULT)
		DRC_LMT_SLP_ADC_CH01																	DRC ADC CH01 Limiter Slope 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101 = 1:32 110 = 1:64 111 = 1 (DEFAULT)
		DEFAULT	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	0x25FF
3B	DRC_ATKDCY_ADC_CH01	DRC_PK_COEF1_ADC_CH01																	DRC ADC CH01 Peak Detection Attack Time (Ts = 1/SMPL_RATE) 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts (DEFAULT) 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1001 = 511*Ts

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DRC_PK_COEF2_ADC_CH01																	DRC ADC CH01 Peak Detection Release Time (Ts = 1/SMPL_RATE) 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts (DEFAULT) 0110 = 4095*Ts 0111 = 8191*Ts 1001 = 16383*Ts
		DRC_ATK_ADC_CH01																	DRC ADC CH01 Attack Time (Ts = 1/SMPL_RATE) 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts (DEFAULT) 0110 = 127*Ts 0111 = 255*Ts 1000 = 511*Ts 1001 = 1023*Ts 1010 = 2047*Ts 1011 = 4095*Ts 1100 = 8191*Ts
		DRC_DCY_ADC_CH01																	DRC ADC CH01 Decay Time (Ts = 1/SMPL_RATE) 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts (DEFAULT) 1000 = 16383*Ts 1001 = 32757*Ts 1010 = 65535*Ts
		DEFAULT	0	0	1	1	0	1	0	0	0	1	0	1	1	1	0	1	0x3457
3C	DRC_KNEE_IP12_ADC_CH23	DRC_ENA_ADC_CH23																	DRC ADC CH23 Enable Control 0 = Disable (DEFAULT) 1 = Enable
		DRC_KNEE2_IP_ADC_CH23																	DRC ADC CH23 Knee Point 2 Select (Step size is 1dB.) 0x00 = 0dB 0x01 = -1dB ▼ 0x14 = -20dB (DEFAULT) ▼ 0x3E = -62dB 0x3F = -63dB
		DRC_SMOOTH3																	DRC ADC CH23 Smooth Filter Enable Control 0 = Disable 1 = Enable (DEFAULT)
		DRC_KNEE1_IP_ADC_CH23																	DRC ADC CH23 Knee Point 1 Select (Step size is 1dB.) 0x00 = 0dB 0x01 = -1dB ▼ 0x06 = -6dB (DEFAULT) ▼ 0x1E = -30dB 0x1F = -31dB
		DEFAULT	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1	0	0x1486
3D	DRC_KNEE_IP34_ADC_CH23	DRC_KNEE4_IP_ADC_CH23																	DRC ADC CH23 Knee Point 4 Select (Step size is 1dB.) 0x00 = -35dB 0x01 = -36dB ▼ 0x0F = -50dB (DEFAULT) ▼ 0x1E = -97dB 0x1F = -98dB

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DRC_KNEE3_IP_ADC_CH23																	DRC ADC CH23 Knee Point 3 Select (Step size is 1dB.) 0x00 = -18dB 0x01 = -19dB ▼ 0x12 = -36dB (DEFAULT) ▼ 0x1E = -80dB 0x1F = -81dB
		DEFAULT	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	0x0F12
3E	DRC_SLOPE_ADC_CH23	DRC_NG_SLP_ADC23																	DRC ADC CH23 Noise Gate Slope 00 = 1:1 01 = 2:1 10 = 4:1 (DEFAULT) 11 = 8:1
		DRC_EXP_SLP_ADC23																	DRC ADC CH23 Expansion Slope 00 = 1:1 01 = 2:1 10 = 4:1 (DEFAULT) 11 = RESERVED
		DRC_CMP2_SLP_ADC23																	DRC ADC CH23 Compressor Slope (Lower Region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = RESERVED 111 = 1 (DEFAULT)
		DRC_CMP1_SLP_ADC23																	DRC ADC CH23 Compressor Slope (Higher Region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = RESERVED 111 = 1 (DEFAULT)
		DRC_LMT_SLP_ADC23																	DRC ADC CH23 Limiter Slope 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101 = 1:32 110 = 1:64 111 = 1 (DEFAULT)
		DEFAULT	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	0x25FF
3F	DRC_ATKDCY_ADC_CH23	DRC_PK_COEF1_ADC_CH23																	DRC ADC CH23 Peak Detection Attack Time (Ts = 1/SMPL_RATE) 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts (DEFAULT) 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1001 = 511*Ts
		DRC_PK_COEF2_ADC_CH23																	DRC ADC CH23 Peak Detection Release Time (Ts = 1/SMPL_RATE) 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts (DEFAULT) 0110 = 4095*Ts 0111 = 8191*Ts 1001 = 16383*Ts
		DRC_ATK_ADC_CH23																	DRC ADC CH23 Attack Time (Ts = 1/SMPL_RATE) 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts (DEFAULT) 0110 = 127*Ts 0111 = 255*Ts 1000 = 511*Ts 1001 = 1023*Ts 1010 = 2047*Ts 1011 = 4095*Ts 1100 = 8191*Ts

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DRC_DCY_A DC_CH23																	DRC ADC CH23 Decay Time (Ts = 1/SMPL_RATE) 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts (DEFAULT) 1000 = 16383*Ts 1001 = 32757*Ts 1010 = 65535*Ts
		DEFAULT	0	0	1	1	0	1	0	0	0	1	0	1	1	1	0	1	0x3457
40	DRC_GAINL_ADC0	DRC_GAIN_A DC0																	DRC Gain Read Out For ADC CH0 ([15:10] for integer, [9:0] for fraction)
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	READ ONLY
41	DRC_GAINL_ADC1	DRC_GAIN_A DC1																	DRC Gain Read Out For ADC CH1 ([15:10] for integer, [9:0] for fraction)
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	READ ONLY
42	DRC_GAINL_ADC2	DRC_GAIN_A DC2																	DRC Gain Read Out For ADC CH2 ([15:10] for integer, [9:0] for fraction)
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	READ ONLY
43	DRC_GAINL_ADC3	DRC_GAIN_A DC3																	DRC Gain Read Out For ADC CH3 ([15:10] for integer, [9:0] for fraction)
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	READ ONLY
45	DRC_KNEE_IP12_DAC	DRC_ENA_D AC																	DRC DAC Channel Enable Control 0 = Disable (DEFAULT) 1 = Enable
		DRC_KNEE2_ IP_DAC																	DRC DAC Knee Point 2 Select (Step size is 1dB.) 0x00 = 0dB 0x01 = -1dB ▼ 0x14 = -20dB (DEFAULT) ▼ 0x1E = -62dB 0x1F = -63dB
		DRC_SMTH_E NA_DAC																	DRC DAC Smooth Filter Enable Control 0 = Disable 1 = Enable (DEFAULT)
		DRC_KNEE1_ IP_DAC																	DRC DAC Knee Point 1 Select (Step size is 1dB.) 0x00 = 0dB 0x01 = -1dB ▼ 0x06 = -6dB (DEFAULT) ▼ 0x1E = -30dB 0x1F = -31dB
		DEFAULT	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1	0	0x1486
46	DRC_KNEE_IP34_DAC	DRC_KNEE4_ IP_DAC																	DRC DAC Knee Point 4 Select (Step size is 1dB.) 0x00 = -35dB 0x01 = -36dB ▼ 0x0F = -50dB (DEFAULT) ▼ 0x1E = -97dB 0x1F = -98dB
		DRC_KNEE3_ IP_DAC																	DRC DAC Knee Point 3 Select (Step size is 1dB.) 0x00 = -18dB 0x01 = -19dB ▼ 0x12 = -36dB (DEFAULT) ▼ 0x1E = -80dB 0x1F = -81dB
		DEFAULT	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	0x0F12

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
47	DRC_SLOPE_DAC	DRC_NG_SLP_DAC																	DRC DAC Noise Gate Slope 00 = 1:1 01 = 2:1 10 = 4:1 (DEFAULT) 11 = 8:1
		DRC_EXP_SLP_DAC																	DRC DAC Expansion Slope 00 = 1:1 01 = 2:1 10 = 4:1 (DEFAULT) 11 = 8:1
		DRC_CMP2_SLP_DAC																	DRC DAC Compressor Slope (Lower Region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = RESERVED 111 = 1 (DEFAULT)
		DRC_CMP1_SLP_DAC																	DRC DAC Compressor Slope (Higher Region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = RESERVED 111 = 1 (DEFAULT)
		DRC_LMT_SLP_DAC																	DRC DAC Limiter Slope 000 = 0 001 = 1:2 (DEFAULT) 010 = 1:4 011 = 1:8 100 = 1:16 101 = 1:32 110 = 1:64 111 = 1
		DEFAULT	0	0	1	0	0	1	0	1	1	1	1	1	1	0	0	1	0x25F9
48	DRC_ATKDCY_DAC	DRC_PK_COEF1_DAC																	DRC DAC Peak Detection Attack Time (Ts = 1/SMPL_RATE) 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts (DEFAULT) 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1XXX = RESERVED
		DRC_PK_COEF2_DAC																	DRC DAC Peak Detection Release Time (Ts = 1/SMPL_RATE) 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts (DEFAULT) 0110 = 4095*Ts 0111 = 8191*Ts 1XXX = RESERVED
		DRC_ATK_DAC																	DRC DAC Attack Time (Ts = 1/SMPL_RATE) 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts (DEFAULT) 0110 = 127*Ts 0111 = 255*Ts 1000 = 511*Ts 1001 = 1023*Ts 1010 = 2047*Ts 1011 = 4095*Ts 1100 = 8191*Ts
		DRC_DCY_DAC																	DRC DAC Decay Time (Ts = 1/SMPL_RATE) 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts (DEFAULT) 1000 = 16383*Ts 1001 = 32757*Ts 1010 = 65535*Ts
		DEFAULT	0	0	1	1	0	1	0	0	0	1	0	1	1	1	0	1	0x3457
49	DRC_GAIN_DAC_CH0	DRC_GAIN_DAC_CH0																	DRC Gain Read Out For DAC CH0 ([15:10] for integer, [9:0] for fraction)
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
4A	DRC_GAIN_DAC_CH1	DRC_GAIN_DAC_CH1																	DRC Gain Read Out For DAC CH1 ([15:10] for integer, [9:0] for fraction)
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
4C	MODE	RESERVED																	RESERVED
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
4D	MODE1	RESERVED																	RESERVED
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
4E	MODE2	RESERVED																	RESERVED
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
50	CLASSG	CLASSG_CLK_SRC																	Class-G Function Clock Divider Select 00 = Clock 2MHz (DEFAULT) 01 = 1/3 MCLK 10 = MCLK 11 = Disable CLK (disable charge pump)
		CLASSG_TIMER																	Class-G Timer Select (Define time for supplies go to ± 0.9 after a Class G signal goes lower than threshold voltage.) 000000 = (DEFAULT) 000001 = 1 ms 000010 = 2 ms 000100 = 8 ms 001000 = 16 ms 010000 = 32 ms 100000 = 64 ms
		CLASSG_THRESHOLD																	Class-G Threshold Select (Threshold for DAC signal level comparison for Class G supplies: Below threshold $\pm .9$ or above ± 1.8 Volt. 1 full scale=1 Vrms) 00 = 1/16 full scale (DEFAULT) 01 = 1/8 full scale 10 = 3/16 full scale 11 = 1/4 full scale
		CLASSG_CMP_EN																	Class-G Compare Path Enable Control (Each Bit enables according DAC path. If CLASSG_EN=1, and CLASSG_CMP_EN=00, supplies stay at $\pm .9$) 0 = Disable (DEFAULT) 1 = Enable Bit 0 = Left DAC Bit 1 = Right DAC
		CLASSG_EN																	Class-G Function Enable Control (± 0.9 Volt supply option) 0 = Disable (DEFAULT- only provide ± 1.8 V) 1 = Enable (supplies are either ± 1.8 or ± 0.9 depend on signal amplitudes, see CLASSG_CMP_EN)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
51	OPT_EFUSE	STANDBY_IN																	OTP Standby Status Register Control 0 = OTP standby (DEFAULT) 1 = OTP in operation mode
		NR_IN																	OTP Normal Read Mode Status Register Control 0 = Standby mode (DEFAULT) 1 = Normal read mode
		PGEN_IN																	OTP Program Mode Status Register Control Active Low 0 = Enable (DEFAULT) 1 = Disable
		STROBE_IN																	OTP Strobe Signal Status Register Control 0 = Disable (DEFAULT) 1 = Enable
		WL_BIN																	eFuse Determiner Bit (Determines which bit to read or write to on the eFuse)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
53	OTPDOU_T1	OTPDOUT1																	OTP Read Out Data Low 16 bits
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
54	OTPDOU_T2	OTPDOUT2																	OTP Read Out Data High 16 bits
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
55	MISC_CTL	RESERVED																	RESERVED
56	I2C_TIMEOUT	TIMEOUT_DISABLE																	Time-out Function Disable Control 0 = Disable (DEFAULT) 1 = Enable
		TIMEOUT_TM																	Time-out Function Coefficient
		DEFAULT	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0xEFFF
57	TEST_MODE	TEST_MODE																	RESERVED
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
58	I2C_DEVICE_ID	I2C_DEVICE_ID																	I2C Device ID
		REG_SI_REV																	I2C Silicon Revision ID
		DEFAULT	0	0	0	1	1	0	1	0	1	1	1	1	0	0	0	1	Read Only 0x1AF1
59	SAR_ADC_DATA_OUT	RATM_TEST_FINISH																	RAM Test Status Bit 0 = Test not finished (DEFAULT) 1 = Test finished
		RAM_TEST_FAIL																	RAM Test Result Bit 0 = Test passed (DEFAULT) 1 = Test failed
		ANALOG_MUTE																	Analog Mute Flag Bit 0 = Disable (DEFAULT) 1 = Enable
		SARADC_DO_UT																	SAR ADC Read Out
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only
66	BIAS_ADJ	RESERVED																	RESERVED
		VMIDEN																	VMID Enable Control 0 = Disable (DEFAULT) 1 = Enable
		VMIDSEL																	VMID Tie-off Select 00 = Open (DEFAULT) 01 = 25k Ohm 10 = 125k Ohm 11 = 2.5k Ohm
		DMICEN2																	DMIC2 Enable Control 0 = Disable (DEFAULT) 1 = Enable
		DMICEN1																	DMIC1 Enable Control 0 = Disable (DEFAULT) 1 = Enable
		BIASADJ																	PGA Master Bias Current Power Select 00 = Normal operation (DEFAULT) 01 = 25% bias current decrease 10 = 14% bias current decrease 11 = 25% bias current increase
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
67	PGA_GAIN	TESTRL																	Headphone Impedance Enable Control (Test/ IMM_MODE) 0 = Disable (DEFAULT) 1 = Enable
		MUTEL																	Left PGA Mute Enable Control 0 = Disable (DEFAULT) 1 = Enable
		M6DBL																	Left AMIC Attenuation Enable Control 0 = 0dB (DEFAULT) 1 = -6dB
		MUTER																	Right PGA Mute Enable Control 0 = Disable (DEFAULT) 1 = Enable
		M6DBR																	Right AMIC Attenuation Enable Control 0 = 0dB (DEFAULT) 1 = -6dB
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
68	TRIM_SETTINGS	DRV_IBCTRHS																	Headphone Output Driver Current Trim Select 1 0 = Low drive current (DEFAULT) 1 = High drive current
		DRV_ICUTHS																	Headphone Output Driver Current Trim Select 2 0 = Low drive current (DEFAULT) 1 = High drive current
		DIS_OC																	Offset Trim Disable Control 0 = Enable (DEFAULT) 1 = Disable Bit0/1 = RESERVED Bit2 = Left headphone output Bit3 = Right headphone output Bit4 = RESERVED
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
69	ANALOG_CONTR_OL_1	RESERVED																	RESERVED
		JKDET_L																	JKDET Threshold Low Select 00 = 0.22 x VDDA (DEFAULT) 10 = 0.40 x VDDA 11 = 0.5 x VDDA
		JKDET_H																	JKDET Threshold High Select 00 = 0.85 x VDDA (DEFAULT) 10 = 0.78 x VDDA 11 = 0.6 x VDDA
		DMIC_DS																	DMIC Clock Drive Current Select 0 = Low drive current (DEFAULT) 1 = High drive current
		DMIC_SLEW																	DMIC Clock Slew Rate Select (For high Cload > 20pF, use faster slew rate.) 000 = Slowest slew rate (DEFAULT) ▼ 111 = Fastest slew rate
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
6A	ANALOG_CONTR_OL_2	HP_AB_ADJ																	Headphone Driver Bias Current Adjust In Class-AB Mode 0 = Normal (DEFAULT) 1 = 2x
		HP_G_ADJ																	Headphone Driver Bias Current Adjust In Class-G Mode 0 = Normal (DEFAULT) 1 = 0.5x
		HP_ADJ																	Headphone Driver Bias Current Adjust In non-Class-G Mode 0 = Normal (DEFAULT) 1 = 2.5x
		HP_G_BST_A_DJ2																	Headphone Output Boost Driver Bias Current Adjust in Class-G Mode 1 0 = Normal (DEFAULT) 1 = Low
		HP_G_BST_A_DJ1																	Headphone Output Boost Driver Bias Current Adjust in Class-G Mode 2 0 = Normal (DEFAULT) 1 = Low
		RESERVED																	RESERVED
		ANALOG_CONTROL2																	Class-D Temperature Alarm Enable Control 0 = Disable (DEFAULT) 1 = Enable
		RESERVED																	RESERVED
		ANALOG_CONTROL2																	Class-D Clamp Disable Control 0 = Enable (DEFAULT - clamping feedback loop) 1 = Disable (better THD)
		RESERVED																	RESERVED
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
6B	ENABLE_LO	TESTDAC																	DAC Test Mode 0 = Disable (DEFAULT) 1 = Enable Bit0 = Force headphone left DAC to GND Bit1 = Force headphone right DAC to GND
		RESERVED																	RESERVED
		ENHSR																	Headphone Right Output Path Enable Control 0 = Disable (DEFAULT) 1 = Enable Bit0 = Enable DAC right channel to right headphone output driver Bit1 = Enable DAC left channel to right headphone output driver
		ENHSL																	Headphone Left Output Path Enable Control 0 = Disable (DEFAULT) 1 = Enable Bit0 = Enable DAC left channel to left headphone output driver Bit1 = Enable DAC right channel to left headphone output driver
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
6C	GAIN_LO	CLK_DAC_IN_V																	DAC Clock Polarity 0 = Non-inverted (DEFAULT) 1 = Inverted
		RESERVED																	RESERVED
		POLARITY																	Mixer Output Polarity 0 = Non-inverted (DEFAULT) 1 = Inverted Bit0 = Inverts left headset out signal phase Bit1 = Inverts right headset out signal phase
		RESERVED																	RESERVED
		GAINHSR																	Headphone Right Channel Output Gain Control (Step size is 1dB.) 000 = 0dB (DEFAULT) 001 = 1dB 010 = 2dB 011 = 3dB 100 = 4dB 101 = 5dB 110 = 6dB
		RESERVED																	RESERVED
		GAINHSL																	Headphone Left Channel Output Gain Control (Step size is 1dB.) 000 = 0dB (DEFAULT) 001 = 1dB 010 = 2dB 011 = 3dB 100 = 4dB 101 = 5dB 110 = 6dB
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
6D	CLASSD_GAIN_1	RESERVED																	RESERVED
		CLASSD_GAIN_1R																	Right Channel Class-D Driver Gain For DAC Right Input (Step size is 1dB.) 00000 = Mute (DEFAULT) 00001 = 0dB 00002 = 1dB ▼ 11000 = 23dB 11001 = 24dB
		ENCLASSD																	Class-D Amplifier Enable Control 0 = Disable (DEFAULT) 1 = Enable
		RESERVED																	RESERVED

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		CLASSDGAIN 1L																	Left Channel Class-D Driver Gain For DAC Right Input (Step size is 1dB.) 00000 = Mute (DEFAULT) 00001 = 0dB 00002 = 1dB ▼ 11000 = 23dB 11001 = 24dB
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
6E	CLASSD_GAIN_2	RESERVED																	RESERVED
		CLASSDGAIN 2R																	Right Channel Class-D Driver Gain For DAC Left Input (Step size is 1dB.) 00000 = Mute (DEFAULT) 00001 = 0dB 00002 = 1dB ▼ 11000 = 23dB 11001 = 24dB
		RESERVED																	RESERVED
		CLASSDGAIN 2L																	Left Channel Class-D Driver Gain For DAC Left Input (Step size is 1dB.) 00000 = Mute (DEFAULT) 00001 = 0dB 00002 = 1dB ▼ 11000 = 23dB 11001 = 24dB
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
71	ANALOG_ADC_1	RESERVED																	RESERVED
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0x0011
72	ANALOG_ADC_2	RESERVED																	RESERVED
		ADC_UPR																	Right Channel PGA Bias Current Increase Enable Control (For driving ADC at high sample rates) 0 = Disable (DEFAULT) 1 = Enable
		ADC_UPL																	Left Channel PGA Bias Current Increase Enable Control (For driving ADC at high sample rates) 0 = Disable (DEFAULT) 1 = Enable
		RESERVED																	RESERVED
		BIAS																	ADC Bias Current Select 00 = Nominal (DEFAULT) 01 = Double 10 = Half 11 = Quarter
		VREFSEL																	ADC VREF Select 00 = Analog supply (DEFAULT) 01 = VMID 10 = VMID + 0.5dB 11 = VMID + 1dB
		PDNOTR																	Right ADC Analog Power Enable Control 0 = Disable (DEFAULT) 1 = Enable
		PDNOTL																	Left ADC Analog Power Enable Control 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0x0020

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
73	RDAC	DAC_EN																	DAC Enable Control 0 = Disable (DEFAULT) 1 = Enable Bit0 = Left DAC Bit1 = Right DAC
		CLK_DAC_EN																	DAC Clock Enable Control 0 = Disable (DEFAULT) 1 = Enable Bit0 = Left DAC Bit1 = Right DAC
		FC_CTR																	DAC Smoothing Filter On HS Output Enable Control 0 = Disable (DEFAULT) 1 = Enable
		CLK_DAC_DELAY																	DAC Clock Delay Select 000 = Delay 0 nsec (DEFAULT) 100 = Delay 4 nsec 001 = Delay 1 nsec 101 = Delay -3 nsec 010 = Delay 2 nsec (Recommended) 110 = Delay -2 nsec 011 = Delay 3 nsec 111 = Delay -1 nsec
		DACVREFSEL																	DAC Full Scale Reference Voltage Select (By setting this value, it will change DAC full scale output. For best performance, use default value.) 00 = External VDDA 01 = 1.5V 10 = 1.6V (DEFAULT) 11 = 1.7V
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0x0008
74	MIC_BIAS	INT2KB																	MICBIAS1 Internal 2K Ohm Resistor For MCGND Enable Control 0 = Disable (DEFAULT) 1 = Enable
		INT2KA																	MICBIAS1 Internal 2K Ohm Resistor For MCGND Enable Control 0 = Disable (DEFAULT) 1 = Enable
		LOWNOISE																	Low Power / Low Noise Mode Select 0 = Low power mode (DEFAULT) 1 = Low noise mode
		POWERUP																	MICBIAS1 Power Enable Control 0 = Disable (DEFAULT) 1 = Enable
		NOCAP																	Low Noise Mode Capacitance Select 0 = 2.2uF or 4.7uF on MICBIAS1 output (DEFAULT) 1 = No capacitance on MICBIAS1 output
		MICBIASLVL1																	MICBIAS1 Output Level Select 000 = VDDA 001 = 1x 010 = 1.1x 011 = 1.2x 100 = 1.3x 101 = 1.4x 110 = 1.53x (DEFAULT) 111 = 1.53x
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0x0006
75	HS_VOLUME_CONTROL	MUTE_HSPG_A2																	Headset Right PGA Mute Enable Control 0 = Disable (DEFAULT) 1 = Enable
		MUTE_HSPG_A1																	Headset Left PGA Mute Enable Control 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
76	BOOST	CLR_APR_EMERGENCY_SHUTDOWN																	Clear Headset Short Circuit Shutdown IRQ 0 = (DEFAULT) 1 = Reset (Momentary)

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		STG2_SEL																	PGA In Class-A Mode Of Operation Enable Instead Of Class-AB Enable Control 0 = Disable (DEFAULT) 1 = Enable
		PDVMDFAST																	VMID Pre-charge Disable Control 0 = Disable (DEFAULT) 1 = Enable
		BIASEN																	Global Analog Bias Enable Control 0 = Disable (DEFAULT) 1 = Enable
		DISCHRG																	Charge Input Enable Control 0 = Disable (DEFAULT) 1 = Enable
		BYPS_IBCTR																	Bypass PGA Current Control Enable Control 0 = Disable (DEFAULT) 1 = Enable
		BOOSTDIS																	HP Boost Driver Disable Control 0 = Enable (DEFAULT) 1 = Disable
		BOOSTGDIS																	HP Boost Driver In Class-G Mode Disable Control 0 = Enable (DEFAULT) 1 = Disable
		SHRT_SHTDWN_DIG_EN																	Short Circuit Shut Down Digital Part Enable Control 0 = Disable (DEFAULT) 1 = Enable
		EN_SHRT_SHTDWN																	Automatic Short-circuit Shutdown Enable Control 0 = (Driver shuts down after 16.3 μ sec debounce when shortage detected. IRQ pin Interrupt is generated. When SHRT_SHTDWN_DIG_EN = 0, APR_EMRGNCY_SHTDWN is cleared if the IRQ pin Interrupt cleared. Users need to clear IRQ pin interrupt. When SHRT_SHTDWN_DIG_EN = 1, APR_EMRGNCY_SHTDWN is cleared 1630 μ sec after shortage removed. Users need to clear IRQ pin interrupt.) 1 = (Headset driver power will be down immediately when shortage detected. No interrupt will be generated.)
		HS_SHRT_THRES_HLD																	Headset Short Circuit Protection Limit 00= 115mA at +FS (DEFAULT) 11= 155mA at +FS
		PAMP_THRS_HLD																	Adjust HS Boost P-driver Bias Current 00 = Normal (DEFAULT) 11 = Decrease current
		NAMP_THRS_HLD																	Adjust HS Boost N-driver Bias Current 00 = Normal (DEFAULT) 11 = Decrease current
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
77	FEPGA	RESERVED																	RESERVED
		CMLCK_ADJ																	PGA Common Mode Threshold Lock Adjust 00 = (DEFAULT)
		IB_LOOP_CTRL																	PGA Current Trim 0 = (DEFAULT)
		IBCTR_CODE																	PGA Current Trim 000 = (DEFAULT)

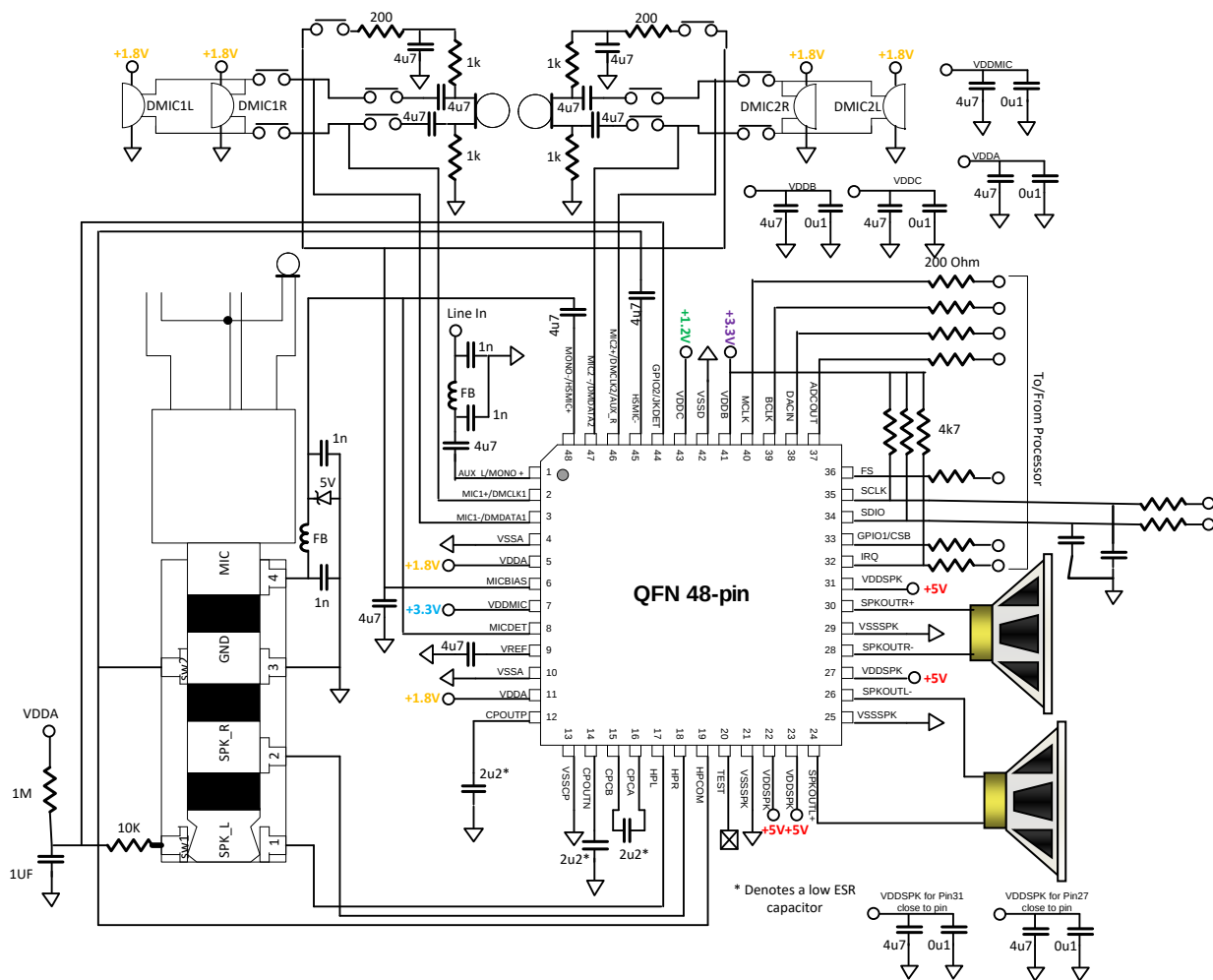
REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		FEPGA_MODER																	Right Channel PGA Input Mode Select 0 = Disable (DEFAULT) 1 = Enable Bit0 = MONO-/HSMIC+/HSMIC- (QFN) AUX_R/HSMIC+/HSMIC- (WLCSP) Bit1 = MIC2+/DMCLK2/MIC2-/DMDATA2/AUXR(QFN) MIC2+/DMCLK2/MIC2-/DMDATA2 (WLCSP) Bit2 = RESERVED Bit3 = Shorts each inputs and terminates with 12kOhm differentially
		FEPGA_MODEL																	Left Channel PGA Input Mode Select 0 = Disable (DEFAULT) 1 = Enable Bit0 = AUXL/MONO+/MONO-/HSMIC+ (QFN) AUXL/MONO+/MONO- (WLCSP) Bit1 = MIC1+/DMCLK1/MIC1-/DMDATA1 Bit2 = RESERVED Bit3 = Shorts each inputs and terminates with 12kOhm differentially
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
78	FEPGA_II	ACDC_CTRL																	Charge Input To VREF Enable Control (Effective when DISCHRG = 1) 0 = Disable (DEFAULT) 1 = Enable Bit 0 = AUXL/MONO+/MONO-/HSMIC+ (QFN) AUXL/MONO+/MONO- (WLCSP) Bit 1 = MONO-/HSMIC+/HSMIC- (QFN) AUX_R/HSMIC+/HSMIC- (WLCSP) Bit 2 = MIC1+/DMCLK1/MIC2+/DMCLK2 Bit 3 = MIC1-/DMDATA1/MIC2-/DMATA2
		FEPGA_GAINR																	Right PGA Gain Control (Step size is 2dB.) 0x00 = 0dB (DEFAULT) 0x01 = 2dB ▼ 0x11 = 34dB 0x12 = 36dB
		FEPGA_GAINL																	Left PGA Gain Control (Step size is 2dB.) 0x00 = 0dB (DEFAULT) 0x01 = 2dB ▼ 0x11 = 34dB 0x12 = 36dB
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
79	FEPGA_SE	RESERVED																	RESERVED
		FEPGASER																	Right Channel Front End PGA Single Ended Input Select 0 = Disable (DEFAULT) 1 = Enable Bit 0 = MONO-/HSMIC+ Bit 1 = HSMIC- Bit 2 = MIC2+/DMCLK2/AUXR Bit 3 = MIC2-/DMDATA2
		RESERVED																	RESERVED
		FEPGASEL																	Left Channel Front End PGA Single Ended Input Select 0 = Disable (DEFAULT) 1 = Enable Bit 0 = AUXL/MONO+ Bit 1 = MONO-/HSMIC+ Bit 2 = MIC1+/DMCLK1 Bit 3 = MIC1-/DMDATA1
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
		RESERVED																	RESERVED

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
7A	FEPGA_ATTENUATION	FEPGA_ATTN_R																	Right Channel Front End PGA Attenuation Control QFN (MONO-/HSMIC+)&(HSMIC-) WLCSP (AUXR/HSMIC+)&(HSMIC-) (Step size is 1.5dB.) 00000 = 0dB (DEFAULT) 00001 = -1.5dB ▼ 11110 = -45dB 11111 = -46.5dB
		RESERVED																	RESERVED
		FEPGA_ATTN_L																	Left Channel Front End PGA Attenuation Control QFN (AUXL/MONO+)&(MONO-/HSMIC+) WLCSP (AUXL/MONO+)&(MONO-) (Step size is 1.5dB.) 00000 = 0dB (DEFAULT) 00001 = -1.5dB ▼ 11110 = -45dB 11111 = -46.5dB
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
7B	ATT_PORT0	ATT0HSR																	RDAC To Right Headset Attenuation Control (Step size is 1dB.) 0x00 = 0dB (DEFAULT) 0x01 = -1dB ▼ 0x1E = -30dB 0x1D = -29dB
		ATT0HSL																	LDAC To Light Headset Attenuation Control (Step size is 1dB.) 0x00 = 0dB (DEFAULT) 0x01 = -1dB ▼ 0x1E = -30dB 0x1D = -29dB
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
7C	ATT_PORT1	ATT1HSR																	LDAC To Right Headset Attenuation Control (Step size is 1dB.) 0x00 = 0dB (DEFAULT) 0x01 = -1dB ▼ 0x1E = -30dB 0x1D = -29dB
		ATT1HSL																	RDAC To Light Headset Attenuation Control (Step size is 1dB.) 0x00 = 0dB (DEFAULT) 0x01 = -1dB ▼ 0x1E = -30dB 0x1D = -29dB
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
7F	POWER_UP_CONTROL	PUPR																	Left PGA Power Enable Control 0 = Disable (DEFAULT) 1 = Enable
		PUPL																	Right PGA Power Enable Control 0 = Disable (DEFAULT) 1 = Enable
		PUP_DRV_IN_STG																	Output Driver Power Enable Control (To reduce pop noise, turn on this first, then turn on PUP_MAIN_DRV) 0 = Disable (DEFAULT) 1 = Enable Bit0 = Left HP driver Bit1 = Right HP driver
		PUP_MAIN_DRV																	Main Driver Power Enable Control 0 = Disable (DEFAULT) 1 = Enable Bit0 = Left HP driver Bit1 = Right HP driver

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
80	CHARGE_PUMP_AND_POWER_DOWN_CONTROL	RESERVED																	RESERVED
		PULL_SPKR_DWN																	Speaker Pull Down Resistor Enable Control (Only work with PUP_MAIN_DRV=00) 0 = Disable (DEFAULT) 1 = Enable Bit0 = Pull HS Left speaker output to ground via a 16ohm resistor Bit1 = Pull HS Right speaker output to ground via a 16ohm resistor
		PD_DAC																	DAC Power Down Bar Enable Control 00 = Disable 11 = Enable (DEFAULT)
		JAMFORCE2																	Register Output Force 1 Control (Charge pump clock to fast) 0 = Disable (DEFAULT) 1 = Enable
		JAMFORCE1																	Register Output Force 2 Control (Charge pump clock to fast) 0 = Disable (DEFAULT) 1 = Enable
		RNIN																	Charge Pump Enable Control 0 = Disable (DEFAULT) 1 = Enable
		PRECHARGE																	VPOS Pre-charge Enable Control (For faster startup) 0 = Disable (DEFAULT) 1 = Enable
		DISCHARGEVEE																	VEE Pad Discharge Enable Control 0 = Disable (DEFAULT) 1 = Enable
		DISCHARGEVPOS																	VPOS Pad Discharge Enable Control 0 = Disable (DEFAULT) 1 = Enable
		SHCIRSEL2																	Charge Up Current Limit 2 0 = Low (DEFAULT) 1 = High
		SHCIRSEL1																	Charge Up Current Limit 1 0 = Low (DEFAULT) 1 = High
		DEFAULT	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0x0300
81	CHARGE_PUMP_INPUT_READ	APR_EMRGNCY_SHTDWN																	APR Emergency Short Circuit Shutdown IRQ
		MODE1BUF																	Monitor MODE1 State Of Charge Pump Block
		NODCBUF																	Monitor Charge Pump Drawing DC Current 0 = Drawing 1 = Not drawing (DEFAULT)
		RN2BUF																	Monitor Charge Pump Enable Status 0 = Off (DEFAULT) 1 = On
		VPOSOK																	Monitor High Voltage Status Of VPOS 0 = Possible short circuit (DEFAULT) 1 = Max output (Normal operation)
		VCOMPBUF																	Monitor Low Voltage & Low Current Status Of Charge Pump 0 = No current 1 = With current (DEFAULT)
		FORCE1BUF																	Monitor Charge Pump Frequency Status 0 = Normal 1 = Max frequency (DEFAULT)
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Only

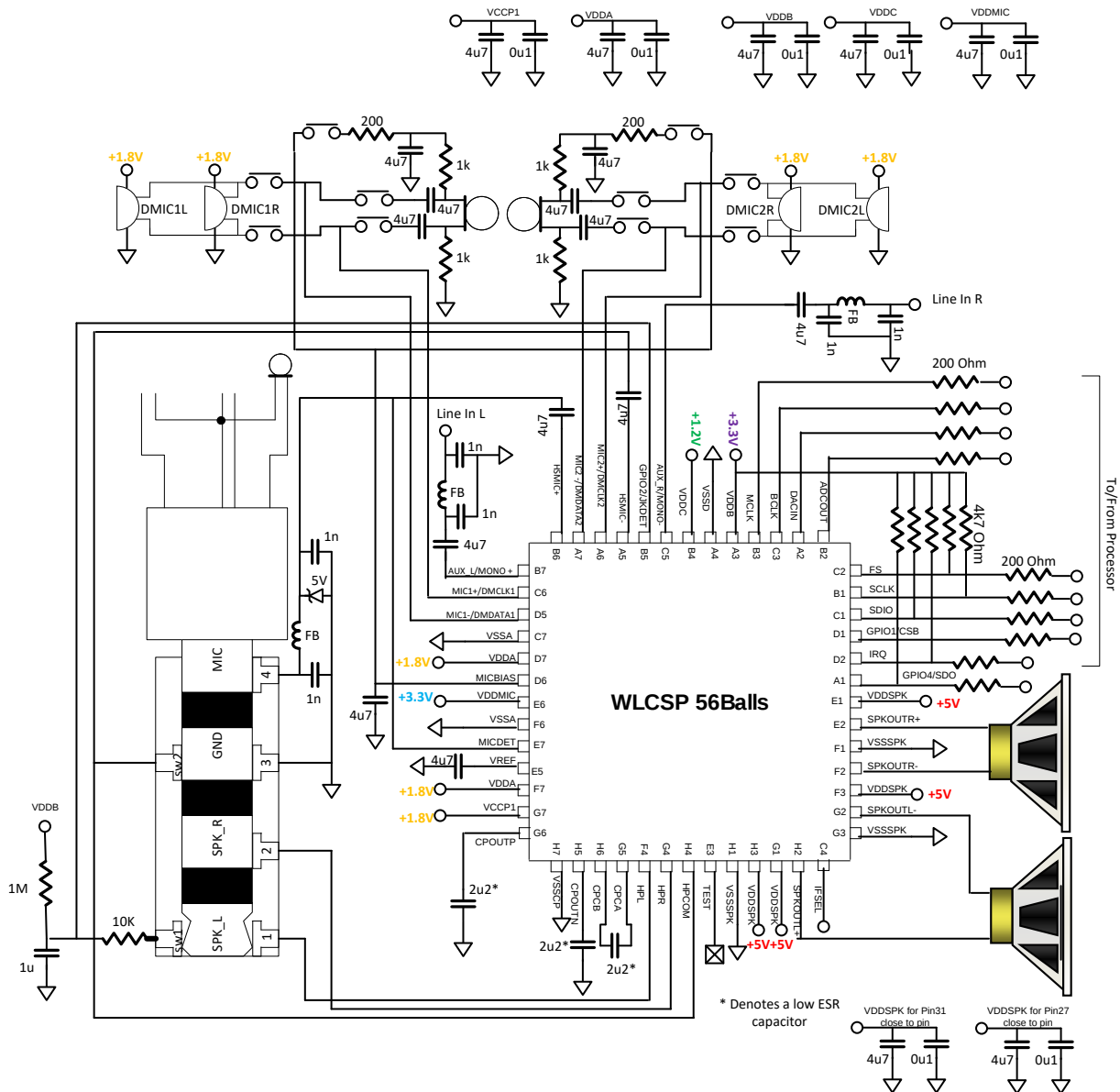
13 Typical Application Diagram

QFN package



NOTE: 1. SDCLK and SDIO can add a low pass filter as show above, the low pass filter cut off frequency range is from 8MHz to 33MHz depending on PCB parasitics.

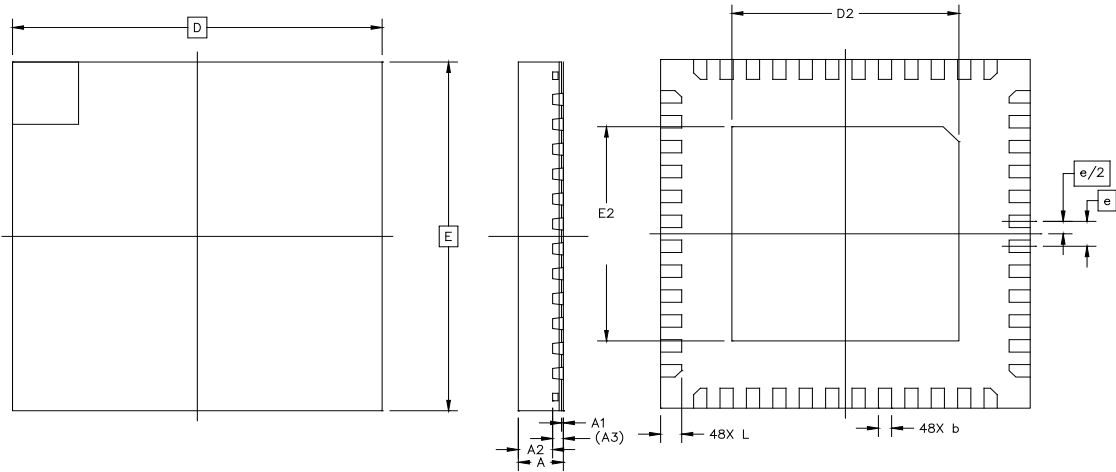
WLCSP package



14 Package Information

14.1 QFN 48L 7X7MM^2

QFN 48L 7X7 MM^2, Thickness: 0.9 MM (Saw type)

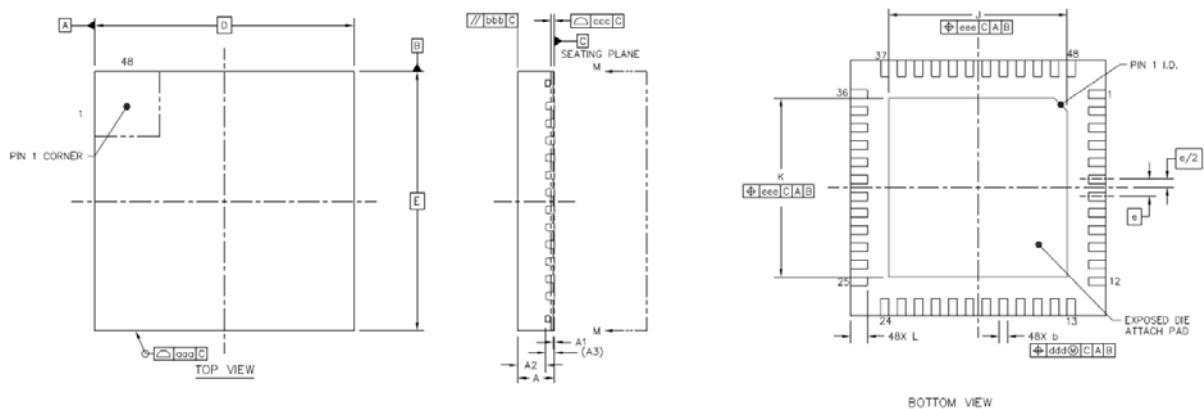


COPLANARITY	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.8	0.85	0.90
STAND OFF	A1	0.00	0.04	0.05
MOLD THICKNESS	A2	---	0.65	0.67
L/F THICKNESS	A3	0.203 REF		
LEAD WIDTH	b	0.20	0.25	0.30
BODY SIZE	D	7.0 BSC		
	E	7.0 BSC		
LEAD PITCH	e	0.5 BSC		
LEAD LENGTH	L	0.30	0.40	0.50
PACKAGE EDGE TOLERANCE	aaa	0.10		
MOLD FLATNESS	bbb	0.10		
COPLANARITY	ccc	0.08		
LEAD OFFSET	ddd	0.10		
EXPOSED PAD OFFSET	eee	0.10		

L/F Pad Size	D2			E2			
	MIN.	NOR.	MAX.	MIN.	NOR.	MAX.	
	2.82	2.97	3.12	2.82	2.97	3.12	S
	3.29	3.44	3.59	3.29	3.44	3.59	S
	5.20	5.30	5.40	5.20	5.30	5.40	AC
	4.20	4.30	4.40	4.20	4.30	4.40	AC

14.2 QFN48L 6x6MM^2

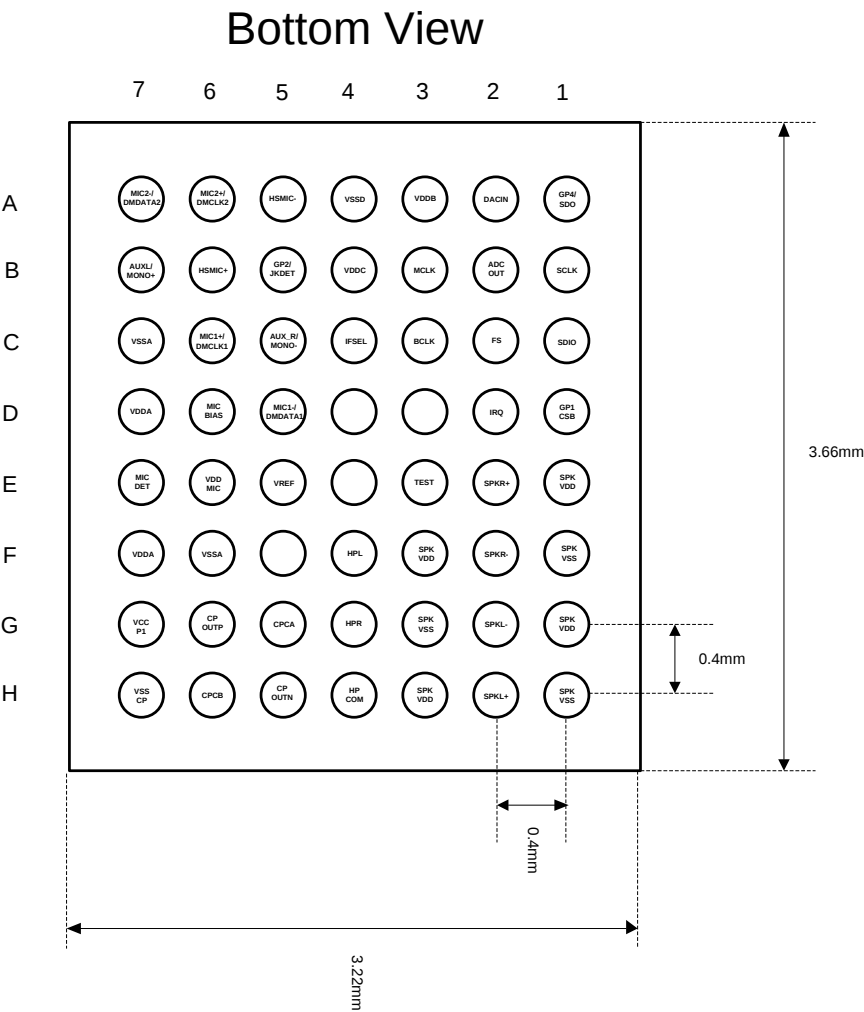
QFN 48L 6X6 MM^2, Thickness: 0.9 mm (Max) Pitch 0.4mm



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	6 BSC		
	Y	E	6 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	J	4.1	4.2	4.3
	Y	K	4.1	4.2	4.3
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		bbb	0.1		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.1		
EXPOSED PAD OFFSET		eee	0.1		

14.3 WLCSP 56 Balls

56 Balls WLCSP with Pitch 0.4mm



ORDERING INFORMATION

Part Number	Dimension	Package	Package Material
NAU88L24YG	7 x 7 mm	QFN-48	Green
NAU88L24IG	6 X 6 mm	QFN-48	Green
NAU88L24VG	3.22 X 3.66 mm	56 Balls WLCSP	Green

NAU88L24

Package Material:

G = Green Package (Halogen-free, RoHS-compliant) & TSCA-compliant

Package Type:

Y = QFN-48

I = QFN-48

V = WLCSP-56

REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.0	Mar 23, 2016	Initial Release
1.1	Mar 23, 2016	P.17, P.57, p.68 Reg0x1A default setting is 0040 with description P.81, Register 69 VDDb changed to VDDA P.10, 12 Notes described supplies domain for pins P.14, adding HPL&HPR maximum loading capacitance P.86, Reg80 JAMFORCE1,2, JAMNODCLOW
1.2	Oct 12, 2016	P.36, Table 23 LR_DIV correction from 3 bits to 2 bits P.35 Fig.8 changed P.70 Reg0x1E&1F time slot description P.47 Added application note P.37, P38 Fig. 10, FLL equation 1 and example change P.71 Reg0x20 TDM time slot for I2S description P.82 Reg0x67A[3] description
1.3	Feb, 2017	P.81 Reg0x58 I2C Device ID explicitly expressed Removal of YG package
1.4	Mar, 2018	P.24 ADC DRC EXP SLOPE register bit map correction P.22, P28, P29, P33 Add Reg0x1C[7], ADDAP, in ADC, DAC, and DAC mixer note. Application diagram add low pass filter
1.5	Jul, 2019	P.36 & P.82, description for DAC zero crossing with ADC sidetone function
1.6	Oct, 2019	Master mode description in register 0x2[7] and 0x1D[3] P.24 adding ADC output L and R has one sampling time period difference P.89, Correct typical application diagram jack low pass filter connected to VDDA
1.7	Jan, 2020	P. 41-P. 42 Enhanced FLL application note
1.8	Nov 12, 2020	Changed AUX_R position P.2 WLCSP diagram P.10 WLCSP pin description P.80-81 Adding WLCSP pin description at REG0x77, REG0x78, REG0x79, REG0x7A
1.9	Mar 10, 2021	P.33 Figure 10 corrected P.23 Table 6 register correction
2.0	Mar 18, 2021	P.58 Reg0x1[11] ADC_OP_off description
2.1	Apr 11, 2022	Update Register Table Format
2.2	Feb 1, 2023	Update Halogen-free, RoHS-compliant and TSCA-compliant description
2.3	July 20, 2023	Update Reg0x79
2.4	Jan 16, 2024	Add note in Electrical Characteristics
2.5	Feb 20, 2024	Update WLCSP G7 description Update SPKOUT+ description Add 4-wire SPI information Add WLCSP application diagram

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