

MAX7219EWG+T-HX/MAX7221EWG+T-HX Serially Interfaced, 8-Digit LED Display Drivers

Description

The MAX7219EWG+T-HX/MAX7221EWG+T-HX are compact, serial input/output common-cathode display drivers designed to interface microprocessors (μ Ps) with 7-segment numeric LED displays of up to 8 digits, bar-graph displays, or 64 individual LEDs. Integrated on-chip features include a BCD code-B decoder, multiplex scan circuitry, segment and digit drivers, as well as an 8x8 static RAM that stores each digit. Only one external resistor is necessary to set the segment current for all LEDs. The MAX7221EWG+T-HX is compatible with SPI™, QSPI™, incorporates slew-rate-limited segment drivers to minimize electromagnetic interference (EMI).

A convenient 4-wire serial interface facilitates connections to all common μ Ps. Individual digits can be addressed and updated without the need to rewrite the entire display. Furthermore, the MAX7219EWG+T-HX/MAX7221EWG+T-HX allows users to select between code-B decoding or no-decoding for each digit.

These devices feature a low-power shutdown mode consuming only 150 μ A, analog and digital brightness control options, a scan-limit register enabling users to display from 1 to 8 digits, as well as a test mode that activates all LEDs simultaneously.

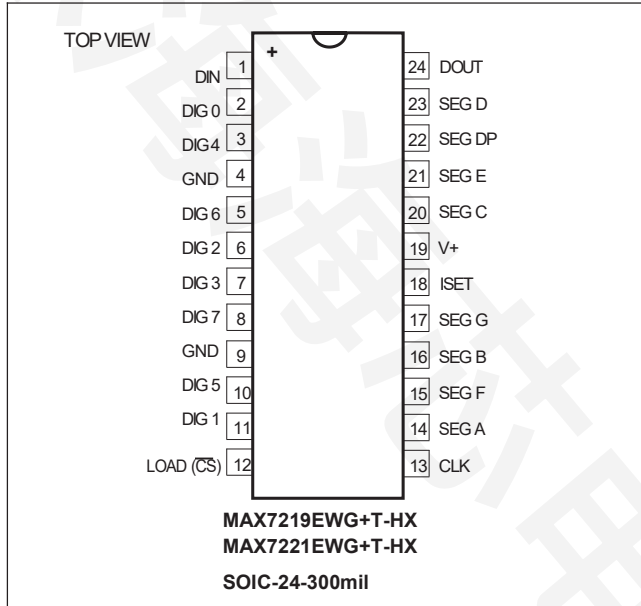
Applications

- ★ Bar-Graph Displays
- ★ Industrial Controllers
- ★ Panel Meters
- ★ LED Matrix Displays

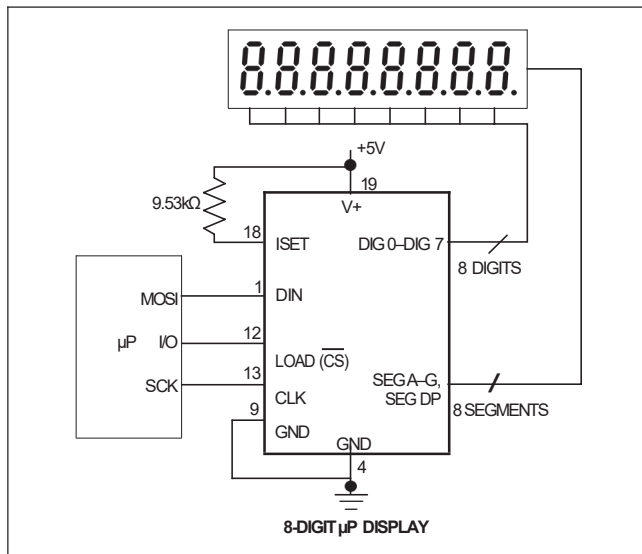
Features

- ★ 10MHz Serial Interface
- ★ Individual LED Segment Control
- ★ Decode/No-Decode Digit Selection
- ★ 150 μ A Low-Power Shutdown (Data Retained)
- ★ Digital and Analog Brightness Control
- ★ Display Blanked on Power-Up
- ★ Drive Common-Cathode LED Display
- ★ Slew-Rate Limited Segment Drivers for Lower EMI (MAX7221EWG+T-HX)
- ★ SPI, QSPI, MICROWIRE Serial Interface (MAX7221EWG+T-HX)
- ★ SOIC-24-300mil Package

Pin Configuration



Typical Application Circuit



Absolute Maximum Ratings

Voltage (with respect to GND)	
V+	-0.3V to 6V
DIN, CLK, LOAD, $\overline{CS}$	-0.3V to 6V
All Other Pins	-0.3V to (V+ + 0.3V)
Current	
DIG 0–DIG 7 Sink Current	500mA
SEG A–G, DP Source Current	100mA
Operating Temperature Ranges (T MIN to T MAX)	
MAX7219C_G/MAX7221C_G	0°C to +70°C
MAX7219E_G/MAX7221E_G	-40°C to +85°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V+ = 5V ±10%, RSET = 9.53kΩ ±1%, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+		4.0		5.5	V
Shutdown Supply Current	I+	All digital inputs at V+ or GND, TA = +25°C			150	μA
Operating Supply Current	I+	RSET = open circuit			8	mA
		All segments and decimal point on, ISEG_ = -40mA		330		
Display Scan Rate	fOSC	8 digits scanned	500	800	1300	Hz
Digit Drive Sink Current	IDIGIT	V+ = 5V, VOUT = 0.65V	320			mA
Segment Drive Source Current	ISEG	TA = +25°C, V+ = 5V, VOUT = (V+ - 1V)	-30	-40	-45	mA
Segment Current Slew Rate (MAX7221EWG+T-HX only)	ΔISEG/Δt	TA = +25°C, V+ = 5V, VOUT = (V+ - 1V)	10	20	50	mA/μs
Segment Drive Current Matching	ΔISEG			3.0		%
Digit Drive Leakage (MAX7221EWG+T-HX only)	IDIGIT	Digit off, VDIGIT = V+			-10	μA
Segment Drive Leakage (MAX7221EWG+T-HX only)	ISEG	Segment off, VSEG = 0V			1	μA
Digit Drive Source Current (MAX7219EWG+T-HX-only)	IDIGIT	Digit off, VDIGIT = (V+ - 0.3V)	-2			mA
Segment Drive Sink Current (MAX7219EWG+T-HX only)	ISEG	Segment off, VSEG = 0.3V	5			mA

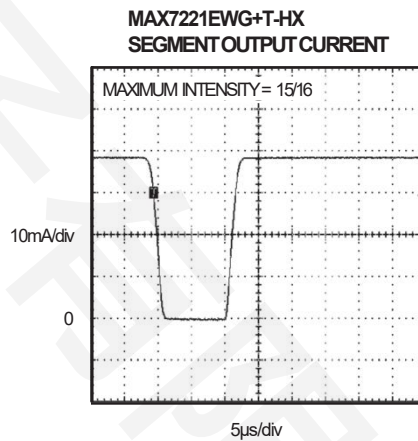
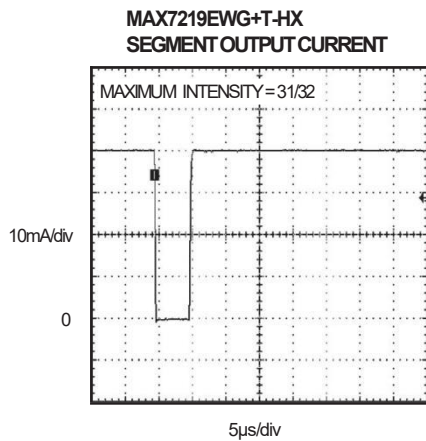
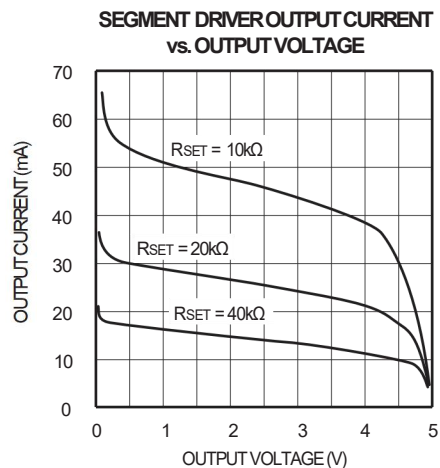
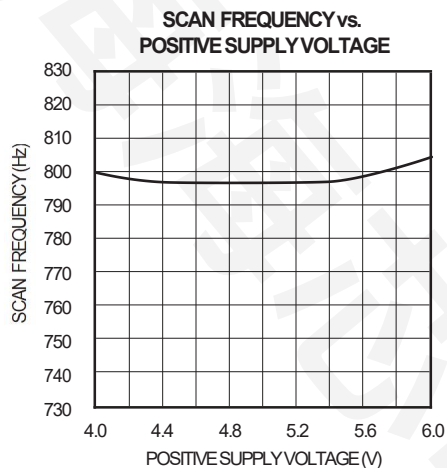
Electrical Characteristics (continued)

(V+ = 5V ±10%, RSET = 9.53kΩ ±1%, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Input Current DIN, CLK, LOAD, CS	I _{IH} , I _{IL}	V _{IN} = 0V or V+	-1		1	μA
Logic High Input Voltage	V _{IH}		3.5			V
Logic Low Input Voltage	V _{IL}				0.8	V
Output High Voltage	V _{OH}	DOUT, I _{SOURCE} = -1mA	V+ - 1			V
Output Low Voltage	V _{OL}	DOUT, I _{SINK} = 1.6mA			0.4	V
Hysteresis Voltage	ΔV _I	DIN, CLK, LOAD, CS		1		V
TIMING CHARACTERISTICS						
CLK Clock Period	t _{CP}		100			ns
CLK Pulse Width High	t _{CH}		50			ns
CLK Pulse Width Low	t _{CL}		50			ns
CS Fall to SCLK Rise Setup Time (MAX7221EWG+T-HX only)	t _{CSS}		25			ns
CLK Rise to CS or LOAD Rise Hold Time	t _{CSH}		0			ns
DIN Setup Time	t _{DS}		25			ns
DIN Hold Time	t _{DH}		0			ns
Output Data Propagation Delay	t _{DO}	C _{LOAD} = 50pF			25	ns
Load-Rising Edge to Next Clock Rising Edge (MAX7219EWG+T-HX only)	t _{LDCK}		50			ns
Minimum CS or LOAD Pulse High	t _{CSW}		50			ns
Data-to-Segment Delay	t _{DSPD}				2.25	ms

Typical Operating Characteristics

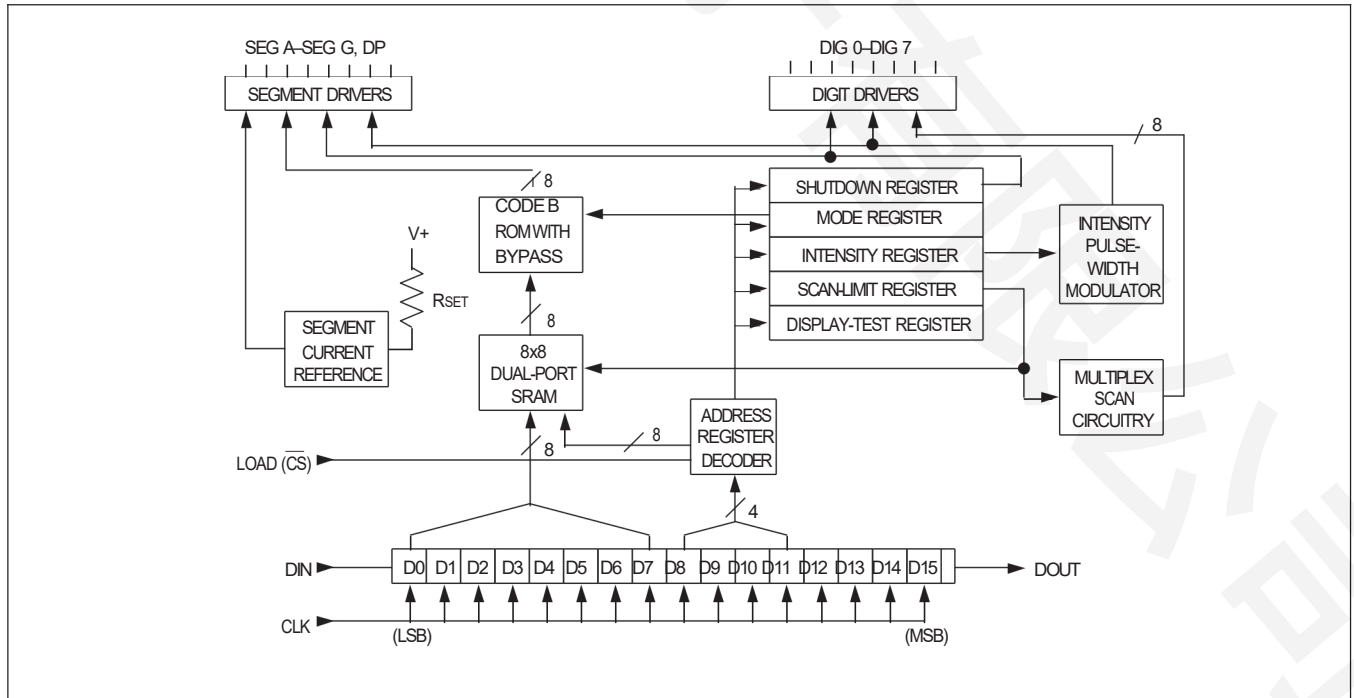
(V+ = +5V, TA = +25°C, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	DIN	Serial-Data Input. Data is loaded into the internal 16-bit shift register on CLK's rising edge.
2, 3, 5-8, 10, 11	DIG 0-DIG 7	Eight-digit drive lines that sink current from the display common cathode. The MAX7219EWG+T-HX pulls the digit outputs to V+ when turned off. The MAX7221EWG+T-HX digit drivers are high-impedance when turned off.
4, 9	GND	Ground. Both GND pins must be connected.
12	LOAD (MAX7219EWG+T-HX)	Load-Data Input. The last 16 bits of serial data are latched on LOAD's rising edge.
	CS (MAX7221EWG+T-HX)	Chip-Select Input. Serial data is loaded into the shift register while CS is low. The last 16 bits of serial data are latched on CS's rising edge.
13	CLK	Serial-Clock Input. 10MHz maximum rate. On CLK's rising edge, data is shifted into the internal shift register. On CLK's falling edge, data is clocked out of DOUT. On the MAX7221EWG+T-HX, the CLK input is active only while CS is low.
14-17, 20-23	SEGA-SEG G, DP	Seven Segment Drives and Decimal Point Drive that source current to the display. On the MAX7219EWG+T-HX, when a segment driver is turned off it is pulled to GND. The MAX7221EWG+T-HX segment drivers are high-impedance when turned off.
18	ISSET	Connect to VDD through a resistor (RSET) to set the peak segment current (Refer to <i>Selecting RSET Resistor and Using External Drivers</i> section).
19	V+	Positive Supply Voltage. Connect to +5V.
24	DOUT	Serial-Data Output. The data into DIN is valid at DOUT 16.5 clock cycles later. This pin is used to daisy-chain several MAX7219EWG+T-HX/MAX7221EWG+T-HX's and is never high-impedance.

Functional Diagram



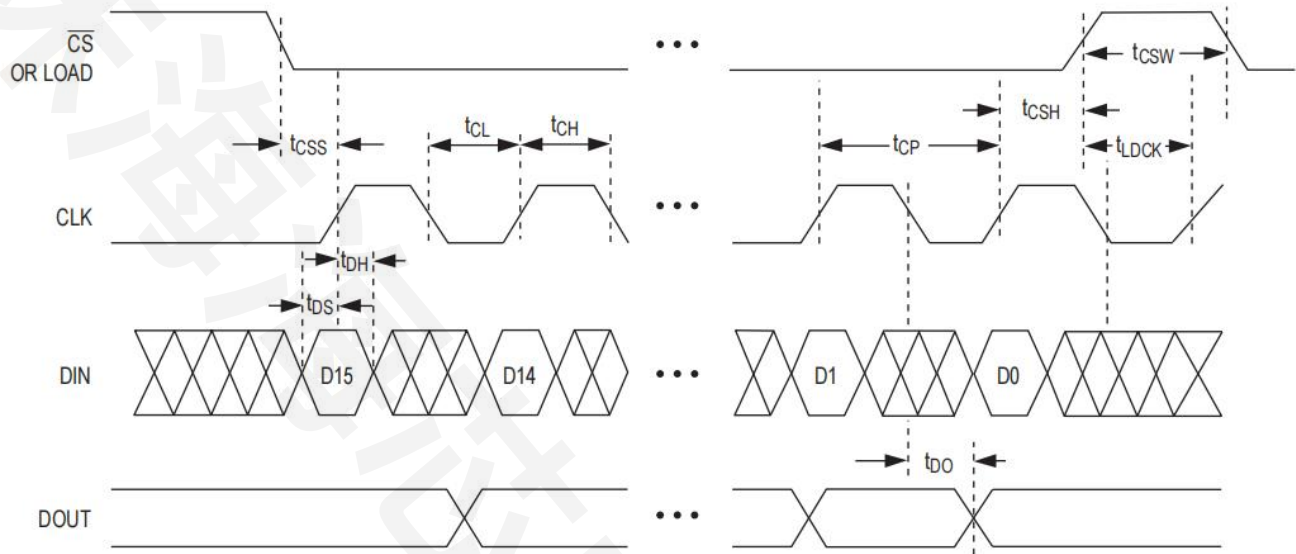


Figure 1. Timing Diagram

Table 1. Serial-Data Format (16 Bits)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	ADDRESS				MSB	DATA						LSB

Detailed Description

MAX7219EWG+T-HX/MAX7221EWG+T-HX Differences

The MAX7219EWG+T-HX/MAX7221EWG+T-HX are identical except for two parameters: the MAX7221EWG+T-HX segment drivers are slew-rate limited to reduce electromagnetic interference (EMI), and its serial interface is fully SPI compatible.

Serial-Addressing Modes

For the MAX7219EWG+T-HX, serial data at DIN, sent in 16-bit packets, is shifted into the internal 16-bit shift register with each rising edge of CLK regardless of the state of LOAD. For the MAX7221EWG+T-HX, CS must be low to clock data in or out. The data is then latched into either the digit or control registers on the rising edge of LOAD/CS. LOAD/CS must go high concurrently with or after the 16th rising clock edge, but before the next rising clock edge or data will be lost. Data at DIN is propagated through the shift register and appears at DOUT 16.5 clock cycles later. Data is clocked out on the falling edge of CLK. Data bits are labeled D0–D15 (Table 1). D8–D11 contain the register address. D0–D7 contain the data, and D12–D15 are “don’t care” bits. The first received is D15, the most significant bit (MSB).

Digit and Control Registers

Table 2 lists the 14 addressable digit and control registers. The digit registers are realized with an on-chip, 8x8 dual-port SRAM. They are addressed directly so that individual digits can be updated and retain data as long as V+ typically exceeds 2V. The control registers consist of decode mode, display intensity, scan limit (number of scanned digits), shutdown, and display test (all LEDs on).

Shutdown Mode

When the MAX7219EWG+T-HX is in shutdown mode, the scan oscillator is halted, all segment current sources are pulled to ground, and all digit drivers are pulled to V+, thereby blanking the display. The MAX7221EWG+T-HX is identical, except the drivers are high-impedance. Data in the digit and control registers remains unaltered. Shutdown can be used to save power or as an alarm to flash the display by successively entering and leaving shutdown mode. For minimum supply current in shutdown mode, logic inputs should be at ground or V+ (CMOS-logic levels).

Typically, it takes less than 250 μ s for the MAX7219EWG+T-HX/MAX7221EWG+T-HX to leave shutdown mode. The display driver can be programmed while in shutdown mode, and shutdown mode can be overridden by the display-test function.

Table 2. Register Address Map

REGISTER	ADDRESS					HEX CODE
	D15-D12	D11	D10	D9	D8	
No-Op	X	0	0	0	0	0xX0
Digit 0	X	0	0	0	1	0xX1
Digit 1	X	0	0	1	0	0xX2
Digit 2	X	0	0	1	1	0xX3
Digit 3	X	0	1	0	0	0xX4
Digit 4	X	0	1	0	1	0xX5
Digit 5	X	0	1	1	0	0xX6
Digit 6	X	0	1	1	1	0xX7
Digit 7	X	1	0	0	0	0xX8
Decode Mode	X	1	0	0	1	0xX9
Intensity	X	1	0	1	0	0xXA
Scan Limit	X	1	0	1	1	0xXB
Shutdown	X	1	1	0	0	0xXC
Display Test	X	1	1	1	1	0xFF

Initial Power-Up

On initial power-up, all control registers are reset, the display is blanked, and the MAX7219EWG+T-HX/MAX7221EWG+T-HX enter shutdown mode. Program the display driver prior to display use. Otherwise, it will initially be set to scan one digit, it will not decode data in the data registers, and the intensity register will be set to its minimum value.

Decode-Mode Register

The decode-mode register sets BCD code B (0-9, E, H, L, P, and -) or no-decode operation for each digit. Each bit in the register corresponds to one digit. A logic high selects code B decoding while logic low bypasses the decoder. Examples of the decode mode control-register format are shown in Table 4.

When the code B decode mode is used, the decoder looks only at the lower nibble of the data in the digit registers (D3-D0), disregarding bits D4-D6. D7, which sets the decimal point (SEG DP), is independent of the decoder and is positive logic (D7 = 1 turns the decimal point on). Table 5 lists the code B font.

When no-decode is selected, data bits D7-D0 correspond to the segment lines of the MAX7219EWG+T-HX/MAX7221EWG+T-HX. Table 6 shows the one-to-one pairing of each data bit to the appropriate segment line.

Table 3. Shutdown Register Format (Address (Hex) = 0xXC)

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Shutdown Mode	0xXC	X	X	X	X	X	X	X	X
Normal Operation	0xXC	X	X	X	X	X	X	X	1

Table 4. Decode-Mode Register Examples (Address (Hex) = 0xX9)

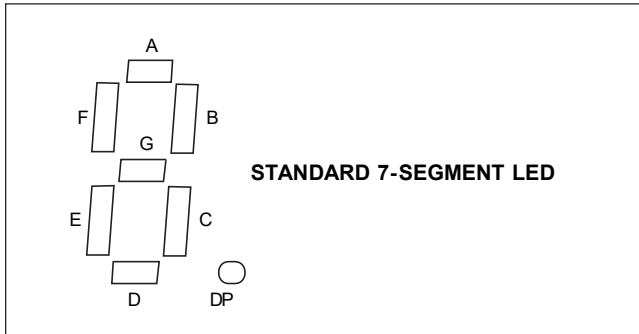
DECODE MODE	REGISTER DATA								HEX CODE
	D7	D6	D5	D4	D3	D2	D1	D0	
No decode for digits 7-0	0	0	0	0	0	0	0	0	0x00
Code B decode for digit 0 No decode for digits 7-1	0	0	0	0	0	0	0	1	0x01
Code B decode for digits 3-0 No decode for digits 7-4	0	0	0	0	1	1	1	1	0x0F
Code B decode for digits 7-0	1	1	1	1	1	1	1	1	0xFF

Table 5. Code B Font

7-SEGMENT CHARACTER	REGISTER DATA						ON SEGMENTS = 1							
	D7*	D6–D4	D3	D2	D1	D0	DP*	A	B	C	D	E	F	G
0		X	0	0	0	0		1	1	1	1	1	1	0
1		X	0	0	0	1		0	1	1	0	0	0	0
2		X	0	0	1	0		1	1	0	1	1	0	1
3		X	0	0	1	1		1	1	1	1	0	0	1
4		X	0	1	0	0		0	1	1	0	0	1	1
5		X	0	1	0	1		1	0	1	1	0	1	1
6		X	0	1	1	0		1	0	1	1	1	1	1
7		X	0	1	1	1		1	1	1	0	0	0	0
8		X	1	0	0	0		1	1	1	1	1	1	1
9		X	1	0	0	1		1	1	1	1	0	1	1
—		X	1	0	1	0		0	0	0	0	0	0	1
E		X	1	0	1	1		1	0	0	1	1	1	1
H		X	1	1	0	0		0	1	1	0	1	1	1
L		X	1	1	0	1		0	0	0	1	1	1	0
P		X	1	1	1	0		1	1	0	0	1	1	1
blank		X	1	1	1	1		0	0	0	0	0	0	0

*The decimal point is set by bit D7 = 1

Table 6. No-Decode Mode Data Bits and Corresponding Segment Lines



	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Corresponding Segment Line	DP	A	B	C	D	E	F	G

Intensity Control and Interdigit Blanking

The MAX7219EWG+T-HX/MAX7221EWG+T-HX allow display brightness to be controlled with an external resistor (RSET) connected between V+ and ISET. The peak current sourced from the segment drivers is nominally 100 times the current entering ISET. This resistor can either be fixed or variable to allow brightness adjustment from the front panel. Its minimum value should be 9.53kΩ, which typically sets the segment current at 40mA. Display brightness can also be controlled digitally by using the intensity register.

Digital control of display brightness is provided by an internal pulse-width modulator, which is controlled by the lower nibble of the intensity register. The modulator scales the average segment current in 16 steps from a maximum of 31/32 down to 1/32 of the peak current set by RSET (15/16 to 1/16 on MAX7221EWG+T-HX). Table 7 lists the intensity register format. The minimum interdigit blanking time is set to 1/32 of a cycle.

Table 7. Intensity Register Format (Address (Hex) = 0xBA)

DUTY CYCLE		D7	D6	D5	D4	D3	D2	D1	D0	HEX CODE
MAX7219EWG+T-HX	MAX7221EWG+T-HX									
1/32 (min on)	1/16 (min on)	X	X	X	X	0	0	0	0	0x0
3/32	2/16	X	X	X	X	0	0	0	1	0x1
5/32	3/16	X	X	X	X	0	0	1	0	0x2
7/32	4/16	X	X	X	X	0	0	1	1	0x3
9/32	5/16	X	X	X	X	0	1	0	0	0x4
11/32	6/16	X	X	X	X	0	1	0	1	0x5
13/32	7/16	X	X	X	X	0	1	1	0	0x6
15/32	8/16	X	X	X	X	0	1	1	1	0x7
17/32	9/16	X	X	X	X	1	0	0	0	0x8
19/32	10/16	X	X	X	X	1	0	0	1	0x9
21/32	11/16	X	X	X	X	1	0	1	0	0xA
23/32	12/16	X	X	X	X	1	0	1	1	0xB
25/32	13/16	X	X	X	X	1	1	0	0	0xC
27/32	14/16	X	X	X	X	1	1	0	1	0xD
29/32	15/16	X	X	X	X	1	1	1	0	0xE
31/32	15/16 (max on)	X	X	X	X	1	1	1	1	0xF

Table 8. Scan-Limit Register Format (Address (Hex) = 0xBB)

SCAN LIMIT	REGISTER DATA								HEX CODE
	D7	D6	D5	D4	D3	D2	D1	D0	
Display digit 0 only*	X	X	X	X	X	0	0	0	0x0
Display digits 0 & 1*	X	X	X	X	X	0	0	1	0x1
Display digits 0 1 2*	X	X	X	X	X	0	1	0	0x2
Display digits 0 1 2 3	X	X	X	X	X	0	1	1	0x3
Display digits 0 1 2 3 4	X	X	X	X	X	1	0	0	0x4
Display digits 0 1 2 3 4 5	X	X	X	X	X	1	0	1	0x5
Display digits 0 1 2 3 4 5 6	X	X	X	X	X	1	1	0	0x6
Display digits 0 1 2 3 4 5 6 7	X	X	X	X	X	1	1	1	0x7

*See Scan-Limit Register section for application.

Scan-Limit Register

The scan-limit register sets how many digits are displayed, from 1 to 8. They are displayed in a multiplexed manner with a typical display scan rate of 800Hz with 8 digits displayed. If fewer digits are displayed, the scan rate is

$8f_{OSC}/N$, where N is the number of digits scanned. Since the number of scanned digits affects the display brightness, the scan-limit register should not be used to blank portions of the display (such as leading zero suppression). Table 8 lists the scan-limit register format.

If the scan-limit register is set for three digits or less, individual digit drivers will dissipate excessive amounts of power. Consequently, the value of the RSET resistor must be adjusted according to the number of digits displayed, to limit individual digit driver power dissipation. Table 9 lists the number of digits displayed and the corresponding maximum recommended segment current when the digit drivers are used.

Display-Test Register

The display-test register operates in two modes: normal and display test. Display-test mode turns all LEDs on by overriding, but not altering, all controls and digit registers (including the shutdown register). In display-test mode, 8 digits are scanned and the duty cycle is 31/32 (15/16 for MAX7219EWG+T-HX). Table 10 lists the display-test register format.

Table 9. Maximum Segment Current for 1-, 2-, or 3-Digit Displays

NUMBER OF DIGITS DISPLAYED	MAXIMUM SEGMENT CURRENT (mA)
1	10
2	20
3	30

Table 10. Display-Test Register Format (Address (Hex) = 0xXF)

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Normal Operation	X	X	X	X	X	X	X	0
Display Test Mode	X	X	X	X	X	X	X	1

Note: The MAX7219EWG+T-HX/MAX7221EWG+T-HX remain in display-test mode (all LEDs on) until the display-test register is reconfigured for normal operation.

No-Op Register

The no-op register is used when cascading MAX7219EWG+T-HX's or MAX7221EWG+T-HX's. Connect all devices' LOAD/CS inputs together and connect DOUT to DIN on adjacent devices. DOUT is a CMOS logic-level output that easily drives DIN of successively cascaded parts. (Refer to the *Serial Addressing Modes* section for detailed information on serial input/output timing.) For example, if four MAX7219EWG+T-HX's

are cascaded, then to write to the fourth chip, sent the desired 16-bit word, followed by three no-op codes (hex 0x00, see Table 2). When LOAD/CS goes high, data is latched in all devices. The first three chips receive no-op commands, and the fourth receives the intended data.

Applications Information

Supply Bypassing and Wiring

To minimize power-supply ripple due to the peak digit driver currents, connect a 10 μ F electrolytic and a 0.1 μ F ceramic capacitor between V+ and GND as close to the device as possible. The MAX7219EWG+T-HX/MAX7221EWG+T-HX should be placed in close proximity to the LED display, and connections should be kept as short as possible to minimize the effects of wiring inductance and electro-magnetic interference. Also, both GND pins must be connected to ground.

Selecting RSET Resistor and Using External Drivers

The current per segment is approximately 100 times the current in ISET. To select RSET, see Table 11. The MAX7219EWG+T-HX/MAX7221EWG+T-HX's maximum recommended segment current is 40mA. For segment current levels above these levels, external digit drivers will be needed. In this application, the MAX7219EWG+T-HX/MAX7221EWG+T-HX serve only as controllers for other high-current drivers or transistors. Therefore, to conserve power, use RSET = 47k Ω when using external current sources as segment drivers.

The example in Figure 2 uses the MAX7219EWG+T-HX/MAX7221EWG+T-HX's segment drivers, a MAX394 single-pole double-throw analog switch, and external transistors to drive 2.3" AND2307SLC common-cathode displays. The 5.6V zener diode has been added in series with the decimal point LED because the decimal point LED forward voltage is typically 4.2V. For all other segments the LED forward voltage is typically 8V. Since external transistors are used to sink current (DIG 0 and DIG 1 are used as logic switches), peak segment currents of 45mA are allowed even though only two digits are displayed. In applications where the MAX7219EWG+T-HX/MAX7221EWG+T-HX's digit drivers are used to sink current and fewer than four digits are displayed, Table 9 specifies the maximum allowable segment current. RSET must be selected accordingly (Table 11). Refer to the *Continuous Power Dissipation* section of the *Absolute Maximum Ratings* to calculate acceptable limits for ambient temperature, segment current, and the LED forward-voltage drop.

Table 11. RSET vs. Segment Current and LED Forward Voltage

ISEG (mA)	VLED (V)				
	1.5	2.0	2.5	3.0	3.5
40	12.2	11.8	11.0	10.6	9.69
30	17.8	17.1	15.8	15.0	14.0
20	29.8	28.0	25.9	24.5	22.6
10	66.7	63.7	59.3	55.4	51.2

Note: RSET values are in Kilo Ohms (kΩ)

Computing Power Dissipation

The upper limit for power dissipation (PD) for the MAX7219EWG+T-HX/MAX7221EWG+T-HX is determined from the following equation:

$$PD = (V+ \times 8mA) + (V+ - VLED)(DUTY \times ISEG \times N)$$

where:

V+ = supply voltage

DUTY = duty cycle set by intensity register

N = number of segments driven (worst case is 8)

VLED = LED forward voltage

ISEG = segment current set by RSET

Dissipation example:

ISEG = 40mA, N = 8, DUTY = 31/32, VLED = 1.8V at

40mA, V+ = 5.25V

$$PD = (5.25V \times 8mA) + (5.25V - 1.8V)(31/32 \times 40mA \times 8) = 1.11W$$

Table 12. Package Thermal Resistance Data

PACKAGE	THERMAL RESISTANCE (θJA)
Maximum Junction Temperature (TJ) = +150. C	
Maximum Ambient Temperature (TA) = +85. C	

Cascading Drivers

The example in Figure 3 drives 16 digits using a 3-wire μP interface. If the number of digits is not a multiple of 8, set both drivers' scan limits registers to the same number so one display will not appear brighter than the other. For example, if 12 digits are need, use 6 digits per display with both scan-limit registers set for 6 digits so that both displays have a 1/6 duty cycle per digit. If 11 digits are needed, set both scan-limit registers for 6 digits and leave one digit driver unconnected. If one display for 6 digits and the other for 5 digits, the second display will appear brighter because its duty cycle per digit will be 1/5 while the first display' s will be 1/6. Refer to the *No-Op Register* section for additional information.

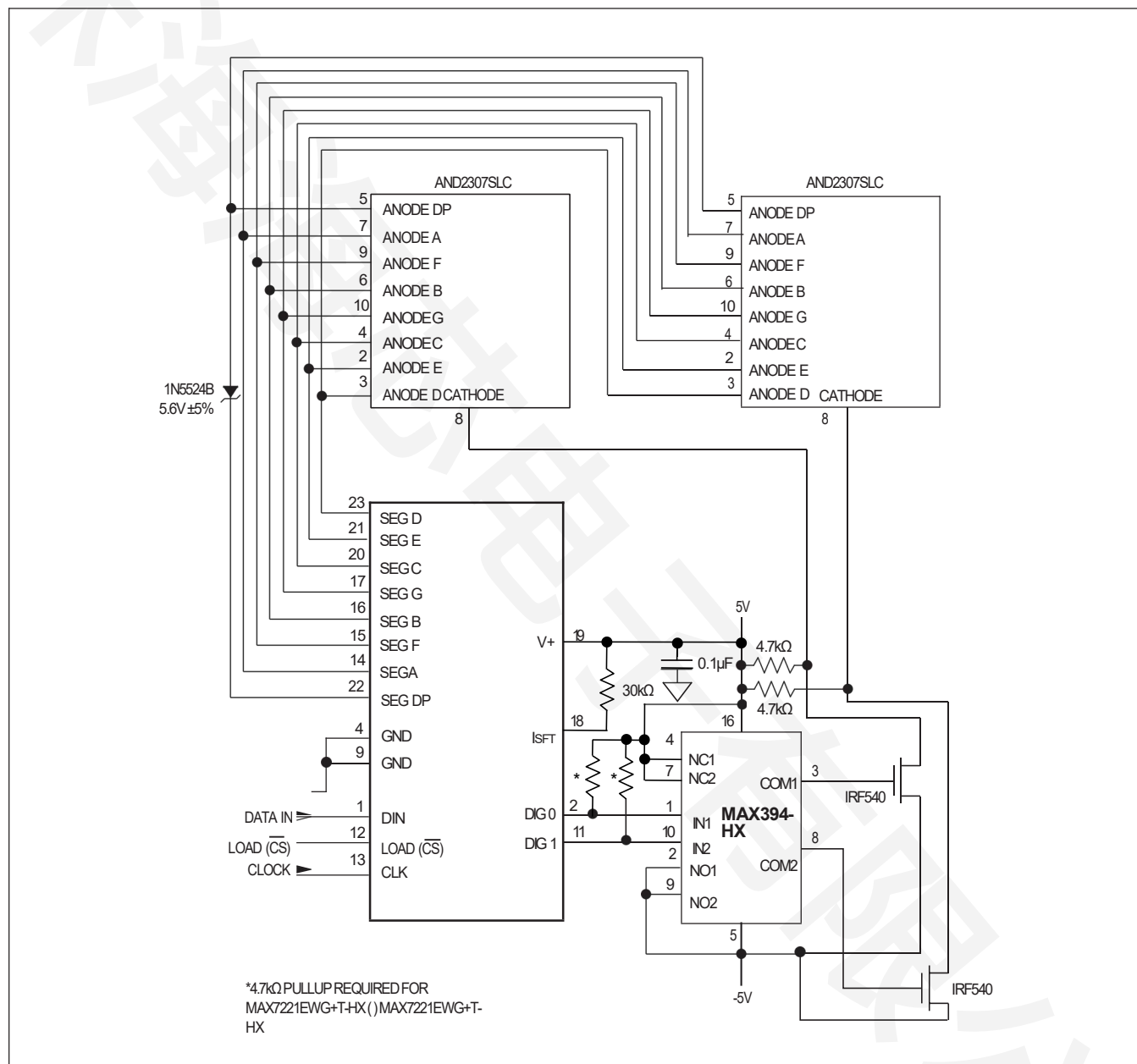


Figure 2. MAX7219EWG+T-HX/MAX7221EWG+T-HX Driving 2.3in Displays

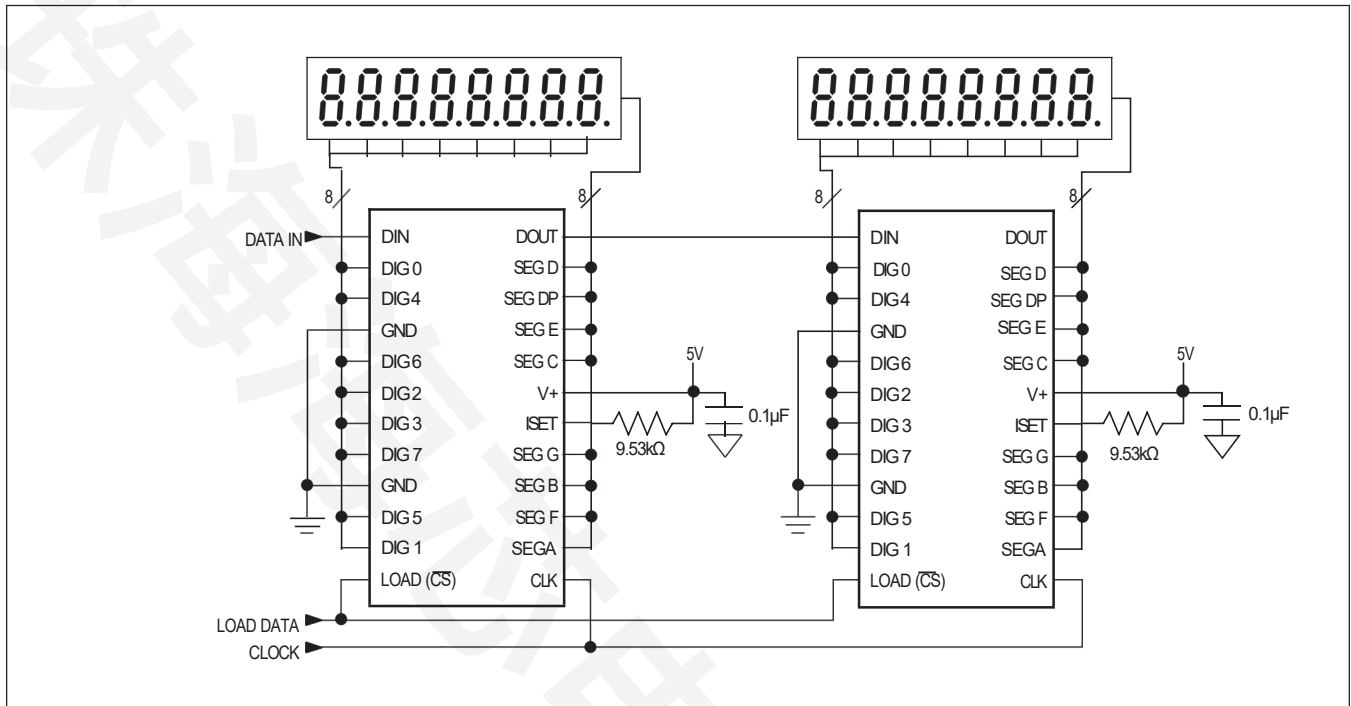


Figure 3. Cascading MAX7219EWG+T-HX/MAX7221EWG+T-HXs to Drive 16 Seven-Segment LED Digits