3-Channel 24/16-bit Sigma-Delta ADC with PGA

FEATURES

Programmable Gain: 1/2/4/8/16/32/64/128
Data Rates: 4.17SPS to 890SPS
RMS Noise:
- **20nV at 4.17SPS (Gain=128)**
- **63nV at 16.7SPS (Gain=128)**
- **21.0 noise-free bits at 4.17SPS (Gain=1)**

Offset Drift: 5nV/°C (Gain=128)
Gain Drift: 1ppm/°C
Integral Non-Linearity: 2ppm
3 Differential Inputs
Simultaneous 50Hz/60Hz Rejection
Reference Detect
Burnout Current Sources
Low-Side Power Switch
Power Supply
- **AVDD: 2.7V to 5.25V**
- **DVDD: 2.7V to 5.25V**

Current: 470μA
Package: 16-lead TSSOP

APPLICATIONS

Weigh Scales
Strain Gauges
Temperature Measurement
Industrial Process Control
Pressure Sensors

DESCRIPTION

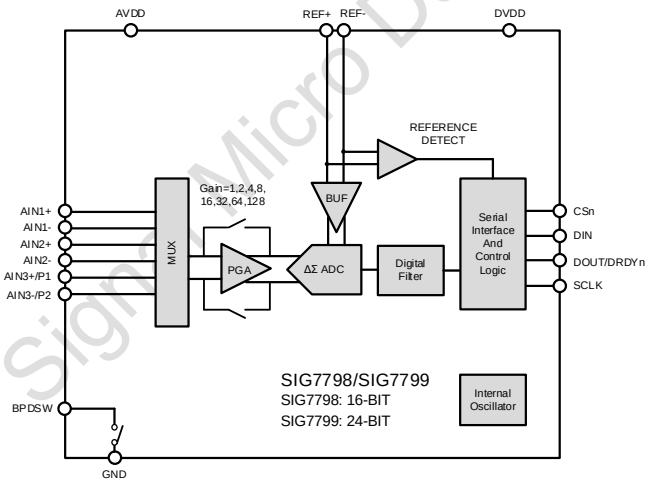
The SIG7798/7799 are low noise, low drift, and high-resolution 16/24-bit analog-to-digital converter (ADC) with integrated programmable gain amplifier (PGA) that offers high-accuracy measurement solutions for bridge sensors, thermocouples, and resistance temperature devices (RTD).

The device contains a low noise PGA with gains selected from 1, 2, 4, 8 16, 32, 64, and 128, a delta-sigma (Δ-Σ) modulator, and digital filter. The output data rate from the device can be configured from 4.17SPS up to 890SPS. 50Hz/60Hz simultaneous rejection option is also provided. Burnout current sources are provided at the analog inputs for sensor connection diagnosis.

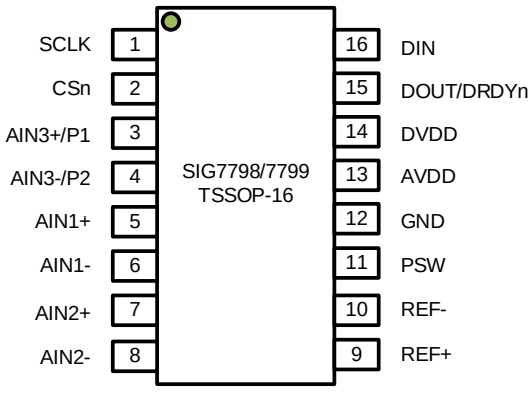
Offset and gain calibration registers are provided with calibration command or direct register write to calibrate the ADC errors or overall system errors. SPI-compatible interface is used for device configuration.

The SIG7798/7799 are available in 16-lead TSSOP packages and are fully specified over the -40℃ to +125℃ temperature range.

Function Block Diagram

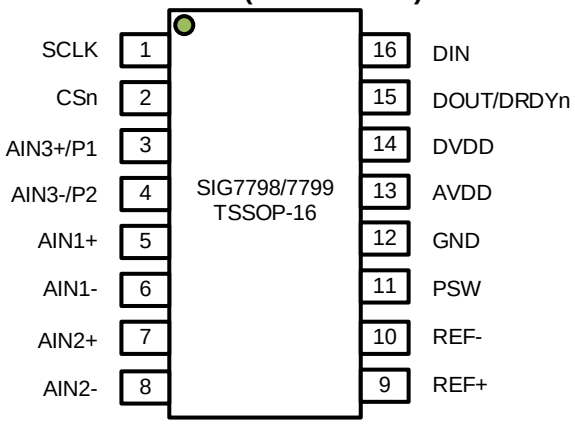


TSSOP-16



PIN CONFIGURATION and DESCRIPTIONS

TOP VIEW (Not To Scale)



PIN		FUNCTION	DESCRIPTION
NO.	NAME		
1	SCLK	Digital Input	Serial data clock.
2	CSn	Digital Input	Serial chip select. Active low.
3	AIN3+/P1	Analog Input/Output	Analog positive input channel 3 or general purpose output 1 between AVDD and GND.
4	AIN3-/P2	Analog Input/Output	Analog negative input channel 3 or general purpose output 2 between AVDD and GND.
5	AIN1+	Analog Input	Analog positive input channel 1.
6	AIN1-	Analog Input	Analog negative input channel 1.
7	AIN2+	Analog Input	Analog positive input channel 2.
8	AIN2-	Analog Input	Analog negative input channel 2.
9	REF+	Analog Input	Positive reference input.
10	REF-	Analog Input	Negative reference input.
11	PSW	Analog Input	Low-side Power switch to GND.
12	GND	Analog	Ground reference point.
13	AVDD	Analog	Positive analog power supply. 2.7V to 5.25V relative to GND. AVDD is independent of DVDD.
14	DVDD	Digital	Digital power supply, 2.7V to 5.25V. DVDD is independent of AVDD.
15	DOUT/DRDYn	Digital Output	Serial data output and data ready indicator.
16	DIN	Digital Input	Serial data input.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKING OPTION
SIG7798	TSSOP-16	-40°C to +125°C	SIG7798-ITSP16-RL	Reel, 5000
SIG7799	TSSOP-16	-40°C to +125°C	SIG7799-ITSP16-RL	Reel, 5000

SPECIFICATIONS

Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage	AVDD to GND	–0.3	6.5	V
	DVDD to GND	–0.3	6.5	V
	Analog input	–0.3	V_{AVDD} + 0.3	V
	Digital input	–0.3	V_{DVDD} + 0.3	V
Current	Input current	–10	10	mA
Temperature	Junction (T_J)	–50	150	°C
	Storage (T_{stg})	-60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

SYMBOL	PARAMTER	CONDITION	VALUE	UNIT
HBM	Human-body Model	ANSI/ESDA/JEDEC JS-001	±6000	V
CDM	Charged-device model	JEDEC EIA/JS-002-2022	±2000	V

This integrated circuit can be damaged by ESD. Signal Micro recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Electrical Characteristics

Minimum/Maximum specifications apply from -40˚C to +125˚C. Typical specifications are at +25˚C. All specification are at V_{AVDD}=5V, V_{DVDD}=3.3V, V_{GND} =0V, V_{REF}=2.5V, f_{CLK}=1.024MHz, data rate=16.7SPS, and PGA Gain=1, unless otherwise noted.

PARAMETER	TEST CONDITION OR NOTES	MIN(1)	TYP	MAX(1)	UNITS
ANALOG INPUTS					
Differential Input Voltage	$V_{IN} = V_{INP} – V_{INN}$	$–V_{REF}$/Gain		$+V_{REF}$/Gain	V
Absolute Input Voltage	Buffer Off	– 0.05		V_{AVDD} + 0.05	V
	Buffer On	+ 0.2		V_{AVDD} – 0.2	
Common Mode Input Range	Buffer On	0.2 + $\lvert V_{INMAX}\rvert$·Gain/2		V_{AVDD} – 0.2 – $\lvert V_{INMAX}\rvert$·Gain/2	V
Absolute Input Current	Buffer Off		±10		nA
	Buffer On		±1		nA
SYSTEM PERFORMANCE					
PGA Gain			1/2/4/8/16/32/64/128		V/V
Resolution	SIG7798		16		Bits
	SIG7799		24		Bits
Data Rate		4.17		890	SPS
Noise		See Noise Table			
Integral Nonlinearity (INL)	Buffer Off		±10		ppm
	Buffer On		±2		ppm
Offset Error	Chop Off		±400/Gain		µV
	Chop On		±1		µV
Offset Drift vs. Temperature	All PGA gains		±400/Gain ± 2		nV/°C
Gain Error(2)	All PGA gains	-500	±100	500	ppm
Gain Mismatch(2)	All PGA gains		150	350	ppm
Gain Drift vs. Temperature	All PGA gains	-3	±1	+3	ppm/°C
Normal Mode Rejection (NMRR)	f_{IN} = 50/60Hz, ±2%, data rate=16.7SPS		See Table 15		dB
Common Mode Rejection (CMRR)	f_{IN} = 50Hz, data rate = 470SPS	100	120		dB
Power Supply Rejection (PSRR)	AVDD	85	105		dB
	DVDD	90	110		dB
EXTERNAL REFERENCE INPUTs					
Differential Reference Voltage (V_{REF})	$V_{REF} = V_{REFP} – V_{REFN}$	0.5	2.5	V_{AVDD} + 0.1	V
Absolute Negative Reference Voltage (V_{REFN})		– 0.05		V_{REFP} – 0.5	V
Absolute Positive Reference Voltage (V_{REFP})		V_{REFN} + 0.5		V_{AVDD} + 0.05	V
Average Voltage Input Current			±1		µA
Burnout Current Sources					
Current Setting			0.5		µA
ADC CLOCK					
Internal Oscillator	Nominal Frequency		1.024		MHz
	Accuracy	–3%	±0.5%	3%	
DIGITAL INPUT/OUTPUT					
High-level Output Voltage (V_{OH})	I_{OH} = 4mA	0.8·V_{DVDD}			V
Low-level Output Voltage (V_{OL})	I_{OL} = –4mA			0.2·V_{DVDD}	V
High-level Input Voltage (V_{IH})		0.7·V_{DVDD}		V_{DVDD}	V
Low-level Input Voltage (V_{IL})		0		0.3·V_{DVDD}	V
Input Hysteresis			0.5		V
Input Leakage				±10	µA
POWER SUPPLY					

AVDD Voltage (V_{AVDD})		2.7		5.25	V
DVDD Voltage (V_{DVDD})		2.7		5.25	V
AVDD Current (I_{AVDD})	Buffer Off		150	200	µA
	Buffer On		350	450	µA
	Sleep Mode		1		µA
DVDD Current (I_{DVDD})	Active Mode		120	200	µA
	Sleep Mode		20		µA
Total Power Dissipation	Buffer Off		1.15		mW
	Buffer On		2.15		mW
	Sleep Mode		0.10		mW
TEMPERATURE RANGE					
Specified temperature range		–40		125	°C
Operating temperature range		–50		125	°C
Storage temperature range		–60		150	°C

(1) Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
(2) MIN and MAX values listed for gain error are for +25°C room temperature only.
(3) The IDAC current does not change by more than 0.01% from the nominal value when staying within the specified compliance voltage.

Timing Requirements: Serial Interface

Over the operating ambient temperature range and DVDD = 2.7V to 5.25V, unless otherwise noted.

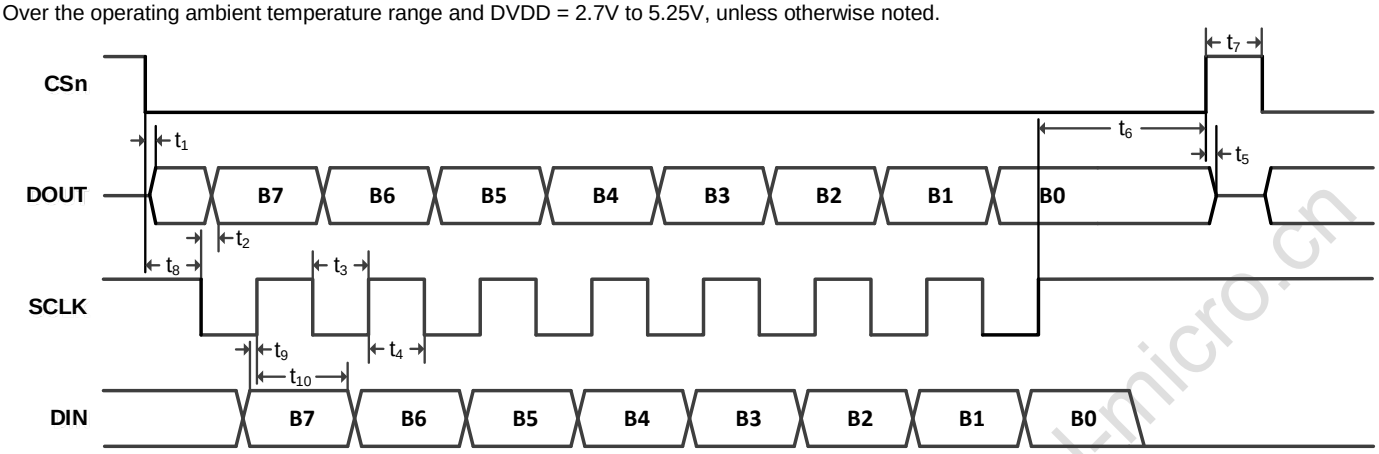


Figure 1. Serial Interface Timing Requirements

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_1	CSn falling edge to DOUT/DRDYn driven: propagation delay(1)		50	ns
t_2	SCLK falling edge to valid DOUT/DRDYn: propagation delay(1)		50	ns
t_3	SCLK low pulse width	100		ns
t_4	SCLK high pulse width	100		ns
	SCLK period	200	10^6	ns
t_5	CSn rising edge to DOUT high impedance: propagation delay		40	ns
t_6	Last SCLK rising edge to CSn rising edge: delay time	50		ns
t_7	CSn high pulse width	50		ns
t_8	CSn falling edge to first SCLK falling edge: setup time(2)	50		ns
t_9	Valid DIN to SCLK rising edge: setup time	50		ns
t_{10}	Valid DIN to SCLK rising edge: hold time	25		ns

(1) DOUT load = 20pF || 100kΩ to GND.
(2) CSn can be tied low.

NOISE PERFORMANCE

The noise performance of the ADC is affected by PGA gain, data rate, and digital filter setting. The following tables show the rms noise and peak-to-peak noise for different data rate with chop enabled. The effective number of bits (ENOB) and noise-free bits are also listed according to Equation (1) and Equation (2):

$$\text{ENOB} = \log_2(2 \times V_{REF} / \text{Gain} / V_{RMS}) \quad (1)$$

$$\text{Noise Free Bits} = \log_2(2 \times V_{REF} / \text{Gain} / V_{p\text{-}p}) \quad (2)$$

The noise data listed in the table are typical and are generated from continuous ADC readings with differential input voltage of 0 V. With chop disabled, the noise increases by 30%.

Table 1. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 2.5 V, Chop Enabled

FS[3:0]	Data Rate (SPS)	PGA GAIN							
		1	2	4	8	16	32	64	128
1111	4.17	0.510(2.10)	0.326(1.46)	0.170(0.872)	0.084(0.412)	0.057(0.236)	0.036(0.165)	0.027(0.115)	0.020(0.095)
1110	6.25	0.658(2.72)	0.420(1.89)	0.220(1.13)	0.109(0.532)	0.073(0.304)	0.047(0.213)	0.035(0.148)	0.026(0.122)
1101	8.33	0.806(3.33)	0.515(2.31)	0.269(1.38)	0.133(0.652)	0.090(0.373)	0.057(0.261)	0.043(0.182)	0.032(0.150)
1100	10	0.931(3.84)	0.595(2.67)	0.311(1.59)	0.154(0.753)	0.103(0.430)	0.066(0.301)	0.049(0.210)	0.036(0.173)
1011	12.5	1.14(4.71)	0.728(3.27)	0.380(1.95)	0.188(0.922)	0.127(0.527)	0.081(0.368)	0.060(0.257)	0.045(0.212)
1010	16.7	1.61(6.66)	1.03(4.62)	0.538(2.76)	0.266(1.30)	0.179(0.745)	0.114(0.521)	0.085(0.363)	0.063(0.300)
1001	16.7	1.56(6.56)	1.00(4.32)	0.522(2.46)	0.245(1.16)	0.177(0.838)	0.111(0.587)	0.081(0.372)	0.063(0.291)
1000	19.6	1.87(9.24)	1.06(6.26)	0.732(2.98)	0.334(1.34)	0.193(1.04)	0.133(0.522)	0.091(0.405)	0.072(0.321)
0111	33.2	2.55(13.7)	1.36(6.56)	0.764(4.47)	0.412(2.20)	0.242(1.27)	0.208(1.04)	0.108(0.536)	0.093(0.449)
0110	39	2.39(10.4)	1.75(7.60)	0.863(3.80)	0.468(2.35)	0.268(1.38)	0.204(0.903)	0.116(0.563)	0.096(0.403)
0101	50	2.70(15.2)	2.11(10.4)	1.06(4.69)	0.664(3.32)	0.354(1.70)	0.265(1.14)	0.157(0.722)	0.120(0.538)
0100	62	3.65(15.8)	2.20(12.1)	1.27(5.81)	0.729(4.17)	0.473(1.99)	0.243(1.09)	0.191(1.02)	0.168(0.687)
0011	123	5.48(29.5)	3.28(19.1)	1.49(8.12)	0.905(4.69)	0.564(3.73)	0.355(1.97)	0.261(1.36)	0.195(1.18)
0010	242	8.90(67.9)	4.82(30.2)	2.37(14.3)	1.48(7.49)	0.721(3.93)	0.488(3.10)	0.358(1.95)	0.287(1.59)
0001	470	22.7(127)	11.7(87.5)	5.98(37.9)	3.14(19.0)	1.55(8.68)	0.943(5.62)	0.583(3.86)	0.421(2.55)
0000	890	236(1360)	112(746)	58.5(395)	28.2(266)	13.6(103)	7.42(49.5)	3.60(24.7)	1.86(12.8)

Table 2. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 2.5 V, Chop Enabled

FS[3:0]	Data Rate (SPS)	PGA GAIN							
		1	2	4	8	16	32	64	128
1111	4.17	23.2(21.0)	22.9(20.7)	22.8(20.5)	22.8(20.5)	22.4(20.3)	22.0(19.9)	21.5(19.4)	20.9(18.7)
1110	6.25	22.8(20.6)	22.5(20.3)	22.4(20.1)	22.5(20.2)	22.0(20.0)	21.7(19.5)	21.1(19.0)	20.5(18.3)
1101	8.33	22.5(20.4)	22.2(20.0)	22.1(19.8)	22.2(19.9)	21.7(19.7)	21.4(19.2)	20.8(18.7)	20.2(18.0)
1100	10	22.3(20.1)	22.0(19.8)	21.9(19.6)	22.0(19.7)	21.5(19.5)	21.2(19.0)	20.6(18.5)	20.0(17.8)
1011	12.5	22.0(19.9)	21.7(19.5)	21.6(19.3)	21.7(19.4)	21.2(19.2)	20.9(18.7)	20.3(18.2)	19.7(17.5)
1010	16.7	21.5(19.4)	21.2(19.0)	21.1(18.8)	21.2(18.9)	20.7(18.7)	20.4(18.2)	19.8(17.7)	19.2(17.0)
1001	16.7	21.6(19.4)	21.3(19.1)	21.2(19.0)	21.3(19.0)	20.8(18.5)	20.4(18.0)	19.9(17.7)	19.2(17.0)
1000	19.6	21.2(19.2)	21.2(18.6)	20.7(18.7)	20.8(18.8)	20.6(18.2)	20.2(18.2)	19.7(17.6)	19.0(16.9)
0111	33.2	21.1(18.8)	20.8(18.5)	20.6(18.1)	20.5(18.1)	20.3(17.9)	19.5(17.2)	19.5(17.2)	18.7(16.4)
0110	39	20.9(18.8)	20.4(18.3)	20.5(18.3)	20.3(18.0)	20.2(17.8)	19.5(17.4)	19.4(17.1)	18.6(16.6)
0101	50	20.4(18.1)	20.2(17.9)	20.2(18.0)	19.8(17.5)	19.8(17.5)	19.2(17.1)	18.9(16.7)	18.3(16.1)
0100	62	20.5(18.4)	20.1(17.7)	19.9(17.7)	19.7(17.2)	19.3(17.3)	19.3(17.1)	18.6(16.2)	17.8(15.8)
0011	123	19.8(17.3)	19.5(17.0)	19.7(17.2)	19.4(17.0)	19.1(16.4)	18.7(16.3)	18.2(15.8)	17.6(15.0)
0010	242	19.3(16.5)	19.0(16.3)	19.0(16.4)	18.7(16.3)	18.7(16.3)	18.3(15.6)	17.7(15.3)	17.1(14.6)
0001	470	17.7(15.0)	17.7(14.8)	17.7(15.0)	17.6(15.0)	17.6(15.1)	17.3(14.8)	17.0(14.3)	16.5(13.9)
0000	890	14.4(11.5)	14.4(11.7)	14.4(11.6)	14.4(11.2)	14.5(11.6)	14.4(11.6)	14.4(11.6)	14.4(11.6)

ON-CHIP REGISTER MAPS

There are total eight registers inside the device which is 8-bit, 16-bit, or 24-bit wide. These registers are used to configure and control the ADC to the desired mode of operation. These registers can be accessed through the SPI-compatible serial interface by using register read and write commands. At power-on or reset, the registers default to their initial settings, as shown in the *Reset Value* column of Table 3.

Table 3. SIG7798/SIG7799 register map

ADDR.	NAME	DIR.	RESET VALUE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3'b000	STATUS	R	80	DRDYn	ERR	NOREF	0	24-bit	CHD[2:0]		
3'b001	MODE	R/W	000A	MD[2:0]			PSW	0	0	0	0
				0	0	0	CHOPn	FS[3:0]			
3'b010	CONFIG	R/W	0710	0	0	BURN	FORMAT	0	PGA[2:0]		
				0	0	REFDET	BUF	0	CH[2:0]		
3'b011	DATA	R	000000 /(0000) (1)	DATA[23:16] (SIG7799 only)							
				DATA[15:8]							
				DATA[7:0]							
3'b100	ID	R	X9/(X8) (1)	x	x	x	x	1	0	0	0/1
3'b101	IO	R/W	00	0	IOEN	IO2DAT	IO1DAT	0	0	0	0
3'b110	OFFSET	R/W	800000 /(8000)(1)	OFFSET[23:16] (SIG7799 only)							
				OFFSET[15:8]							
				OFFSET[7:0]							
3'b111	GAIN	R/W	555555 /(5555)(1)	GAIN[23:16] (SIG7799 only)							
				GAIN[15:8]							
				GAIN[7:0]							

(1) The values in bracket are the default reset value for SIG7798.

STATUS Register

Table 4. STATUS Register (Address = 3'b000)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DRDYn	ERR	NOREF	0	24-bit	CHD[2:0]		

Power-On/Reset Value = 0x80(SIG7798)/ 0x88(SIG7799)

Bits	Bit Name	Access	Reset	Description
7	DRDYn	R	1'b1	**ADC Ready Bit:** This bit is cleared when new data is written to the ADC data register. It is set automatically after the ADC data register is read. In addition to this bit, DOUT/DRDYn pin can also be used as an alternative to monitor the update of new ADC data.
6	ERR	R	1'b0	**ADC Error Bit.** This bit is written at the same time as new data update. Error sources include input overrange, input underrange, or lower than expected reference voltage.
5	NOREF	R	1'b0	**No External Reference Bit:** The function of this bit is only enabled by setting the REFDET bit in the CONFIG Register to 1. While the REFDET bit is 1 and the selected reference voltage is below a specified threshold, which is about 0.4V, this bit is set and conversion results are clamped to all 1s.
4	RESERVED	R	1'b0	**Reserved**
3	24-bit	R	1'b0(7798) 1'b1(7799)	**24-Bit Device Indicator.** This bit indicates whether this device is 16-bit (SIG7798) or 24-bit (SIG7799).
2:0	CHD[2:0]	R	3'b000	**Data Channel Number:** These bits indicate the corresponding channel to the ADC data in data register (see Table 7).

MODE Register

Table 5. MODE Register (Address = 3'b001)

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MD[2:0]			PSW	0	0	0	0
0	0	0	CHOPn	FS[3:0]			

Power-On/Reset Value = 0x000A

Bits	Bit Name	Access	Reset	Description
15:13	MD[2:0]	R/W	3'b000	**Mode Select Bits:** These bits select the operating mode of the device. 000: Continuous conversion mode. (default) 001: Single conversion mode. ADC first wakeup if in idle or sleep mode; resets the filter to perform one conversion; and enters sleep mode. The conversion result remains in the data register with DOUT/DRDYn as low. 010: Idle mode. The digital filter is in reset state with ADC free running. 011: Sleep mode. Most of circuitry is turned off to save the power. 100: Internal zero-scale calibration. 101: Internal full-scale calibration. 110: System zero-scale calibration. 111: System full-scale calibration. For each above calibration mode, DOUT/DRDYn goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is automatically placed in idle mode after the calibration. The measured offset/full-scale coefficient is placed in the offset/full-scale register of the selected channel.
12	PSW	R/W	1'b0	**Low-Side Power Switch Control Bit:** When this bit is set to 1, the switch is closed to short PSW to GND with low on-resistor of typical 3 Ohms. The switch is open if the bit is cleared. The switch remains open in sleep mode.
11:5	RESERVED	R/W	7'b0000000	**Reserved** Always write 7'b0000000
4	CHOPn	R/W	1'b0	**Chop Disable Bit:** When chop is enabled with bit clear to logic 0, the offset and offset drift of the ADC are dramatically improved with settling time doubled. All output data are fully settled data. For default data rate settling of 16.7SPS, the conversion time is 60ms for all output data with chop disabled. If chop is enabled, the conversion time is 120ms for the first data and 60ms thereafter.
3:0	FS[3:0]	R/W	4'b1010	**Data Rate Configuration:** Selects the ADC data rate. 0000: 890SPS 0001: 470SPS 0010: 242SPS 0011: 123SPS 0100: 62SPS 0101: 50SPS 0110: 39SPS 0111: 33.2SPS 1000: 19.6SPS 1001: 16.7SPS 1010: 16.7SPS (default) 1011: 12.5SPS 1100: 10SPS 1101: 8.33SPS 1110: 6.25SPS 1111: 4.17SPS

CONFIG Register

Table 6. CONFIG Register (Address = 3'b010)

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	BURN	FORMAT	0	PGA[2:0]		
0	0	REFDET	BUF	0	CH[2:0]		

Power-On/Reset Value = 0x0710

Bits	Bit Name	Access	Reset	Description
15:14	RESERVED	R/W	2'b00	**Reserved** Always write 2'b00
13	BURN	R/W	1'b0	**Burnout Enable Bit:** When this bit is enabled, a pair of 0.5μA current sources are applied to analog inputs to source positive input and sink negative input.
12	FORMAT	R/W	1'b0	**Data Format Bit:** This bit sets the ADC data format. 0: Bipolar mode (default) 1: Unipolar mode
11	RESERVED	R/W	1'b0	**Reserved** Always write 1'b0
10:8	PGA[2:0]	R/W	3'b111	**PGA Gain Configuration:** Selects the PGA gain. If PGA gain is set to other than 1 and 2, the BUF bit setting is ignored with buffer always enabled. 000: Gain=1 001: Gain=2 010: Gain=4 011: Gain=8 100: Gain=16 101: Gain=32 110: Gain=64 111: Gain=128 (default)
7:6	RESERVED	R/W	2'b00	**Reserved** Always write 2'b00
5	REFDET	R/W	1'b0	**Reference Detection Enable Bit:** When this bit is enabled, the NOREF bit in the STATUS register indicates when the reference input voltage is less than specified threshold, which is about 0.4V.
4	BUF	R/W	1'b1	**Buffer Enable Bit:** When this bit is set, analog input is buffered. Otherwise the input buffer is bypassed. The buffer can only be disabled when the gain equals 1 or 2. For higher gains, the buffer is automatically enabled.
3	RESERVED	R/W	1'b0	**Reserved** Always write 1'b0
2:0	CH[2:0]	R/W	3'b000	**Channel Select Bits:** These bits select which channel is enabled for ADC conversion (see Table 7). When ADC finishes the conversion and places the data into data register with the corresponding channel information in STATUS register.

Table 7. Channel Selection

CHD[2:0]	Positive Input AIN+	Negative Input AIN-	Status Register Bits CHD[2:0]	Calibration Register Pair
000	AIN1+	AIN1-	000	0
001	AIN2+	AIN2-	001	1
010	AIN3+	AIN3-	010	2
011	AIN1-	AIN1-	011	0
100	Reserved		100	
101	Reserved		101	
110	Reserved		110	
111	AVDD Monitor(1)		111	Default Reset Values

(1) For AVDD monitor measurement, the AVDD is internally attenuated by 6, PGA gain is forced to 1 with buffer on and internal 1.17V reference is used disregarding user register configuration.

DATA Register

This register is 16 bits wide for SIG7798 and 24 bits wide for SIG7799.

Table 8. DATA Register (Address = 3'b011)

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DATA[23]	DATA[22]	DATA[21]	DATA[20]	DATA[19]	DATA[18]	DATA[17]	DATA[16]
DATA[15]	DATA[14]	DATA[13]	DATA[12]	DATA[11]	DATA[10]	DATA[9]	DATA[8]
DATA[7]	DATA[6]	DATA[5]	DATA[4]	DATA[3]	DATA[2]	DATA[1]	DATA[0]

Power-On/Reset Value = 0x0000(SIG7798)/0x000000(SIG7799)

Bits	Bit Name	Access	Reset	Description
23:0	DATA[23:0]	R	0x000000	**Data Bits:** The 16-bit word for SIG7798 or 24-bit word for SIG7799 is signed number in 2's complement format. See Data Format section for more information.

ID Register

Table 9. ID Register (Address = 3'b100)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
x	x	x	x	1	0	0	0/1

Power-On/Reset Value = 0xX8(SIG7798)/0xX9(SIG7799)

Bits	Bit Name	Access	Reset	Description
7:0	ID	R	8'bxxxx100x	**ID Bits:** Read only.

IO Register

Table 10. IO Register (Address = 3'b101)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	IOEN	IO2DAT	IO1DAT	0	0	0	0

Power-On/Reset Value = 0x00

Bits	Bit Name	Access	Reset	Description
7	RESERVED	R/W	1'b0	**Reserved** Always write 1'b0
6	IOEN	R/W	1'b0	**P2 and P1 Output Enable Bit:** When this bit is set to 1, the P2 and P1 pins are configured as outputs. When this bit is set to 0, the P2 and P1 pins are tri-state.

5	IO2DAT	R/W	1'b0	**Data Output P2 Bit:** This bit sets the value of the P2 output pin if IOEN bit is set to 1. During IO register read, the IO2DAT reflects the status of the P2 pin if IOEN bit is set to 1.
4	IO1DAT	R/W	1'b0	**Data Output P1 Bit:** This bit sets the value of the P1 output pin if IOEN bit is set to 1. During IO register read, the IO1DAT reflects the status of the P1 pin if IOEN bit is set to 1.
3:0	RESERVED	R/W	4'b0000	**Reserved** Always write 4'b0000

OFFSET Register

The device has four OFFSET registers, each channel has a dedicated OFFSET register (see Table 7). This register is 16 bits wide for SIG7798 and 24 bits wide for SIG7799. OFFSET register read is allowed anytime, but writing to OFFSET register is only allowed while the device is in idle or sleep mode.

Table 11. OFFSET Register (Address = 3'b110)

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OFFSET[23]	OFFSET[22]	OFFSET[21]	OFFSET[20]	OFFSET[19]	OFFSET[18]	OFFSET[17]	OFFSET[16]
OFFSET[15]	OFFSET[14]	OFFSET[13]	OFFSET[12]	OFFSET[11]	OFFSET[10]	OFFSET[9]	OFFSET[8]
OFFSET[7]	OFFSET[6]	OFFSET[5]	OFFSET[4]	OFFSET[3]	OFFSET[2]	OFFSET[1]	OFFSET[0]

Power-On/Reset Value = 0x8000(SIG7798)/0x800000(SIG7799)

Bits	Bit Name	Access	Reset	Description
23:0	OFFSET[23:0]	R/W	0x800000	**Offset Calibration Bits:** The 24-bit word is signed number in offset binary format. See Calibration section for more information.

GAIN Register

The device has four GAIN registers, each channel has a dedicated GAIN register (see Table 7). This register is 16 bits wide for SIG7798 and 24 bits wide for SIG7799. GAIN register read is allowed anytime, but writing to GAIN register is only allowed while the device is in idle or sleep mode.

Table 12. GAIN Register (Address = 3'b111)

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GAIN[23]	GAIN[22]	GAIN[21]	GAIN[20]	GAIN[19]	GAIN[18]	GAIN[17]	GAIN[16]
GAIN[15]	GAIN[14]	GAIN[13]	GAIN[12]	GAIN[11]	GAIN[10]	GAIN[9]	GAIN[8]
GAIN[7]	GAIN[6]	GAIN[5]	GAIN[4]	GAIN[3]	GAIN[2]	GAIN[1]	GAIN[0]

Power-On/Reset Value = 0x5555(SIG7798)/0x555555(SIG7799)

Bits	Bit Name	Access	Reset	Description
23:0	GAIN[23:0]	R/W	0x555555	**Gain Calibration Bits:** The 24-bit word is unsigned positive number in binary format. See Calibration section for more information.

REVISION HISTORY

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please contact to make sure you have the latest revision.

DATE	REVISION	CHANGE
May 20, 2022		Initial release.
Sept. 18, 2024		Revision.

DISCLAIMER

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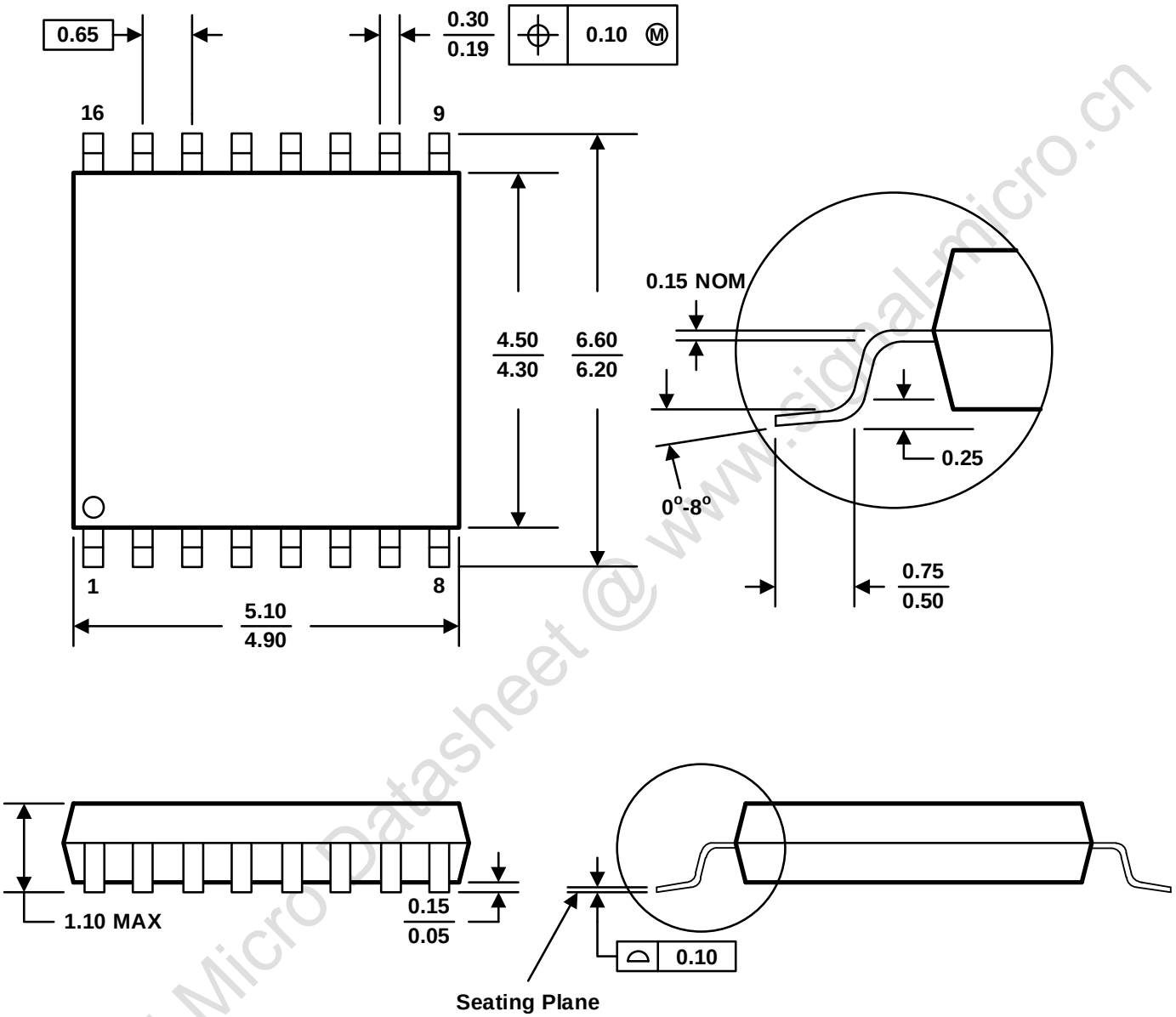
PACKAGE OUTLINE DIMENSIONS



A. Compliant to JEDEC STARDARDS MO-153-AD.
B. All linear dimensions are in millimeters.
C. This drawing is subject to change without notice.