FEATURES

Industrial Applications

Servers

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FEATURES

♦4.5V to 40V operating input range

♦Internal 40V, 30mΩ Ron hot-swap N-Channel FET

♦Reverse blocking current in 0.2us

♦Integrated current sensing with sense output

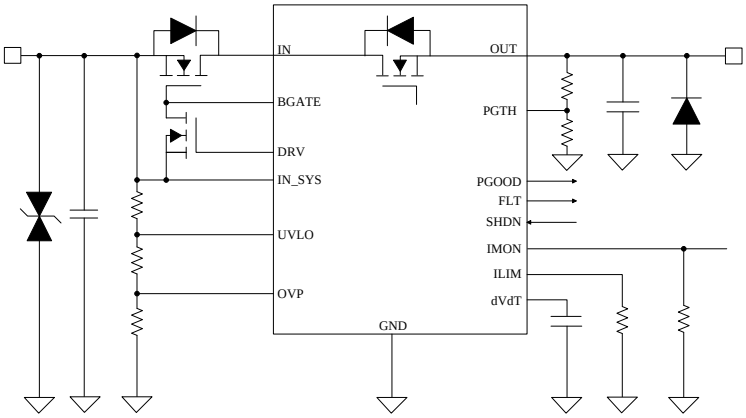
♦Adjustable current limit from 0.6A to 5A

♦Adjustable UVLO, OVP cutoff, output slew rate control for inrush current limiting

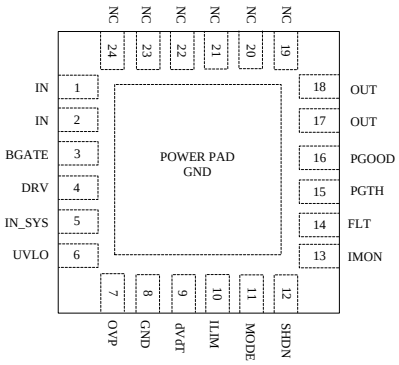
♦Power Good Output (PGOOD)

♦ overcurrent fault response with auto-retry

♦Models with 1.5x pulsed overcurrent support



Simplified schematic



TPS26630 Package QFN4*4-24L

General information

Ordering information

Part Number	Description
TPS26630RGER	QFN4*4-24L， RoHS

Package dissipation rating

Package	$R_{\theta JA}$（℃/W）	$R_{\theta JC}$（℃/W）(top)
QFN4*4-24L	32	23

Absolute maximum ratings

Parameter	Value
IN, IN_SYS, OUT, UVLO, $\overline{FLT}$, PGOOD, PGTH	-0.3~60V
IN, IN_SYS (10ms transient)	-0.3~65V
BGATE	-0.3~65V
DRV	-0.3~65V
DRV - IN_SYS	-0.3~15V
OVP, dVdT, I_{MON}, MODE, $\overline{SHDN}$, I_{LIM}	-0.3~5.5V
Junction temperature T_J	-40 to 150℃
Ambient temperature T_A	-40 to 85℃
Storage temperature T_{STG}	-55 to 150℃
ESD(HBM)	±2.0kV
Leading temperature (soldering, 10secs)	260℃

Note: stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

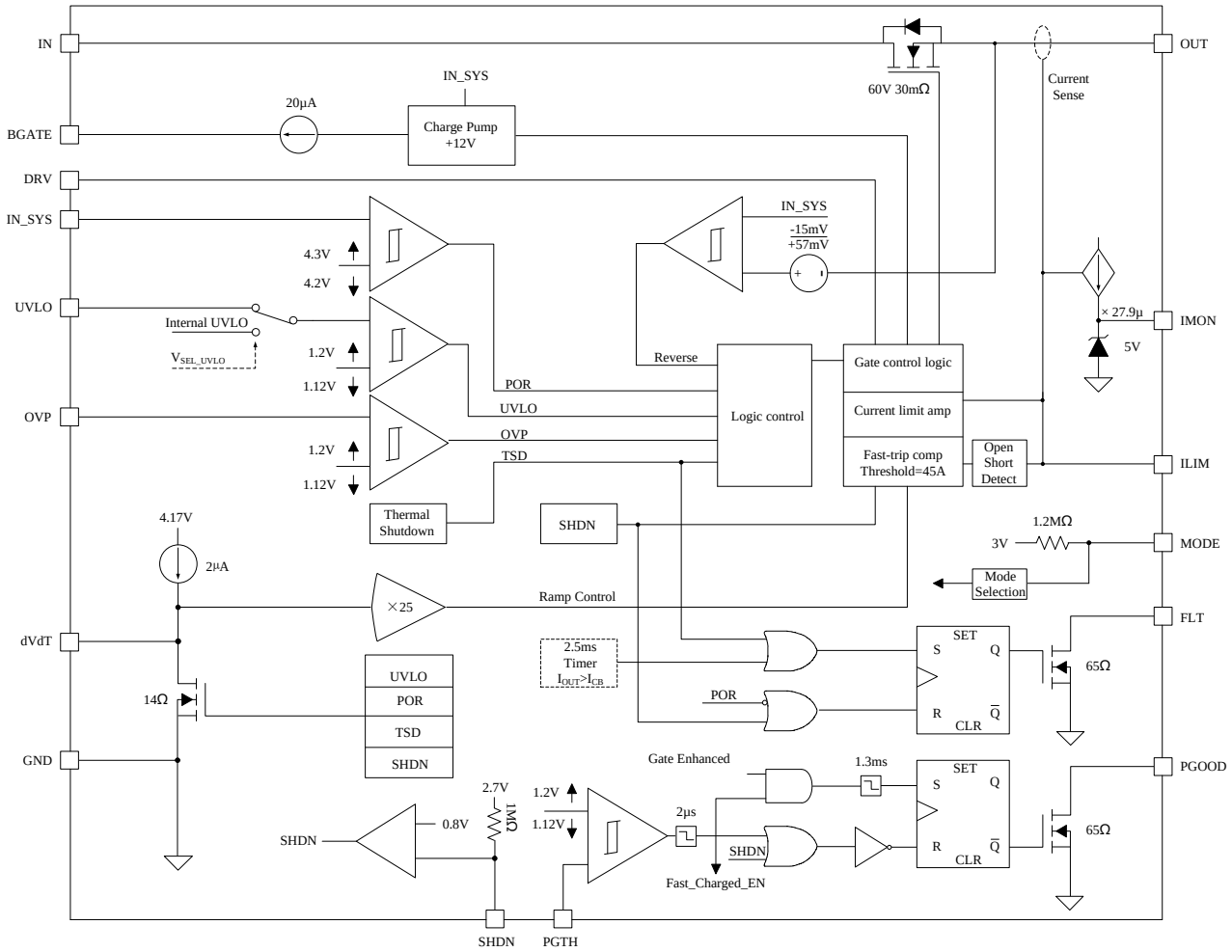
Recommended operating condition

Symbol	Parameter	Range
IN_SYS, IN	Input Voltage	4.5~40V
OUT, UVLO, PGTH, PGOOD, $\overline{FLT}$		0-40V
OVP, dVdT, IMON, MODE, $\overline{SHDN}$		0~5V
ILIM	Resistance	5~100kΩ
IMON		≥1kΩ
IN, IN_SYS, OUT	Capacitance	≥100nF
dVdT		≥10nF

Terminal assignments

PIN NO.	PIN name	Description
1/2	IN	Power input. Connect to the Drain of the internal FET.
3	BGATE	Blocking FET gate driver output. Connect to GATE of the external FET. If external FET is not used, then leave BGATE pin floating.
4	DRV	Blocking FET fast pull-down switch drive. Connect DRV to the GATE of external pull-down switch. Leave this pin floating if external FET is not used
5	IN_SYS	Power input and supply voltage of the device. Short IN_SYS to IN in case blocking FET is not used.
6	UVLO	Input for setting the programmable UVLO threshold. Connect UVLO pin to GND to select the internal default threshold.
7	OVP	Input for setting the programmable OVP threshold. Connect OVP to GND if OVP not used.
8	GND	System ground pin.
9	dVdT	A capacitor from this pin to GND sets output voltage slew rate.
10	ILIM	A resistor from this pin to GND sets overload and short circuit current limit.
11	MODE	Mode selection for ILIM pin short protection mode.This pin is pulled up internal.
12	$\overline{SHDN}$	Pulling $\overline{SHDN}$ pin low makes the device to enter shutdown mode. Cycling $\overline{SHDN}$ pin voltage resets the device that fast latched off due to a fault condition.
13	IMON	Analog current monitor. A resistor from this pin to GND converts current to voltage. If unused, leave it floating.
14	$\overline{FLT}$	Fault event indicator. It is an open drain output. If unused, leave floating or connect to GND.
15	PGTH	PGOOD comparator input.
16	PGOOD	Active high. A high indicates PGTH has crossed the V_{PGTHR} threshold, and the internal driver is high. PGOOD goes low when V_{PGTH} hits V_{PGTHF} threshold. If PGOOD is unused connect to GND or leave it floating.
17/18	OUT	Power output of the device.
19~24	NC	No connect.
Power Pad		Ground.

Block Diagram



Electrical characteristics

4.5V ≤ V_{IN_SYS} = V_{IN} ≤ 40V, $V_{\overline{SHDN}}$ = 2V, R_{ILIM} = 10kΩ, UVLO = OVP = 0V, C_{OUT} = 1μF, C_{dVdT} = OPEN. (Unless otherwise noted))

Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
IN_SYS supply voltage						
V_{IN_SYS}	Operating input voltage		4.5		40	V
IQ_{ON}	Supply current	$\overline{SHDN}$ = 3V enable	0.5	1.0	1.5	mA
IQ_{OFF}	Supply current	$\overline{SHDN}$ = 0V disable	5	10	30	uA
Under Voltage Lockout Input						
UVLO	Internal undervoltage trip level	IN_SYS rising	14.8	15.4	16.0	V
		IN_SYS falling	14.0	14.6	14.8	V
V_{SEL_UVLO}	Internal UVLO select threshold		180	210	240	mV
V_{UVLOR}	UVLO threshold voltage, rising		1.18	1.21	1.26	V
V_{UVLOF}	UVLO threshold voltage, falling		1.06	1.13	1.17	V
I_{UVLO}	UVLO input leakage current	0V ≤ V_{UVLO} ≤ 40V	-1	0	1	uA
OVERVOLTAGE PROTECTION (OVP) INPUT						
V_{OVPR}	OVP threshold voltage, rising		1.18	1.21	1.26	V
V_{OVPF}	OVP threshold voltage, falling		1.06	1.13	1.17	V
I_{OVP}	OVP input leakage current	0V ≤ V_{OVP} ≤ 4V	-1	0	1	uA
Current Limit Programming ILIM						
I_{OL}	Overload current limit	R_{ILIM} = 75kΩ， V_{IN} - V_{OUT} = 1V	0.54	0.6	0.66	A
		R_{ILIM} = 20kΩ， V_{IN} - V_{OUT} = 1V	1.80	2.05	2.22	A
		R_{ILIM} = 7.5kΩ， V_{IN} - V_{OUT} = 1V	4.37	4.86	5.39	A
		R_{ILIM} = 6.2kΩ， V_{IN} - V_{OUT} = 1V	4.99	5.49	6.03	A
I_{OL_Pulse}	Transient pulse over current limit	6.2kΩ≤R_{LIM}≤75kΩ	1.5*I_{OL}			A
$I_{FASTTRIP}$	Fast-trip comparator threshold	6.2kΩ≤R_{LIM}≤75kΩ	I_{OL}			A
I_{SCP}	Short circuit protect current		45			A
BGATE （Blocking FET Gate Driver）						
V_{BGATE}	BGATE clamp voltage	V_{BGATE} - V_{IN_SYS}	8.0	10.0	14.0	V
I_{BGATE}	Blocking FET gate drive current	V_{BGATE} - V_{IN_SYS} = 1V	16	20	23	uA
R_{PD_BGATE}	B_{GATE} pull down resistance		800	1300	1500	KΩ
V_{DRV_OH}	DRV logic high level	V_{DRV} - V_{IN_SYS}, C_{DRV} ≤ 50pF	3	5	6	V
PASS FET OUTPUT (OUT)						
R_{ON}	IN to OUT total ON resistance	0.6A ≤ I_{OUT} ≤ 5A	20	30	50	mΩ
I_{lkgOUT}	OUT leakage during input supply brownout	V_{IN_SYS} = 0V, V_{OUT} = 24V, V_{IN} = Floating, $V_{\overline{SHDN}}$ = 3V, Sinking	3	3.5	7	mA
V_{REVTH}	V_{IN_SYS} – V_{OUT} threshold for reverse protection comparator, rising		-20	-15	-9	mV
V_{FWDTH}	V_{IN_SYS} – v_{OUT} threshold for reverse protection comparator, falling		45	57	67	mV
OUTPUT RAMP CONTROL (dVdT)						

I_{dVdT}	dVdT charging current	V_{dVdT} = 0V	1.8	2.1	2.3	uA
$GAIN_{dVdT}$	dVdT to OUT gain	V_{OUT} / V_{dVdT}	23.5	25	26	V/V
$V_{dVdTmax}$	dVdT maximum capacitor voltage		4.5	5.0	5.5	V
R_{dVdT}	dVdT discharging resistance		10	14.0	24..0	Ω
LOW IQ SHUTDOWN ($\overline{SHDN}$) INPUT						
$V_{\overline{SHDN}}$	Open circuit voltage	$I_{\overline{SHDN}}$ = 0.1μA	2.48	2.7	3.3	V
V_{SHUTF}	$\overline{SHDN}$ threshold voltage for low IQ shutdown, falling		0.8			V
V_{SHUTR}	$\overline{SHDN}$ threshold rising				2	V
$I_{\overline{SHDN}}$	Leakage current	$V_{\overline{SHDN}}$ = 0V	-10	-2.7	0	uA
CURRENT MONITOR OUTPUT (IMON)						
$GAIN_{IMON}$	Gain factor I_{IMON}: I_{OUT}	0.6A ≤ I_{OUT} ≤ 2A	25.66	27.9	30.14	uA/A
		2A ≤ I_{OUT} ≤ 5A	26.22	27.9	29.58	uA/A
FAULT FLAG ($\overline{FLT}$): ACTIVE LOW						
$R_{\overline{FLT}}$	$\overline{FLT}$ Pull-down resistance		36	70	130	Ω
$I_{\overline{FLT}}$	$\overline{FLT}$ Input leakage current	0V ≤ $V_{\overline{FLT}}$ ≤ 40V	-1	0	1	uA
POWER GOOD (PGOOD)						
R_{PGOOD}	PGOOD Pull-down resistance		36	70	130	Ω
I_{PGOOD}	PGOOD Input leakage current	0V ≤ V_{PGOOD} ≤ 40V	-1	0	1	uA
POSITIVE INPUT FOR POWER GOOD COMPARATOR (PGTH)						
V_{PGTHR}	PGTH threshold voltage, rising		1.20	1.24	1.26	V
V_{PGTHF}	PGTH threshold voltage, falling		1.13	1.15	1.17	V
I_{PGOOD}	PGTH input leakage current	0V ≤ V_{PGTH} ≤ 40V	-1	0	1	uA
THERMAL PROTECTION						
$T_{TSDrelease}$	Thermal shutdown release			130		℃
T_{TSD}	Thermal shutdown TSD threshold, rising			140		℃
$T_{TSDhyst}$	TSD hysteresis			11		℃

Timing Requirements

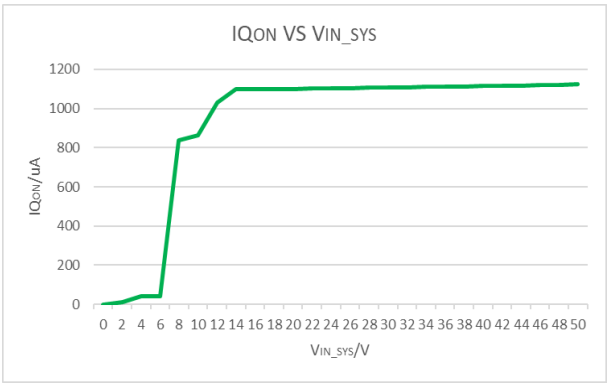
4.5V ≤ V_{IN_SYS} = V_{IN} ≤ 40V, $V_{\overline{SHDN}}$ = 3V, R_{ILIM} = 10kΩ, UVLO = OVP = 0V, C_{OUT} = 1 µF, C_{dVdT} = OPEN. (Unless otherwise noted))

Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
UVLO INPUT (UVLO)						
$UVLO_{t_{on(dly)}}$	UVLO switch turn-on delay	UVLO ↑ (100mV above V_{UVLOR}) to V_{OUT} = 100mV with V_{PGTH} < V_{PGTHF}, C_{dVdT} ≥ 10nF, [C_{dVdT} in nF]		730 + 49.5 x C_{dVdT}		us
$UVLO_{t_{on(fast\_dly)}}$	UVLO switch turn-on delay (fast)	UVLO ↑ (100mV above V_{UVLOR} to FET ON with V_{PGTH} > V_{PGTHF})	70	90	200	us
$UVLO_{t_{off(dly)}}$	UVLO switch turnoff delay	UVLO ↓ (20mV below V_{UVLOF}) to $\overline{FLT}$ ↓		520	600	us
$tUVLO_{(\overline{FLT}dly)}$	UVLO to fault de-assertion delay	UVLO ↑ to $\overline{FLT}$ ↑ delay	500	640	700	us
OVER VOLTAGE PROTECTION INPUT (OVP)						
$OVP_{t_{OFF(dly)}}$	OVP switch turnoff delay	OVP ↑ (20mV above V_{OVPR}) to $\overline{FLT}$ ↓	8	14	30	us
$OVP_{t_{on(fast\_dly)}}$	OVP switch turn-on delay (fast)	OVP ↓ (100mV below V_{OVPF}) to FET ON with V_{PGTH} > V_{PGTHF}	10	34	60	us
$OVP_{t_{on(dly)}}$	OVP switch disable delay	OVP ↓ (100mV below V_{OVPF}) to FET ON with V_{PGTH} < V_{PGTHF}, C_{dVdT} ≥ 10nF, [C_{dVdT} in nF]		200 + 49.5 x C_{dVdT}		us
SHUTDOWN CONTROL INPUT ($\overline{SHDN}$)						
$t_{SD(dly)}$	SHUTDOWN entry delay	$\overline{SHDN}$ ↓ (below V_{SHUTF}) to FET OFF	0.8	1	1.5	us
CURRENT LIMIT						
$t_{FASTTRIP(dly)}$	Hot-short response time	I_{OUT} > I_{SCP}		1		us
	Soft short response	$I_{FASTTRIP}$ < I_{OUT} < I_{SCP}	2.2	3.2	4.5	us
$t_{CBRetry(dly)}$	Retry delay in Pulse over current limiting		550	670	800	ms
REVERSE CURRENT BLOCKING (RCB) COMPARATOR						
$t_{RCB(fast\_dly)}$	Reverse protection comparator detection delay (reverse)	(V_{IN_SYS} – V_{OUT}) ↓ (1V overdrive below V_{REVTH}) to V_{DRV} – V_{IN_SYS} = V_{DRV_OH}		0.2		us
$t_{RCB(dly)}$		(V_{IN_SYS} – v_{OUT}) ↓ (10mV overdrive below V_{REVTH}) to V_{DRV} – V_{IN_SYS} = V_{DRV_OH}		0.5		us
$t_{RCB(flt\_dly)}$	Fault assertion Delay	(V_{IN_SYS} – V_{OUT}) ↓ (10mV overdrive below V_{REVTH}) to $\overline{FLT}$↓	500	600	800	us
$t_{FWD\_\overline{FLT}\ (dly)}$	Reverse protection comparator detection delay (forward)	(V_{IN_SYS} – V_{OUT}) ↑ (10mV overdrive above V_{FWDTH}) to V_{BGATE} – V_{IN_SYS} = 5V, $C_{BFET\text{-}IN\_SYS}$ = 4.7nF		1.0		ms
	Fault de-assertion Delay	(V_{IN_SYS} – V_{OUT}) ↑ (10mV overdrive above V_{FWDTH}) to $\overline{FLT}$↑	430	630	800	us

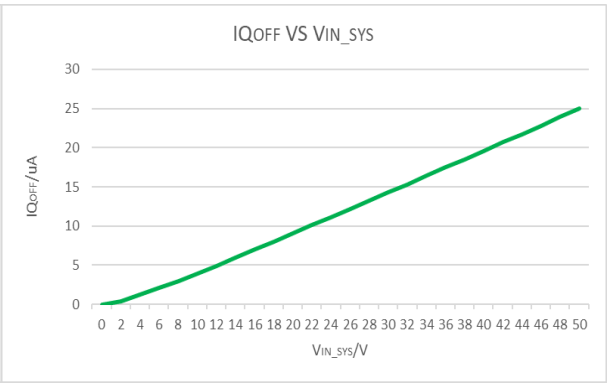
OUTPUT RAMP CONTROL (dVdT)						
$t_{FASTCHARGE}$	Output ramp time in fast charging	C_{dVdT} = Open, 10% to 90% V_{OUT}, C_{OUT} = 1µF; V_{IN} = 24V	50	100	300	us
t_{dVdT}	Output ramp time	C_{dVdT} = 10nF, 10% to 90% V_{OUT}, V_{IN} = 24V		4.0		ms
POWER GOOD (PGOOD)						
t_{PGOODR}	PGOOD delay (deglitch) time	Rising edge	1.0	2.0	3.0	ms
t_{PGOODF}	PGOOD delay (deglitch) time	Falling edge, PGTH ↓ (10mV below V_{PGTHF})	1.3	3.2	4	us
FAULT FLAG ($\overline{FLT}$)						
$t_{CB\_\overline{FLT}\ (dly)}$	$\overline{FLT}$ assertion delay in Pulse over current limiting	Delay from I_{OUT} > I_{OL} to $\overline{FLT}$↓.	22	25	30	ms
THERMAL PROTECTION						
t_{TSD_retry}	Retry delay in TSD		500	660	800	ms

Typical Characteristics

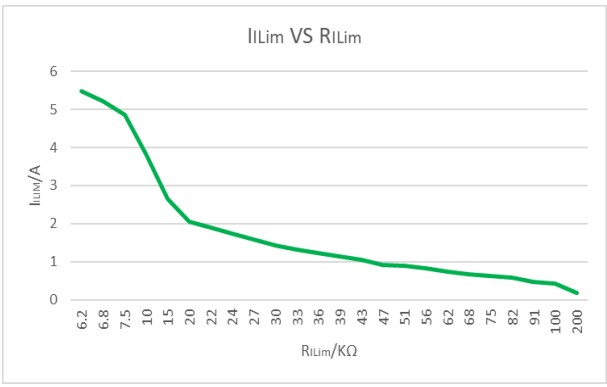
V_{IN_SYS} = V_{IN} = 24V, $V_{\overline{SHDN}}$ = 3V, R_{ILIM} = 10kΩ, UVLO = OVP = 0V, C_{OUT} = 1μF, C_{dvdT} = OPEN. (Unless stated otherwise)



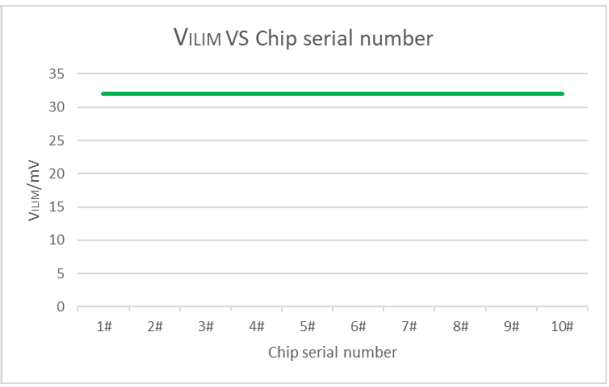
Supply Current vs Supply Voltage During Normal Operation



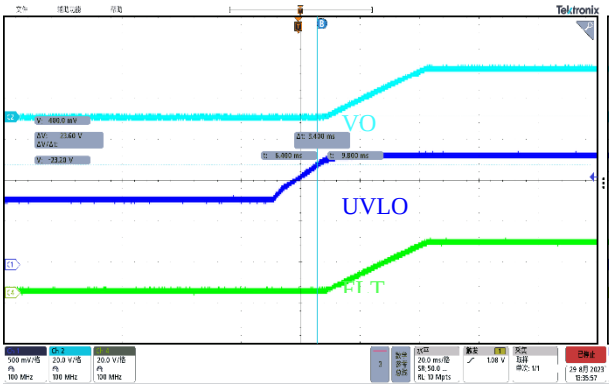
Supply Current vs Supply Voltage in Shutdown



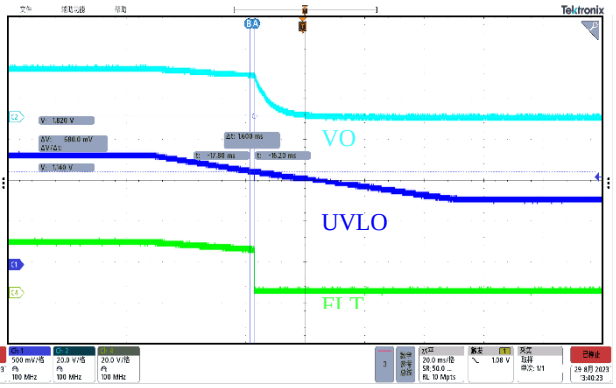
I_{ILIM} VS R_{ILIM} with V_{IN_SYS} = 24V



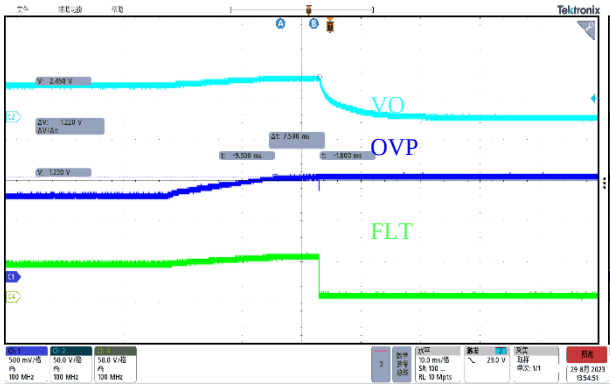
V_{ILIM} consistency between different chips



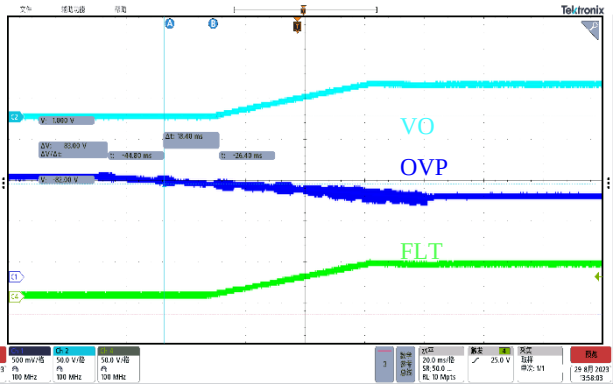
UVLO Performance during V_{IN_SYS} from 14V to 24V



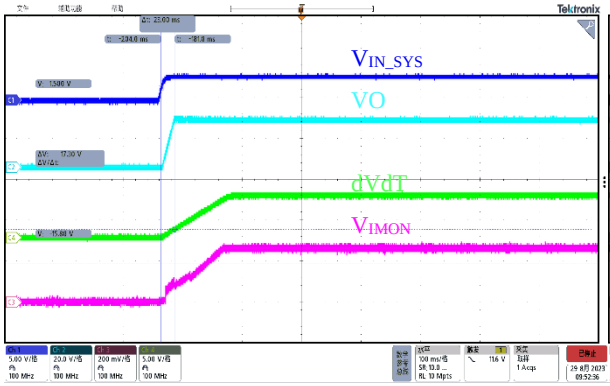
UVLO Performance during V_{IN_SYS} from 24V to 14V



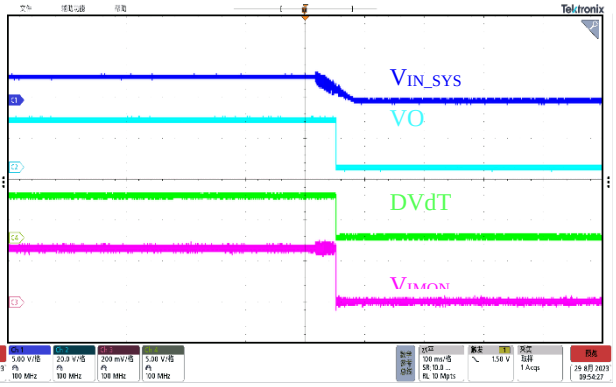
Enter OVP protection



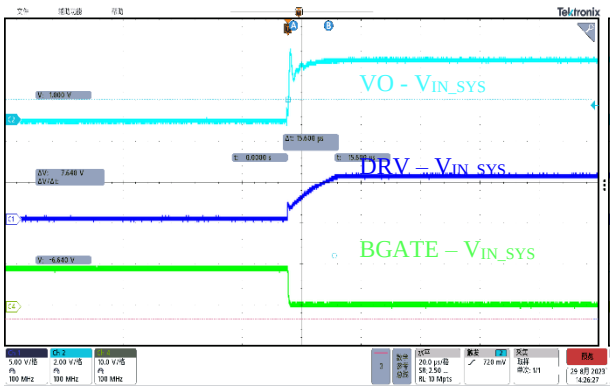
Exit OVP Protection



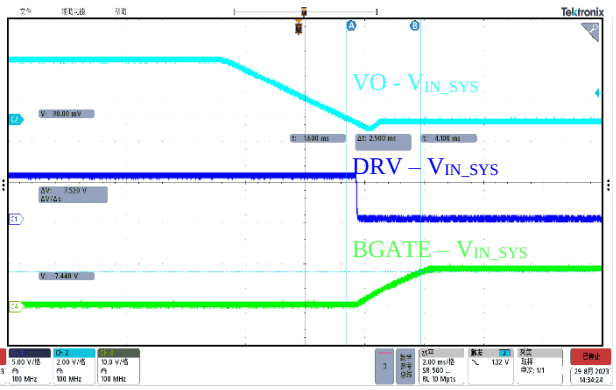
Turn on control with SHDN



Turn off control with SHDN

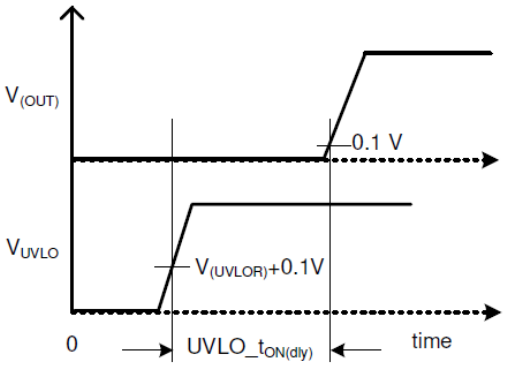


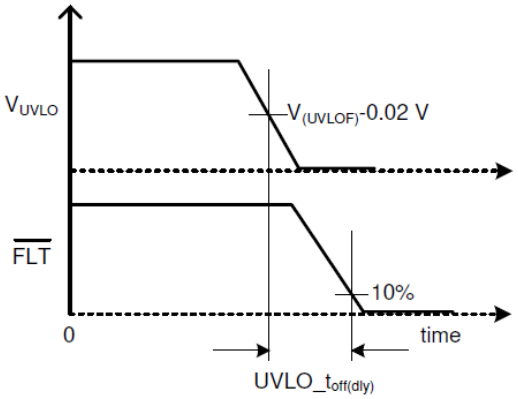
Enter Reverse Current Protection

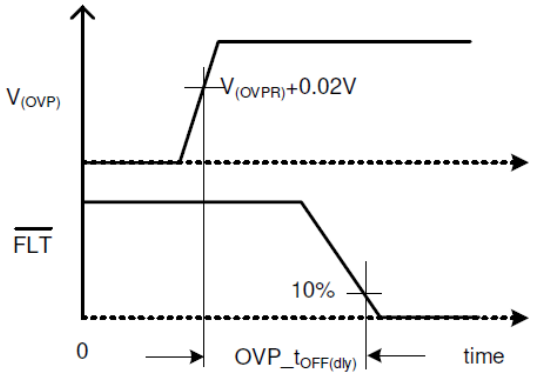


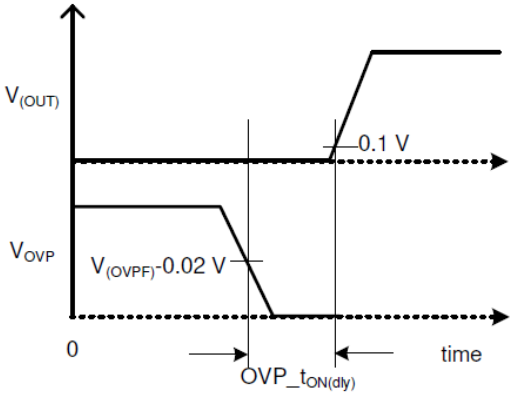
Exit Reverse Current Protection

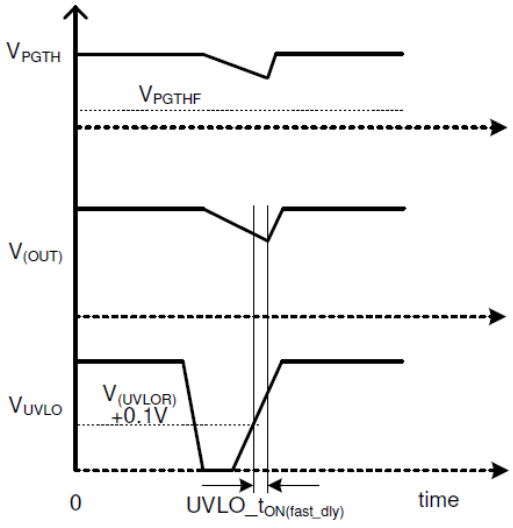
Parameter Measurement Information

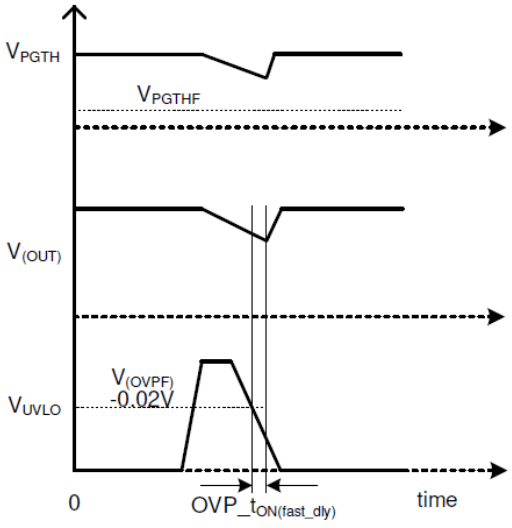


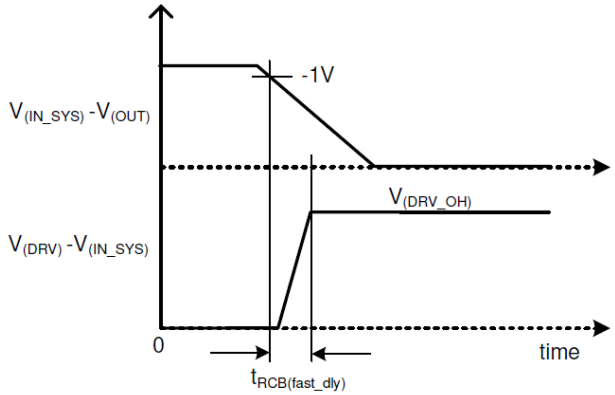


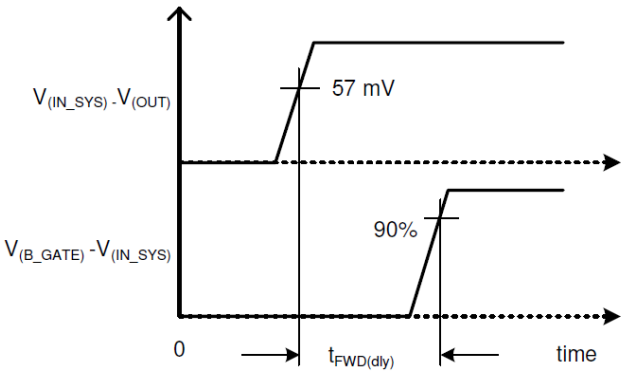









-1V
$V_{(IN\_SYS)}$ -$V_{(OUT)}$
$V_{(DRV\_OH)}$
$V_{(DRV)}$ -$V_{(IN\_SYS)}$
0
time
$t_{RCB(fast\_dly)}$


57 mV
$V_{(IN\_SYS)}$ -$V_{(OUT)}$
90%
$V_{(B\_GATE)}$ -$V_{(IN\_SYS)}$
0
$t_{FWD(dly)}$
time

Operation description

The TPS26630RG is an 40V industrial eFuse. The device provides robust protection for all systems and applications powered from 4.5V to 40V. For hot-pluggable boards, the devices provide hot-swap power management with in-rush current control and programmable output voltage slew rate features using the dVdT pin. Load, source, and device protections are provided with many programmable features including overcurrent, overvoltage and undervoltage. The precision overcurrent limit (±10% at 5A) helps to minimize over design of the input power supply, while the fast response short circuit protection immediately isolates the faulty load from the input supply when a short circuit is detected. The device features fast reverse current blocking response (0.2us). The internal robust protection control blocks of the TPS26630 along with its 40V rating, helps to simplify the system designs for the industrial surge compliance ensuring complete protection of the load and the device. The 40V maximum DC operating and 60V absolute maximum voltage rating enables system protection from 40V DC input supply faults and from industrial SELV power supplies.

By monitoring the output (Load) voltage through the PGTH pin, the device distinguishes between real system faults and system transients and the turn ON delay during a fault recovery is controlled accordingly. The valid load voltage detection threshold can be adjusted using a resistor ladder network from OUT, PGTH and GND.

The devices provide precise monitoring of voltage bus for brown-out, overvoltage conditions and asserts fault signal for the downstream system. Its overall threshold accuracy of 2% ensures tight supervision of bus, eliminating the need for a separate supply voltage supervisor chip. The devices monitor V_{IN_SYS} and V_{OUT} to provide true reverse current blocking when a reverse condition or input power failure condition is detected.

Additional features of the TPS26630 include:

• ±10% Current monitor output (I_{MON}) for health monitoring of the system

• PGOOD indicator output with ±2% accurate adjustable valid load voltage detection threshold (PGTH)

• Over temperature protection to safely shutdown in the event of an overcurrent event

• De-glitched fault reporting for supply brown-out and overvoltage faults

• Enable and disable control from an MCU using $\overline{SHDN}$ pin.

Hot Plug-In and In-Rush Current Control

The devices are designed to control the inrush current upon insertion of a card into a live backplane or other "hot" power source. This limits the voltage sag on the backplane's supply voltage and prevents unintended resets of the system power. The controlled start-up also helps to eliminate conductive and radiative interferences. An external capacitor connected from the dVdT pin to GND defines the slew rate of the output voltage at power-on. The fastest output slew rate of 24V/120µs can be achieved by leaving dVdT pin floating. The inrush current can be calculated using the following formula:

$$I = C * \frac{dV}{dT} \geq I_{INRUSH} = C_{OUT} * \frac{V_{IN}}{t_{dVdT}}$$

where

$$t_{dVdT} = 20.8 * 10^3 * V_{IN} * C_{dVdT}$$

PGOOD and PGTH

The devices feature an open drain Power good (PGOOD) indicator output. PGOOD can be used for enabling and disabling of the downstream loads like DC-DC converters. Connect a resistor ladder network from V_{OUT}, PGTH and GND to set the PGOOD threshold level. PGOOD goes high when the internal FET's gate is enhanced and V_{PGTH} is above V_{PGTHR}. PGOOD goes low when V_{PGTH} goes below V_{PGTHF}. There is a deglitch of t_{PGOODR}, 2.0ms (typical) at the rising edge and t_{PGOODF}, 3.2µs (typical) deglitch on the falling edge of PGOOD indication. PGOOD is a rated for 40V and can be pulled to IN_SYS or OUT through a resistor. PGTH can be used for setting down stream's supply UVLO levels and PGOOD as enable and disable control.

PGTH as V_{OUT} Sensing Input

The devices use PGTH as the output (Load) voltage monitor input and to set the downstream loads UVLO threshold. To set the input PGTH threshold, connect a resistor divider network from V_{OUT} to PGTH terminal to GND as shown in the Simplified schematic. During a system fault recovery (example: OVP high to low or UVLO low to high) when the internal FET gate control is enabled, the device samples the PGTH information and decides whether to turn ON the FET with fast slew rate or dVdT mode based on the sampled V_{PGTH}

information.

During the fault recovery instance if the V_{PGTH} level is above V_{PGTHF} then the internal FET turns ON within a delay of $t_{OVP(dly\_fast)}$ with fast slew rate (ignores the capacitance connected at dVdT pin). Maximum current through the device during this operation is limited at I_{OL}. During the fault recovery instance if the V_{PGTH} level is below V_{PGTHF} then the device turns ON the internal FET in dVdT mode and the slew rate will depend on the dVdT capacitor value and maximum current through the devices is limited at I_{OL}. This way the device distinguishes between real system faults and system transients and the turn ON delay is controlled accordingly. The fast turn ON during transient recovery feature can be disabled by connecting PGTH to GND. In this case, PGOOD will be pulled low.

Undervoltage Lockout (UVLO)

The TPS26630RG features an accurate ±2% adjustable undervoltage lockout functionality. When the voltage at UVLO pin falls below V_{UVLOF} during input undervoltage fault, the internal FET quickly turns off and $\overline{FLT}$ is asserted. The UVLO comparator has a hysteresis of 78mV (typical). To set the input UVLO threshold, connect a resistor divider network from IN supply to UVLO terminal to GND as shown in the Simplified schematic. The TPS26630RG also features a factory set 15V input supply undervoltage lockout $V_{IN\_SYS\_UVLO}$ threshold with 1V hysteresis. This feature can be enabled by connecting the UVLO terminal directly to the GND terminal. If the Undervoltage Lock-Out function is not needed, the UVLO terminal must be connected to the IN_SYS terminal. UVLO terminal must not be left floating. In the applications where reverse polarity protection is required connect a minimum of 300kΩ resistor between UVLO and IN_SYS.

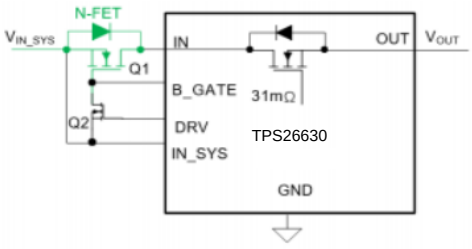
Overvoltage Protection (OVP)

The TPS26630 incorporate circuitry to protect the system during overvoltage conditions. The TPS26630 features an accurate ±2% adjustable overvoltage cut off functionality. A voltage more than V_{OVPR} on OVP pin turns off the internal FET and protects the downstream load. To program the OVP threshold externally, connect a resistor divider from IN_SYS supply to OVP terminal to GND as shown in the Simplified schematic.

Reverse Current Protection

Connect an N-channel power FET (Q1) with the source to IN_SYS, drain to IN and GATE to BGATE as shown in the following figure. This forms a back-to-back FET topology in power path that is required to protect the current reverse. Connect an external signal FET (Q2) across BGATE, DRV and IN_SYS. Q2 acts as a pull-down gate switch for Q1.

In the applications where reverse polarity protection and reverse current blocking is not required then connect IN_SYS and IN togetherand leave BGATE and DRV open.



Configuration for Reverse Current Blocking

The device monitors V_{IN_SYS} and V_{OUT} to provide true reverse current blocking when a reverse condition or input power failure condition is detected.

The reverse comparator turns OFF the external blocking FET Q1 quickly as soon as $V_{IN\_SYS} - V_{OUT}$ falls below –1V. The total time taken to turn OFF the FET Q1 in this condition is $t_{RCB(fast\_dly)} + t_{Driver}$. The delay due to the driver stage t_{Driver} can be calculated using the following formula:

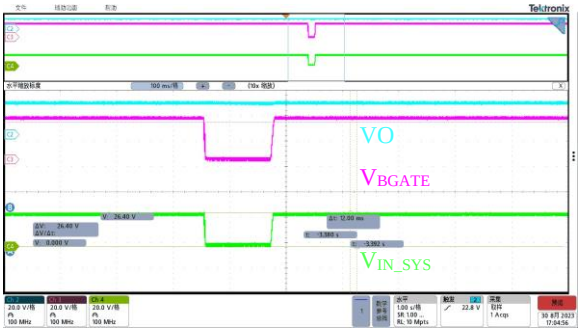
$$t_{Driver} = -RDSON_{Q2} * Ciss_{Q1} * \ln\left(\frac{VGTH_{Q1}}{V_{BGATE}}\right)$$

where

- $RDSON_{Q2}$ is the on resistance of the fast pull-down switch Q2
- $Ciss_{Q1}$ is the input capacitance of the blocking FET Q1
- $VGTH_{Q1}$ is the GATE threshold voltage of the blocking FET Q1
- V_{BGATE} = 10.2V (typical)

In a typical system design, t_{Driver} is generally 10% to 20% of $t_{RCB(fast\_dly)}$ of 0.2us (typical).

The following figure illustrates the behavior of the system during input hot short circuit condition. The blocking FET Q1 is turned ON within 1.6ms (typical) once the differential forward voltage $V_{IN\_SYS} - V_{OUT}$ exceeds 57mV (typical).



Input Hot Short Functionality at 24V Supply

The reverse comparator architecture has a supply line noise immunity resulting in a robust performance in noisy environments. This is achieved by controlling the turn OFF time of the internal FET based on the over-drive differential voltage $V_{IN\_SYS} - V_{OUT}$ over V_{REVTH}. Higher the over-drive, faster the turn OFF time, $t_{RCB(dly)}$.

Overload and Short Circuit Protection

The device monitors the load current by sensing the voltage across the internal sense resistor. The FET current is monitored during start-up and normal operation.

Overload Protection

Set the current limit using the following formula:

$$V_{ILIM} = (I_{OUT} * GAIN_{ILIM}) * R_{ILIM}$$

where,

• $GAIN_{IMON}$ is the gain factor I_{ILIM}: I_{OUT} = 27.9 µA/A (Typical)

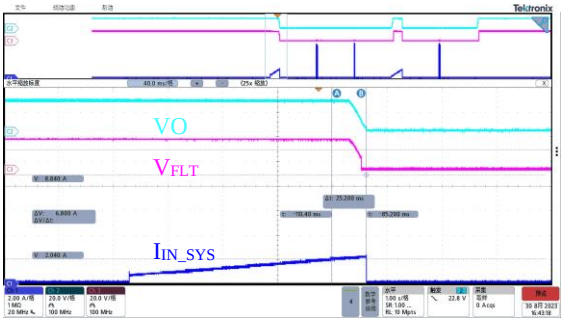
• I_{OUT} is the load current

• R_{ILIM} is the current limit resistor in K Ω

Active Current Limiting with I_{OL} Pulse Current Support

TPS26630 after the start-up and with PGOOD high, if the load current reaches to I_{OL}, the device will pass through the over current demanded by the load not more than I_{OL}. Power dissipation across the device during this operation will be (V_{IN} – V_{OUT}) x I_{OL} and this could heat up the device and eventually enter thermal shutdown. If load current reaches to 1.5 x I_{OL}, the internal FET is shut down immediately.

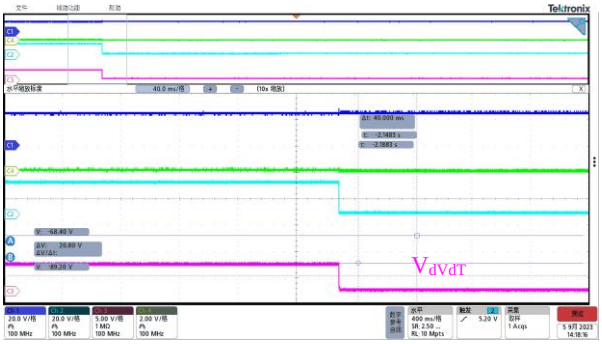
The I_{OL} pulse current support is activated only after PGOOD goes high. If PGOOD is in low state such as during start-up operation or during auto-retry cycles, the I_{OL} pulse current support is not activated， and the device limits the current at I_{OL} level. The following figure illustrate overload current limiting performance.



Overload Performance with TPS26630 during Load Step from 0A to 3A

MODE

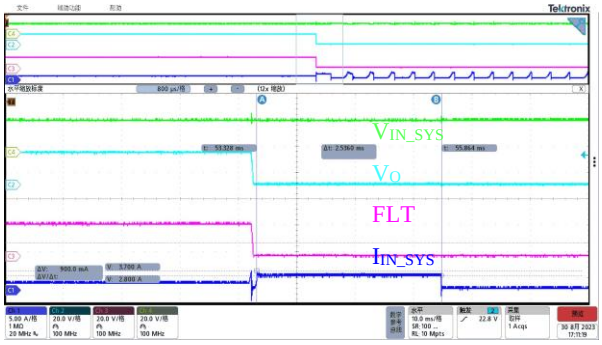
If the voltage of the MODE is less than 1.2V, ILIM pin has short-circuit protection, otherwise don't have short-circuit protection. The TPS26630 features open fault detection. When ILIM enters open or short circuit protection, the internal FET is turned OFF and it remains OFF till the ILIM pin fault is removed.



V_{IN_SYS} = 24V, R_{ILIM} = 6.2kΩ to GND

Short Circuit Protection

During a transient output short circuit event, the current through the device increases rapidly. As the current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the device incorporates a fast-trip comparator. The fast-trip comparator architecture is designed for fast turn OFF $t_{FASTTRIP(dly)}$ = 1µs (typical) with I_{SCP} = 45A of the internal FET during an output short circuit event. The fast-trip threshold is internally set to $I_{FASTTRIP}$. The fast trip circuit holds the internal FET off for only a few microseconds, after which the device turns back on slowly, allowing the current-limit loop to regulate the output current to I_{OL}. Then the device functions is similar to the overload condition. The following figure illustrates output hot-short performance of the device.



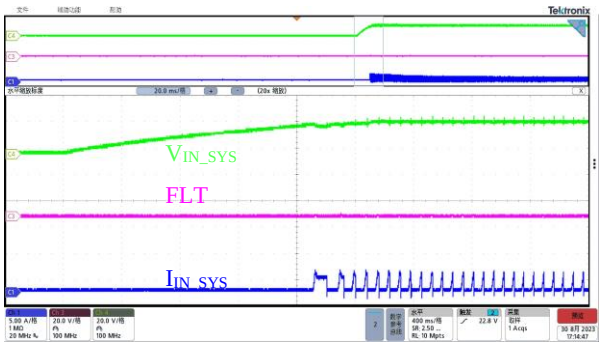
V_{IN_SYS} = 24V R_{ILIM} = 20KΩ

Output Hot-Short Response

The fast-trip comparator architecture has a supply line noise immunity resulting in a robust performance in noisy environments. This is achieved by controlling the turn OFF time of the internal FET based on the overcurrent level, $I_{FASTTRIP}$ through the device. Higher the overcurrent, faster the turn OFF time, $t_{FASTTRIP(dly)}$. At overload current level in the range of $I_{FASTTRIP}$ < I_{OUT} < I_{SCP} the fast-trip comparator response is 3.2µs (typical).

Start-Up With Short-Circuit on Output

When the device is started with short-circuit on the output, the current begins to limit at I_{OL}. Due to high power dissipation of V_{IN} x I_{OL} within the device the junction temperature increases. $\overline{FLT}$ remains asserted till the output short-circuit is removed. The following figure illustrates the behavior of the device in this condition.



V_{IN} = 24V R_{ILIM} = 20kΩ

Start-Up With Short on Output

Current Monitoring Output (IMON)

The TPS26630RG features an accurate analog current monitoring output. A current source at I_{MON} terminal is internally configured to be proportional to the current flowing from IN to OUT. This current can be converted into a voltage using a resistor R_{IMON} from I_{MON} terminal to GND terminal. The I_{MON} voltage can be used as a means of monitoring current flow through the system. The maximum voltage $V_{IMONmax}$ for monitoring the current is limited to 4V. This puts a limitation on maximum value of R_{IMON} resistor and is determined by the following formula:

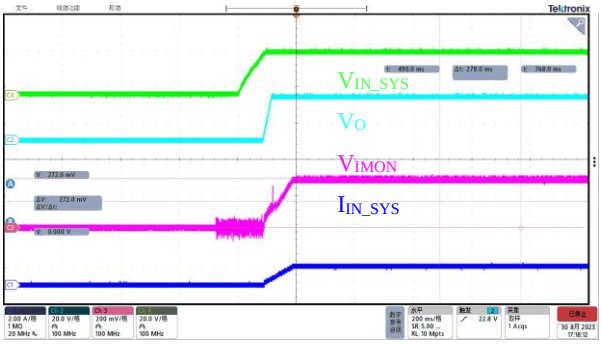
$$V_{IMOM} = (I_{OUT} * GAIN_{IMON}) * R_{IMON}$$

where,

• $GAIN_{IMON}$ is the gain factor I_{IMON}: I_{OUT} = 27.9 µA/A (Typical)

• I_{OUT} is the load current

The following figure illustrates I_{MON} performance.



I_{MON} Response During a Load Step

The I_{MON} pin must not have a bypass capacitor to avoid delay in the current monitoring information.

FAULT Response ($\overline{FLT}$)

The $\overline{FLT}$ open-drain output asserts (active low) under the fault's events such as undervoltage, overvoltage, overload, power limiting, reverse current, I_{LIM} pin short and thermal shutdown conditions. The device is designed to eliminate false reporting by using an internal "de-glitch" circuit for fault conditions without the need for an external circuitry. $\overline{FLT}$ can be left open or connected to GND when not used.

IN_SYS, IN, OUT and GND Pins

Connect a minimum of 0.1uF capacitor across IN_SYS and GND. For systems and applications where reverse polarity protection and/or reverse current blocking feature is required

• Connect a N-channel FET between IN_SYS and IN with source of the FET connected to IN_SYS, Drain at IN, and GATE to BGATE.

• Connect a N-channel signal FET with GATE to DRV, Drain to BGATE, Source to IN_SYS.

If the external N-channel FET is not used, then connect IN_SYS and IN together and leave BGATE and DRV pins floating. Do not leave any of the IN and OUT pins un-connected.

Thermal Shutdown

The device has a built-in overtemperature shutdown circuitry designed to protect the internal FET, if the junction temperature exceeds T_{TSD}, 130°C (typical). After the thermal shutdown event, the device commences an auto-retry cycle of 660ms (typical), t_{TSD_retry} after $T_J < [T_{TSD} – 11°C]$. During the thermal shutdown, the fault pin $\overline{FLT}$ pulls low to indicate a fault condition.

Low Current Shutdown Control ($\overline{SHDN}$)

The internal, external FET and hence the load current can be switched off by pulling the $\overline{SHDN}$ pin below 0.8V threshold with a micro-controller GPIO pin or can be controlled remotely with an opto-isolator device. The device quiescent current reduces to 10μA (typical) in shutdown state. To assert $\overline{SHDN}$ low, the pull down must have sinking capability of at least 10μA. To enable the device, $\overline{SHDN}$ must be pulled up to at least 2V. Once the device is enabled, the internal FET turns on with dVdT mode.

Layout considerations

• For all the applications, a 0.1μF or higher value ceramic decoupling capacitor is recommended between IN_SYS terminal and GND.

• The external FET Q1 should be placed with DRAIN close to the VIN pins of TPS26630 and connected through a plane. The fast pulldown switch Q2 DRAIN, and SOURCE should be placed very close to the GATE and SOURCE terminals of Q1 with very short loop.

• The optimum placement of decoupling capacitor is closest to the IN_SYS and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN_SYS terminal, and the GND terminal of TPS26630.

• High current carrying power path connections must be as short as possible and must be sized to carry at least twice the full-load current.

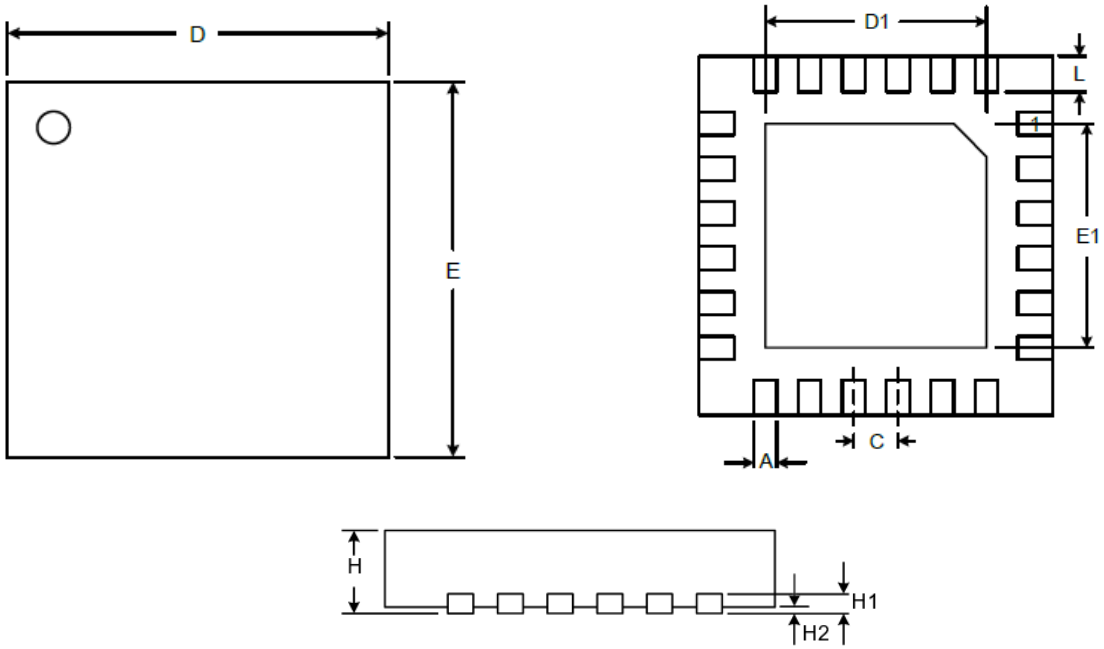
• Locate TPS26630 support components R_{ILIM}, C_{dVdT}, R_{IMON}, UVLO, OVP and PGTH resistors close to their connection pin. Connect the other end of the component to the GND with shortest trace length.

• The trace routing for the R_{ILIM} component to the device must be as short as possible to reduce parasitic effects on the current limit and current monitoring accuracy. These traces must not have any coupling to switching signals on the board.

• Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT and GND pins.

• Thermal Considerations: When properly mounted, the Power PAD package provides significantly greater cooling ability. To operate at rated power, the Power PAD must be soldered directly to the board GND plane directly under the device. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications.

Package information



SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.18	0.25	0.30
C		0.50	
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D1	2.60	2.70	2.80
E1	2.60	2.70	2.80
L	0.35	0.40	0.45
H	0.7	0.75	0.8
H1		0.203	
H2	0.00	0.025	0.05

QFN4*4-24L for TPS26630RGER