High–Performance Silicon–Gate CMOS

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 5.0 V
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 100 FETs or 25 Equivalent Gates

DIP-16

SOP-16

TSSOP-16

Package/Ordering Information

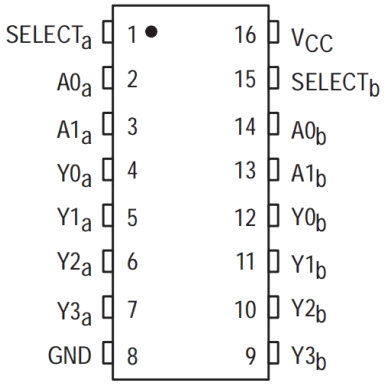
DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC139N	DIP-16	74HC139	TUBE	1000pcs/Box
74HC139M/TR	SOP-16	74HC139	REEL	2500pcs/Reel
74HC139MT/TR	TSSOP-16	HC139	REEL	2500pcs/Reel

General Description

The 74HC139 is identical in pinout to the LS139. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

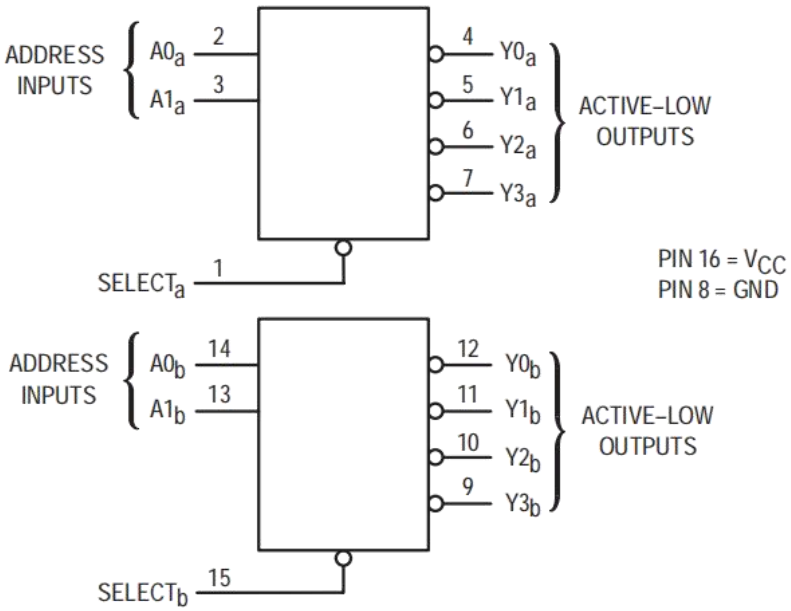
This device consists of two independent 1–of–4 decoders, each of which decodes a two–bit Address to one–of–four active–low outputs. Active–low Selects are provided to facilitate the demultiplexing and cascading functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and utilizing the Select as a data input.

Pin Assignment



DIP-16/SOP-16/TSSOP-16

Logic Diagram



Function Table

Inputs			Outputs			
Select	A1	A0	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

X = don't care

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	20	mA
I_{out}	DC Output Current, per Pin	25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	50	mA
P_D	Power Dissipation in Still Air, Plastic DIP† SOP Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	℃
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOP Package)	260	℃

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/℃ from 65 to 125℃
SOP Package: – 7 mW/℃ from 65 to 125℃

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	5.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+ 85	℃
t_r, t_f	Input Rise and Fall Time(Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 5.0 V	0	1000 500 400	ns

Dc Electrical Characteristics (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				-40 to25℃	85℃	125℃	
V_{IH}	Minimum High–Level InputVoltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ 20μA	2.0 4.5 5.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low–Level InputVoltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ 20μA	2.0 4.5 5.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High–Level OutputVoltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ 20μA	2.0 4.5 5.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ 4.0 mA $\|I_{out}\|$ 5.2 mA	4.5 5.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low–Level OutputVoltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ 20μA	2.0 4.5 5.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ 4.0 mA $\|I_{out}\|$ 5.2 mA	4.5 5.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.0	4	40	160	μA

Ac Electrical Characteristics (CL = 50 pF, Input tr = tf = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			-40 to25℃	85℃	125℃	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Select to Output Y(Figures 1 and 3)	2.0 4.5 5.0	115 23 20	145 29 25	175 35 30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y(Figures 2 and 3)	2.0 4.5 5.0	115 23 20	145 29 25	175 35 30	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output(Figures 1 and 3)	2.0 4.5 5.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Per Decoder)*		Typical @ 25℃, V_{CC} = 5.0 V 55			pF

Switching Waveforms

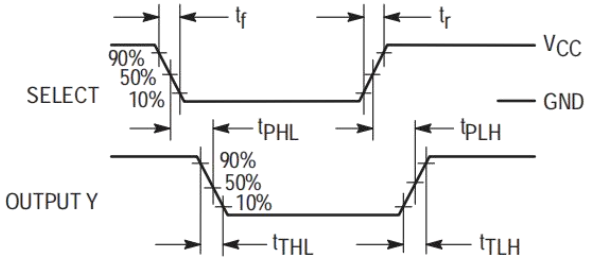


Figure 1.

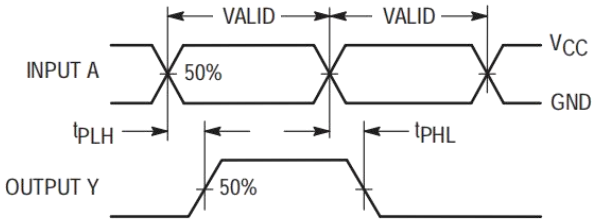
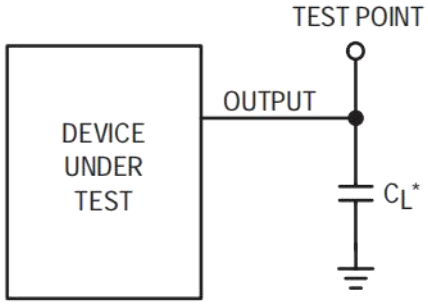


Figure 2.



*Includes all probe and jig capacitance

Figure 3. Test Circuit

Pin Descriptions

ADDRESS INPUTS

A0a, A1a, A0b, A1b (Pins 2, 3, 14, 13)

Address inputs. These inputs, when the respective 1–of–4 decoder is enabled, determine which of its four active–low outputs is selected.

CONTROL INPUTS

Selecta, Selectb (Pins 1, 15)

Active–low select inputs. For a low level on this input, the outputs for that particular decoder follow the Address inputs. A high level on this input forces all outputs to a high level.

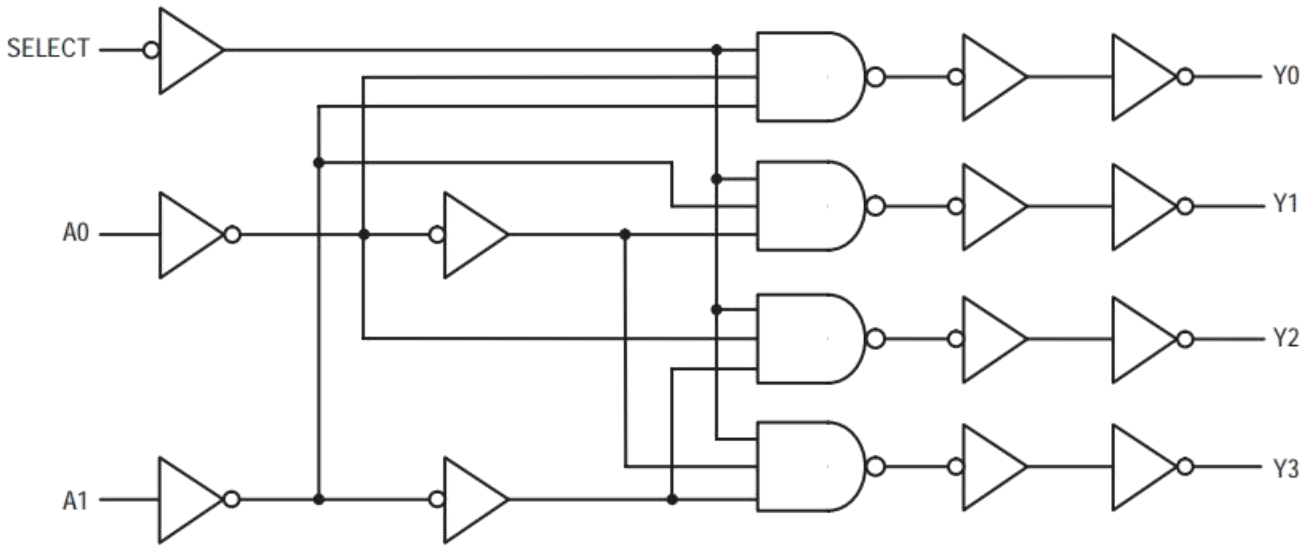
OUTPUTS

Y0a – Y3a, Y0b – Y3b (Pins 4 – 7, 12, 11, 10, 9)

Active–low outputs. These outputs assume a low level when addressed and the appropriate Select input is active. These outputs remain high when not addressed or the appropriate Select input is inactive.

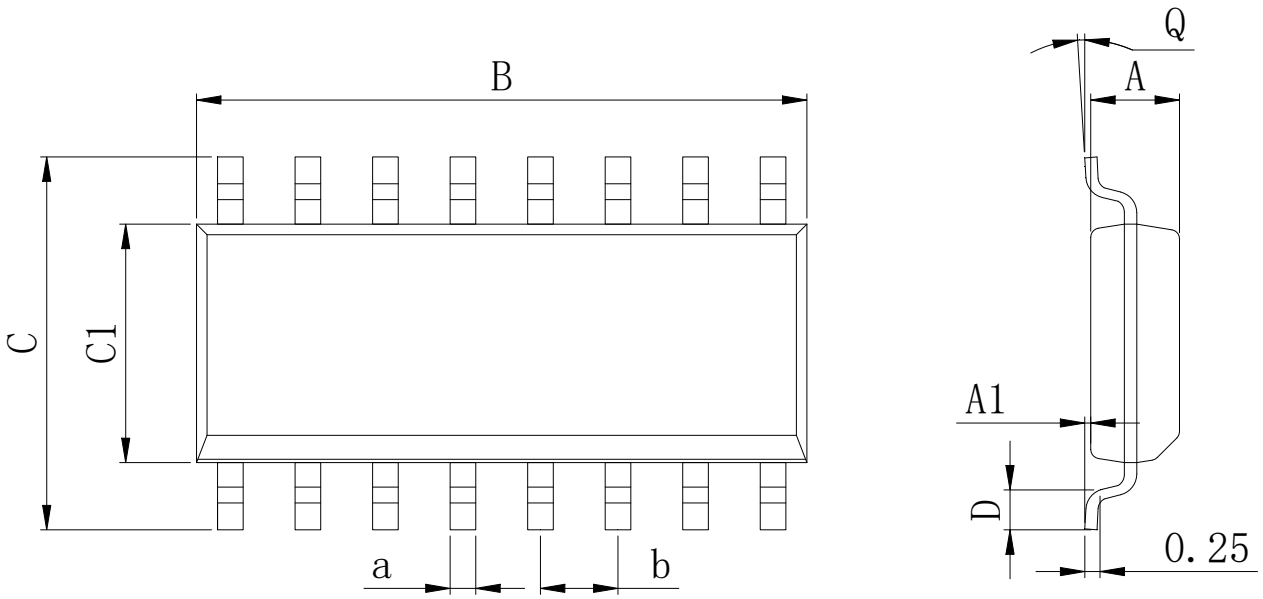
EXPANDED LOGIC DIAGRAM

(1/2 OF DEVICE)



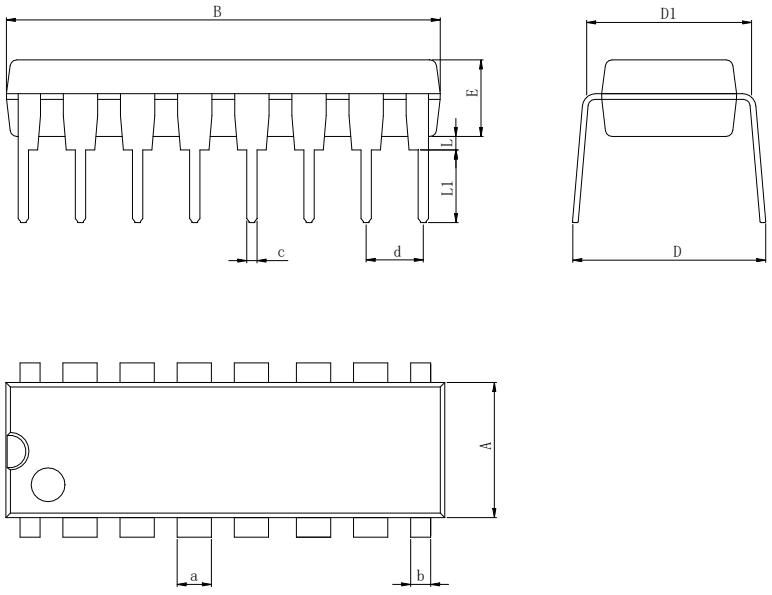
Physical Dimensions

SOP-16



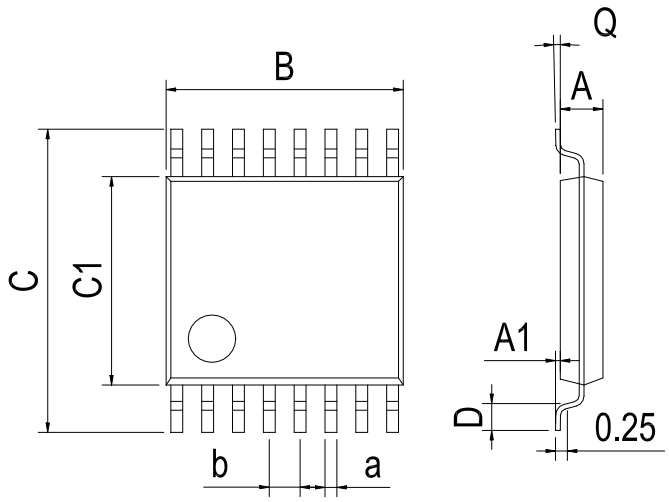
Dimensions In Millimeters(SOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	9.80	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	10.0	6.20	4.00	0.80	8°	0.45	

DIP-16



Dimensions In Millimeters(DIP-16)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

TSSOP-16



Dimensions In Millimeters(TSSOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

Revision History

DATE	REVISION	PAGE
2016-3-8	New	1-10
2023-9-18	Modify the package dimension diagram TSSOP-16、Updated DIP-16 dimension	7、8
2024-11-5	Update Lead Temperature	3

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