# VP3677

## *High-Efficiency Full Bridge Buck-Boost DC/DC Controller*

## General Description

The VP3677 is a high efficiency full-bridge buck-boost DC/DC controller designed for use in voltage step-up or step-down converting application. It operates over a wide input range from 4.2V to 55V and is capable of adjusting output voltage to 55V. Current mode control scheme also makes it wide bandwidth and good transient response. The operating frequency can be adjusted simply with an external resistor or any external clock source between 100kHz and 600kHz. Its internal gate driver provides 2A peak current driving capability.

The VP3677 also provides input/output average current sensing and limiting function, optional EMI improvement and power status indication pin. This device features lots of protection such as cycle-by-cycle current limiting, input under-voltage lockout, output over voltage, short, over-temperature and optional hiccup mode in sustained overload conditions. Programmable soft-start circuitry reduces the inrush current at start-up.

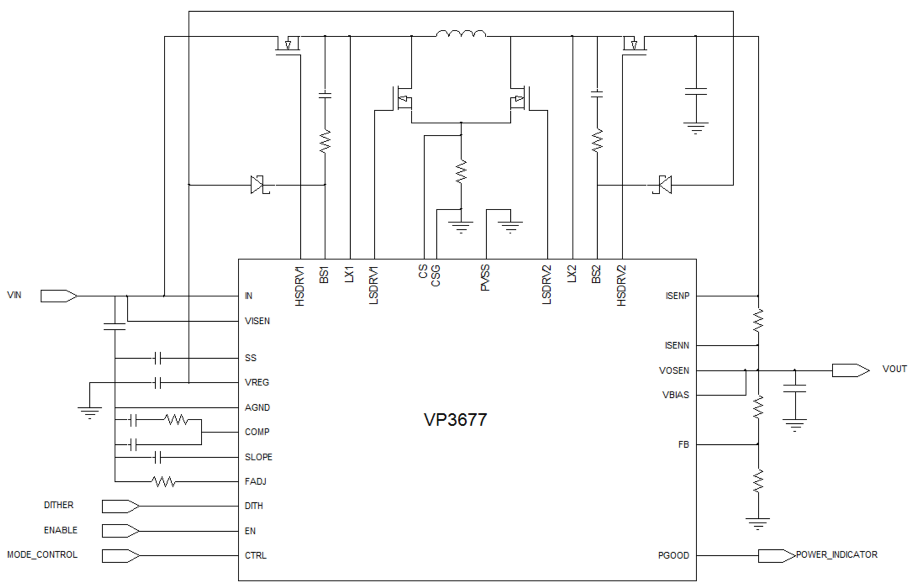
## Features

- 4-Switch Step-Up/Step-Down Operation
- Wide Input Voltage from 4.2V to 55V
- Adjustable Output Voltage from 0.8V to 55V
- Adjustable 100kHz~600kHz Clock Frequency
- Optional Frequency Synchorization/Dithering
- 2A Peak Driving Current
- Current Mode Operation
- External RC Compensation
- Programmable Soft-Start and Input UVLO
- Power Good Indication
- Output Over-Voltage Protection
- Output Short Voltage Protection
- Current Limit and Over Temperature Protection
- TSSOP28EP Exposed Pad and QFN28 4x5 Green Package with RoHS Compliant

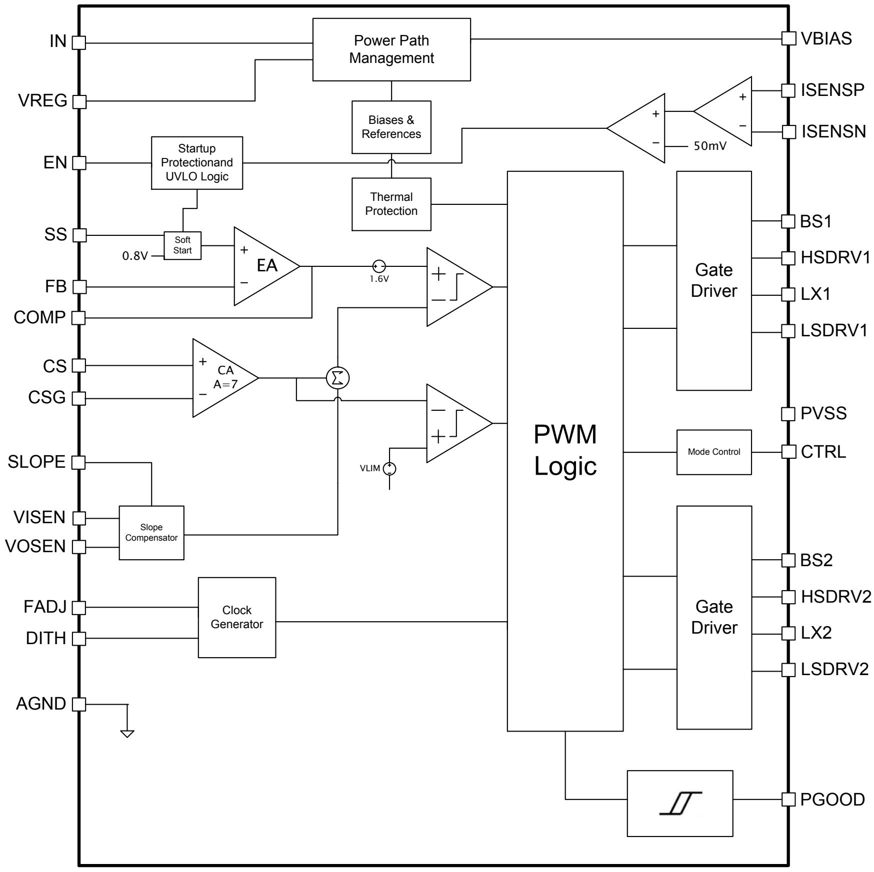
## Applications

- USB Power Delivery
- Industrial Power Supplies
- Battery and Super-Capacitor Charging
- LED Lighting
- Automotive Start/Stop Systems

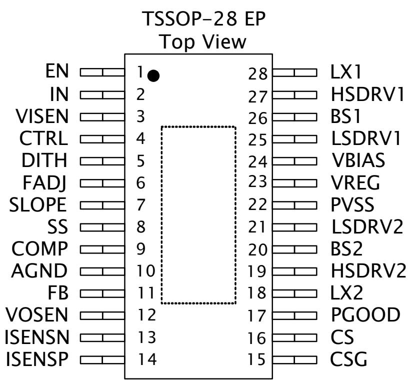
## Typical Application

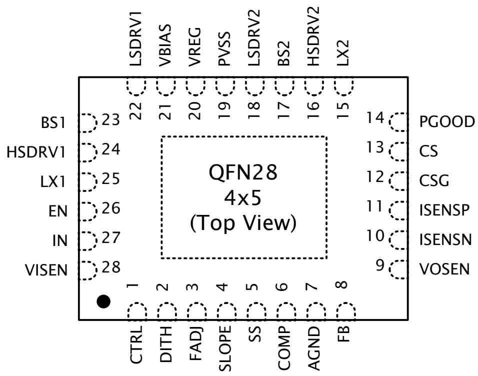


## Functional Block Diagram




## Pin Assignments



## Pin Descriptions

| TSSOP | QFN | Pin | I/O/P | Function Description |
|---|---|---|---|---|
| 1 | 26 | EN | I | Chip Enable. For EN<0.7V, the VP3677 enters shutdown mode. For 0.7V<EN<1.23V, VREG is enabled but no PWM switching. For EN>1.3V, PWM switching is enabled. TTL Logic levels with compliance to $V_{IN}$. |
| 2 | 27 | IN | P | Power Supply Input. Connect this pin to power supply. |
| 3 | 28 | VISEN | I | Input Voltage Sense Input. Connect this pin close to input capacitors. |
| 4 | 1 | CTRL | I | Mode Control. Connect a resistor to ground to configure Forced CCM operation and CCM hiccup mode. See functional description for setting table. |
| 5 | 2 | DITH | I | Frequency Dithering Adjust. Connect a capacitor to ground to make the VP3677 PWM modulation frequency swing in ±5% of the frequency specified by FADJ external resistor. Leave this pin unconnected for disabling this feature. |
| 6 | 3 | FADJ | I | Frequency Adjust or Synchronization. A resistor connected from this pin to ground simply sets the oscillator frequency. An external clock signal at this pin will synchronize the controller. |
| 7 | 4 | SLOPE | I | Slope Compensation. Connect a capacitor to ground to perform slope compensation for buck-boost operating stabilization. |
| 8 | 5 | SS | I | Soft-Start Programming. Connect a capacitor to ground to program the soft-start time. |
| 9 | 6 | COMP | O | Compensation. Use a Type II RC//C network to do proper loop compensation. |
| 10 | 7 | AGND | P | Analog Ground. |
| 11 | 8 | FB | I | Output Feedback. Connect the external resistor divider network from output to this pin to sense output voltage. |
| 12 | 9 | VOSEN | I | Output Voltage Sense Input. Connect this pin close to output capacitors. |
| 13 | 10 | ISENSN | I | Average Current Limit Negative Input. |
| 14 | 11 | ISENSP | I | Average Current Limit Positive Input. |
| 15 | 12 | CSG | I | Negative Current Amplifier Input. |
| 16 | 13 | CS | I | Positive Current Amplifier Input. |
| 17 | 14 | PGOOD | OD | Power Good Indicator (Open Drain). PGOOD is pulled low if FB pin is outside specified $V_{FB}$ regulation. |
| 18 | 15 | LX2 | I | 2nd Switching Node. LX2 is the 2nd switching node. |
| 19 | 16 | HSDRV2 | O | 2nd High-Side Drive Pin. |
| 20 | 17 | BS2 | - | Bootstrap I/O for 2nd High-Side Switch. |
| 21 | 18 | LSDRV2 | O | 2nd Low-Side Drive Pin. |
| 22 | 19 | PVSS | P | Power Ground. The ground connection to all low-side gate drivers. |
| 23 | 20 | VREG | O | Internal Regulator. Connect a capacitor to ground. |
| 24 | 21 | VBIAS | I | Output Bias Connection. Connect this pin to output to improve efficiency. |
| 25 | 22 | LSDRV1 | O | 1st Low-Side Drive Pin. |
| 26 | 23 | BS1 | - | Bootstrap I/O for 1st High-Side Switch. |
| 27 | 24 | HSDRV1 | O | 1st High-Side Drive Pin. |
| 28 | 25 | LX1 | I | 1st Switching Node. LX1 is the 1st switching node. |
| - | - | Exposed Pad | P | Thermal Ground. The pad should be soldered to the analog ground with low thermal resistance. |

## Absolutely Maximum Ratings

Over operating free-air temperature range, unless otherwise specified (* 1)

| Symbol | Parameter | Limit | Unit |
|---|---|---|---|
| $V_{IN}$ | Supply voltage range | -0.3 to 60 | V |
| $V_{IN(HV)}$ (EN/VISEN/VOSEN/ ISENSP/ISENSN) | High voltage input range | -0.3 to 60 | V |
| $V_{IN(HV)}$(VBIAS) | High voltage bias input range | -0.3 to 60 | V |
| $V_{IN(LV)}$ (COMP/FB/SS/DITH/ FADJ/SLOPE) | Low voltage input range | -0.3 to 3.6 | V |
| $V_{REG}$(VREG/CTRL/PGOOD) | Internal regulator related pin input | -0.3 to 6 | V |
| LSDRV1,LSDRV2<br>BS1, HSDRV1 to LX1<br>BS2, HSDRV2 to LX2 | Input voltage range | -0.3 to 6 | V |
| $V_{SW}$(LX1/LX2) | Switch node voltage | LX1: -1 to 60<br>LX2: -1 to 60 | V |
| $V_{BS}$(BS1,BS2) | Bootstrap node voltage | BS1: -0.3 to 60<br>BS2: -0.3 to 60 | V |
| CS, CSG | Sense pins differential input voltage range | -0.3 to 0.3 | V |
| $T_{J(MAX)}$ | Operating junction temperature range | 150 | °C |
| $T_{STG}$ | Storage temperature range | -65 to 150 | °C |
| Electrostatic discharge | Human body model | 2 | kV |
| Electrostatic discharge | Machine model | 200 | V |
| $\theta_{JC(TSSOP28)}$ | TSSOP28 Thermal resistance (Junction to Case) | 16 | °C/W |
| $\theta_{JC(QFN28)}$ | QFN28 Thermal resistance (Junction to Case) | 13 | °C/W |
| $\theta_{JA(TSSOP28)}$ | TSSOP28 Thermal resistance (Junction to Air) | 37 | °C/W |
| $\theta_{JA(QFN28)}$ | QFN28 Thermal resistance (Junction to Air) | 34 | °C/W |

( *1): Stress beyond those listed at table above may cause permanent damage to the device. These are stress rating ONLY. For functional operation are strongly recommend follow up "recommended operation conditions" table.

## Recommended Operating Conditions

| Symbol | Parameter | Specification | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{IN}$(IN) | Supply voltage | 4.2 | 55 | V |
| $V_{IN}$(VISEN) | Supply Input with VBIAS connected (VBIAS≥5V or IN≥4.5V) | 2.5 | 55 | V |
| VBIAS | Auxiliary supply voltage | 6 | 36 | V |
| $V_{IN}$(VOSEN) | Output sense input voltage | 0.8 | 55 | V |
| EN | Enable pin input voltage | 0 | 55 | V |
| ISENSP, ISENSN | Sense pin input voltage | 0 | 55 | V |
| $f_{OSC}$ | Switching voltage range | 100 | 600 | kHz |
| $T_A$ | Operating free-air temperature range | -40 | 85 | °C |
| $T_J$ | Operating temperature range | -40 | 125 | °C |

## Electrical Characteristics

Operating condition $V_{IN}$=24V, $C_{SS}$=0.1μF, $T_J$=25℃, unless otherwise specified (* 1)

| Symbol | Parameter | Test Condition | Specification | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ. | Max | |
| **SUPPLY VOLTAGE** | | | | | | |
| $V_{IN}$ | Input voltage | | 4.2 | | 55 | V |
| $I_{SD}$ | Shutdown mode supply current | $V_{EN}$=0V | | 12 | 16 | μA |
| $I_{STBY}$ | Standby mode supply current | $V_{EN}$=1.1V, non-switching | | 1 | 2 | mA |
| $I_Q$ | Operating current | $V_{EN}$=2V, $V_{FB}$=0.9V | | 2.19 | 4 | mA |
| **ENABLE/UVLO** | | | | | | |
| $V_{EN(STBY)}$ | Standby threshold voltage | $V_{EN}$ rising | 0.55 | 0.79 | 0.97 | V |
| $I_{EN(STBY)}$ | Standby mode pin source current | $V_{EN}$=1.1V | | 2 | 3 | μA |
| $V_{EN(OPER)}$ | Operating threshold voltage | $V_{EN}$ rising | 1.17 | 1.23 | 1.29 | V |
| $I_{HYS(OPER)}$ | Operating hysteresis current | $V_{EN}$=2.4V | 1.5 | 3.5 | 5.5 | μA |
| **VBIAS** | | | | | | |
| $V_{VBIAS(SW)}$ | Internal bias switchover voltage | | | 5.75 | | V |
| **ERROR AMPLIFIER** | | | | | | |
| $V_{FB}$ | Feedback reference voltage | $V_{EN}$=2V, FB connect to COMP | 0.788 | 0.8 | 0.812 | V |
| $I_{FB}$ | Feedback bias current | $V_{FB}$ in regulation | | | 0.1 | μA |
| BW | Unity gain bandwidth | | | 2 | | MHz |
| $I_{COMP}$ | COMP source current | FB=$V_{REF}$−300mV, COMP=0V | | 306 | | μA |
| | COMP sink current | FB=$V_{REF}$+300mV, COMP=3V | | 309 | | |
| $g_{M(EA)}$ | Error amplifier trans-conductance | | | 1490 | | μS |
| **VREG** | | | | | | |
| $V_{REG}$ | Internal regulation voltage | EN=2V, VBIAS pin open, VREG pin open | 5.1 | 5.3 | 5.5 | V |
| $V_{UV}$ | VREG UVLO threshold | $V_{REG}$ rising | | 3.3 | | V |
| $R_{OUT(VREG)}$ | LDO Output impedance | $I_{OUT}$=0.03A, $V_{IN}$=3.5V | | 9.3 | 16 | Ω |
| | UVLO hysteresis | | | 100 | | mV |
| $I_{OUT(VREG)}$ | VREG maximum supply current | $V_{IN}$=3.5V, $V_{REG}$=0V | | 80 | | mA |
| **PGOOD** | | | | | | |
| $V_{PGOOD}$ | PGOOD trip ratio for FB (Falling) | Ratio to $V_{FB}$ | | -9 | | % |
| | PGOOD trip ratio for FB (Rising) | Ratio to $V_{FB}$ | | 10 | | % |
| | Hysteresis | | | 1.6 | | % |
| $I_{LEAK(PGOOD)}$ | PGOOD leakage current | FB=0.8V, $V_{PGOOD}$=5V | | | 100 | nA |
| $I_{SINK(PGOOD)}$ | PGOOD sink current | FB=0V, $V_{PGOOD}$=0.4V | 2 | 4.2 | 6.5 | mA |

( *1): Stress beyond those listed at "absolute maximum rating" table may cause permanent damage to the device. These are stress rating ONLY. For functional operation are strongly recommend follow up "recommended operation conditions" table.

## Electrical Characteristics (cont.)

Operating condition $V_{IN}$=24V, $C_{SS}$=0.1μF, $T_J$=25℃, unless otherwise specified (* 1)

| Symbol | Parameter | Test Condition | | Specification Min | Specification Typ. | Specification Max | Unit |
|---|---|---|---|---|---|---|---|
| **FREQUENCY/SYNC/DITHER** | | | | | | | |
| $PW_{SYNC}$ | SYNC input pulse width | | | 75 | | 500 | ns |
| $f_{sw}$ | PWM switching frequency | $V_{FB}$=0.7V | $R_T$=133kΩ | | 200 | | kHz |
| | | | $R_T$=47kΩ | | 500 | | kHz |
| $V_{SYNCH}$ | SYNC input high threshold | | | 2.1 | | | V |
| $V_{SYNCL}$ | SYNC input low threshold | | | | | 1.2 | V |
| $V_{DITHER}$ | Dither high threshold | | | | 1.27 | | V |
| | Dither low threshold | | | | 1.16 | | V |
| $I_{DITHER}$ | Dither source/sink current | DITHER=1.1V, DITHER=1.3V | | | 10.5 | | μA |
| **SOFT START** | | | | | | | |
| $I_{SS}$ | Soft start pull-up current | $V_{SS}$=0V | | 4.30 | 6 | 7.25 | μA |
| $V_{SS(CL)}$ | Soft start clamp voltage | SS open | | | 1.31 | | V |
| $\Delta V_{FB}-V_{SS}$ | FB to SS offset voltage | $V_{SS}$=0V | | | -15 | | mV |
| **GATE DRIVER** | | | | | | | |
| $I_{HSDRV1,2}$ | Gate driver peak source current | $V_{BS1}-V_{LX1}$=5.3V | | | 1.8 | | A |
| | Gate driver peak sink current | $V_{BS1}-V_{LX1}$=5.3V | | | 2.2 | | A |
| $I_{LSDRV1,2}$ | Gate driver peak source current | $V_{BS2}-V_{LX2}$=5.3V | | | 1.8 | | A |
| | Gate driver peak sink current | $V_{BS2}-V_{LX2}$=5.3V | | | 2.2 | | A |
| $R_{HSDRV1,2}$ | Gate driver pull-up resistance | $V_{BS1,2}-V_{LX1,2}$=5.3V | | | 1.9 | | Ω |
| | Gate driver pull-down resistance | $V_{BS1,2}-V_{LX1,2}$=5.3V | | | 1.3 | | Ω |
| $R_{LSDRV1,2}$ | Gate driver pull-up resistance | $I_{LSDRV1,2}$=0.1A | | | 2 | | Ω |
| | Gate driver pull-down resistance | $I_{LSDRV1,2}$=0.1A | | | 1.5 | | Ω |
| $V_{UV(BS1,2)}$ | BS1,2 to LX1,2 UVLO threshold | HSDRV1,2 shut off | | | 2.73 | | V |
| | BS1,2 to LX1,2 UVLO hysteresis | HSDRV1,2 begin switching | | | 280 | | mV |
| | BS1,2 to LX1,2 threshold for re-fresh pulse | | | | 4.45 | | V |
| $t_{DTH}$ | HSDRV1,2 off to LSDRV1,2 on dead time | | | | 45 | | ns |
| $t_{DTL}$ | LSDRV1,2 off to HSDRV1,2 on dead time | | | | 45 | | ns |
| **OUTPUT OVP** | | | | | | | |
| $V_{OVP}$ | Output overvoltage threshold | Relative to FB | | | 0.86 | | V |
| | Output overvoltage hysteresis | | | | 21 | | mV |

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## Electrical Characteristics (cont.)

Operating condition $V_{IN}$=24V, $C_{SS}$=0.1μF, $T_J$=25℃, unless otherwise specified (* 1)

| Symbol | Parameter | Test Condition | Specification | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ. | Max | |
| **CURRENT LIMIT** | | | | | | |
| $V_{CS(BUCK)}$ | Buck mode current limit threshold (Valley) | $V_{IN}=V_{VISNS}$=24V, $V_{VOSNS}$=12V, $V_{SLOPE}$=0V | 53.2 | 85 | 98 | mV |
| $V_{CS(BOST)}$ | Boost mode current limit threshold (Peak) | $V_{IN}=V_{VISNS}$=12V, $V_{VOSNS}$=18V, $V_{SLOPE}$=0V | 119 | 165 | 221 | mV |
| $I_{BIAS(CS/CSG)}$ | CS/CSG pin bias current | $V_{CS}=V_{CSG}=V_{SLOPE}$=0V | | -95 | | μA |
| $I_{OFFSET(CS/CSG)}$ | CSG pin offset current | $V_{CS}=V_{CSG}=V_{SLOPE}$=0V | | | 14 | μA |
| **CONSTANT CURRENT LOOP** | | | | | | |
| $V_{SNS}$ | Average current loop regulation | $V_{ISNSN}$=24V, sweep ISNSP, Measure $V_{SS}$ | 43 | 50 | 57 | mV |
| $I_{SNS}$ | ISNSN/ISNSP pin bias currents | $V_{IN}=V_{ISNSP}=V_{ISNSN}$=24V | | 7 | | μA |
| $g_{M(CS)}$ | Current sense amplifier trans-conductance | $V_{ISNSP}-V_{ISNSN}$=55mV, $V_{SS}$=0.5V | | 1 | | mS |
| **SLOPE COMPENSATION** | | | | | | |
| $I_{SLOPE}$ | Buck adaptive slope current | $V_{IN}=V_{VISNS}$=24V, $V_{VOSNS}$=12V, $V_{SLOPE}$=0V | 28 | 34 | 40 | μA |
| $I_{SLOPE}$ | Boost adaptive slope current | $V_{IN}=V_{VISNS}$=12V, $V_{VOSNS}$=18V, $V_{SLOPE}$=0V | 16 | 21 | 26 | μA |
| $g_{M(SLOPE)}$ | Slope compensation amplifier trans-conductance | | | 2 | | μS |
| **MODE CONTROL** | | | | | | |
| $I_{MODE}$ | Source current out of CTRL pin | CTRL=0V | 17 | 20 | 23 | μA |
| $V_{CCM\_HIC}$ | CCM with hiccup threshold voltage | | 1.18 | 1.28 | 1.38 | V |
| $V_{CCM}$ | CCM no hiccup threshold voltage | | 2.22 | 2.4 | 2.6 | V |
| **THERMAL PROTECTION** | | | | | | |
| $T_{SHUTDOWN}$ | Thermal shutdown trip point | | | 160 | | ℃ |
| | Thermal shutdown hysteresis | | | 15 | | ℃ |

( *1): Stress beyond those listed at “absolute maximum rating” table may cause permanent damage to the device. These are stress rating ONLY. For functional operation are strongly recommend follow up “recommended operation conditions” table.

## Functional Descriptions

The VP3677 is a high efficiency full bridge buck-boost controller with wide input voltage range. In addition to buck mode and boost mode, VP3677 also operates in buck-boost mode with excellent efficiency and low ripple output voltage when $V_{IN}$ close to $V_{OUT}$.

VP3677 integrates two half-bridge N-channel MOSFET gate drivers and is designed to work with 4 external MOSFET switches. When $V_{IN}$ is greater then $V_{OUT}$, the VP3677 PWM control works in valley current mode. The inductor current should be monitored for cycle-by-cycle current limit and is sensed through an external sense resistor connected to the source of low-side MOSFET switches and power ground.

When $V_{IN}$ is lower then $V_{OUT}$, the VP3677 PWM control works in peak current mode. For the application cases of lower $V_{IN}$ (e.g. below than 5.6V) and higher $V_{OUT}$, VP3677 is capable of supporting bias VBIAS terminal with $V_{OUT}$. In this condition, internal regulator source would be switched from $V_{IN}$ to $V_{OUT}$ for higher gate driver bias so that better switching efficiency would be achieved.

Besides cycle-by-cycle current limiting, the VP3677 supports average current sense scheme for either input or output current detection. Soft-start is also supported with an external capacitor connected to ground to eliminate inrush current and voltage overshoot during startup.

VP3677 supports continuous conduction mode (Forced CCM) for noise sensitive application such as audio or radio frequency use. For the output overload condition VP3677 provides optional hiccup mode to reduce the heat and damage during sustained overload case. If the hiccup mode is disabled the controller remains in a cycle-by-cycle current limit until the overload case is fixed. Use CTRL terminal to configure CCM mode PWM operation and CCM hiccup mode selection.

The VP3677 supports over-voltage protection and power good status indication. If the output feedback voltage exceeds then 7.5% or above nominal reference $V_{REF}$(0.8V) the high side drivers would be turn off. PGOOD terminal would be externally pulled high when FB pin voltage is regulated within +10% and -9% centered with $V_{REF}$.

The VP3677 can operate in shutdown state, standby state and normal operation state. It can be configured with setting EN terminal with 3 distinct voltage ranges.

### Operation States and UVLO

The VP3677 has chip enable and under-voltage lock out protection. When EN pin voltage is below than standby threshold 0.79V, the controller enters the shutdown state and most of the functional blocks are disabled including $V_{REG}$ regulator.

When EN voltage is greater than standby threshold but less than the operating threshold 1.23V, both internal $V_{REG}$ regulator and VBIAS bias input are enabled but the controller will still not start up and hence no switching.

When EN voltage is greater than operating threshold, the controller will start switching if the $V_{REG}$ is also above $V_{REG}$ under-voltage threshold (3.3V). If $V_{REG}$ is still under UV threshold, the VP3677 will not switch. Table 1 shows the relation between the state and EN pin threshold voltage range.

To implement UVLO protection, the simplest way is to use a resistor network from $V_{IN}$ to AGND with the mid-point connect to EN pin. The turn-on threshold can be obtained by equation 1.

## Functional Descriptions (cont.)

$$V_{IN(UVLO)} = 1.23V \times \left(1 + \frac{R_{EN2}}{R_{EN1}}\right) - R_{EN2} \times 1.5\mu A$$
(1)

$$\Delta V_{HYS(UVLO)} = 3.5\mu A \times R_{EN2}$$
(2)

Equation 2 shows the hysteresis between the UVLO turn-on and turn-off threshold and can be obtained with this equation. Beware of the EN pin source current is about 3.5μA when EN pin voltage is above 1.23V.

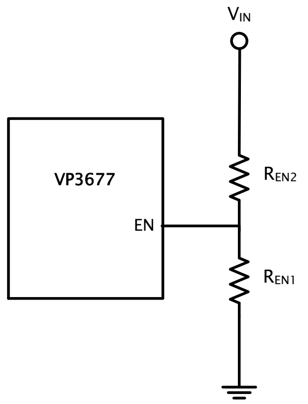



Figure 1. Programming EN pin

| EN | $V_{REG}$ | State |
|---|---|---|
| EN<0.79V | N/A | Shutdown |
| 0.79V<EN<1.23V | N/A | Standby |
| EN>1.23V | $V_{REG}$<3.3V | Standby |
| EN>1.23V | $V_{REG}$>3.3V | Operating, Switching |

Table 1. EN pin threshold voltage

### Frequency Adjustment

It is simply to use an external resistor to adjust the PWM clock frequency. Connect a resistor from FADJ terminal to AGND to program switching frequency from 100kHz to 600kHz. Equation 3 shows how to calculate the external resistor:

$$R_T = \frac{\left(\frac{1}{f_{SW}} - 200ns\right)}{37pF}$$
(3)

The VP3677 can be synchronized with external clock source. Figure 2 demonstrates the connection to AC clock source. The external clock frequency should be higher than resistor programmed frequency. Beware of the pulse width of the external PWM clock should be in range from 75ns to 500ns and the pulse amplitude must not exceed 3.3V.

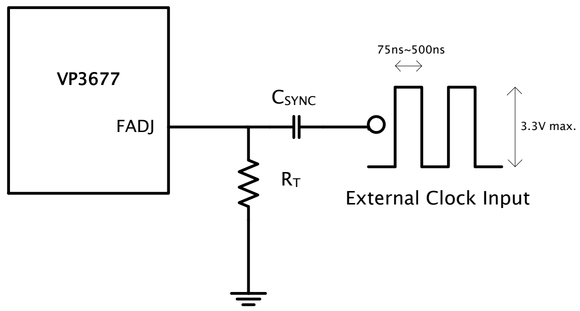



Figure 2. External Clock Synchronization

Frequency dithering is an important skill to improve EMI performance. Connect a capacitor from DITH pin to AGND to enable this function. Equation 4 shows the calculation of dithering capacitance:

$$C_{DITH} = \frac{10\mu A}{f_{SW} \times 0.24V}$$
(4)

Connect the DITH pin to ground to disable this function. Dithering function is also disabled when using external clock input.

### Soft Start

The VP3677 provides soft start scheme to prevent transient during startup and could be adjusted by a soft start capacitor connected from SS terminal to AGND. During powering up, an internal current source charges the soft start capacitor. When the SS pin voltage below the feedback reference $V_{REF}$, soft-start block raises the FB voltage with the same slope as the SS pin. After SS pin voltage exceeds $V_{REF}$, the soft-start period is finished and the output voltage is almost reached to desired output

## Functional Descriptions (cont.)

value. If the FB voltage is still under 0.3V after the soft start progress is finished, the VP3677 will enter standby mode and latched. Soft-start time can be calculated by equation 5:

$$t_{ss} = \frac{C_{SS} \times 0.8V}{6\ \mu A} \quad (5)$$

SS pin will be discharged in the following 3 conditions, EN falling below UVLO voltage and VREG UV threshold, enter hiccup mode and thermal shutdown state. When average current limiting is active, the SS pin would be also discharged by the constant current loop trans-conductance amplifier to limit the current.

### Average Current Limit

To implement current limit protection of input or output, a constant current trans-conductance amplifier is integrated in the VP3677. An additional current sense resistor connected in series with the ISENSP and ISENSP pins to monitor the voltage drop and compare it with internal 50mV reference. If the voltage drop is greater than 50mV then the constant current loop trans-conductance amplifier gradually discharges the soft-start capacitor to pull low the output voltage to limit the input or output current. Use equation 6 to obtain the current limit value. Short ISENSP and ISENSN to disable this function.

$$I_{CL(AVG)} = \frac{50mV}{R_{SENS}} \quad (6)$$

### Forced CCM Operation

For noise sensitive application such as audio amplifier, the switching noise needs to be filtered to prevent any hearable noise. CCM operation the inductor current can flow in either direction and the controller switches at a fixed frequency regardless of the load current.

| CTRL pin | Protection |
|---|---|
| Direct to VREG | Cycle-by-cycle limit |
| Use 91k to AGND | Hiccup |

Table 2. CTRL Pin Selections

Table 2 shows how the CTRL pin configures the protection scheme. The mode is latched at startup.

### Over-current Protection

In buck operation, the sensed valley voltage across $R_{SENSE}$ is limited to 85mV. If the sensed value is not below this threshold during the buck switch off-time, the high-side buck switch skips a cycle. In boost operation, the maximum peak voltage across the $R_{SENSE}$ is limited to 165mV. If the peak current in boost switch causes the CS pin to exceed this threshold, the low-side boost switch is turned-off for the rest of the clock.

Use proper connection networks defined in Table 2 to configure VP3677 in the appropriate working manner. If the hiccup mode is enabled, the controller shuts down after detecting cycle-by-cycle current for 128 cycles and then the soft-start capacitor is discharged. After 4000 clock cycles the SS pin resumes to charge soft-start capacitor again and the controller starts over again. If the hiccup mode is not enabled, the VP3677 will perform cycle-by-cycle current limit when overload condition occurs.

### Output Over-voltage Protection

VP3677 will turns off the 2 gate drivers when the feedback voltage is 7.5% greater than the nominal reference voltage $V_{REF}$. Once the feedback value falls in 5% of $V_{REF}$, the VP3677 resumes switching.

## Functional Descriptions (cont.)

### Internal Regulator and VBIAS Input

Since the VP3677 uses half-bridge gate drivers and high side NMOSFET gate bias should be generated from internal $V_{REG}$ with boot-strap circuits. For $V_{IN}$ is less than the certain of value, the $V_{REG}$ voltage tracks $V_{IN}$ with few voltage drop. Otherwise the internal regulator $V_{REG}$ voltage will be fixed and regulated. The on/off scheme follows the control mechanism of EN pin as previous described.

When $V_{OUT}$ is greater then $V_{REG}$ nominal value plus one more diode drop, the internal regulator will use $V_{OUT}$ to regulate internal $V_{REG}$ instead of using $V_{IN}$. In buck mode, connect VBIAS pin to $V_{OUT}$ with $V_{OUT}$ value greater than 7V will improve the efficiency. Please be aware that the voltage on VBIAS pin should not exceed then 36V.

If $V_{IN}$ is lower and working topology is boost, use higher output voltage and feed it back to $V_{OUT}$ to generate internal $V_{REG}$ is a good idea. For this case, place a series blocking diode between the input power source and IN terminal to prevent VREG back-feeding into IN pin through internal MOSFET body diode.

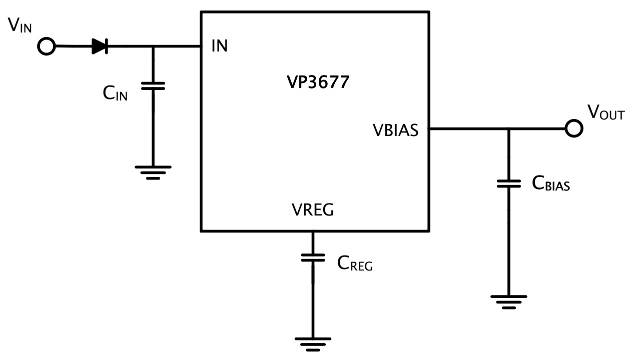



Figure 3. VREG and VBIAS

$V_{REG}$ grounding capacitor is good to use a 1μF ceramic capacitor and is better to be placed close to VREG pin.

Since the VP3677 uses internal LDO to generate internal low-voltage power $V_{REG}$, the method of using VBIAS to supply internal power will essentially generate heat. When the VBIAS pin voltage is low (such as 12V), the $\Delta V^{x}I_{VREG}$ power loss will not have a great impact on VP3677. However, if VBIAS pin voltage is high (greater than 36V), the power loss will significantly increase the temperature of the IC body and then worse the stability and reliability.

To reduce the heat under this operating condition, there are two options to replace the internal LDO with the external power supply. This external power supply can use either an external LDO or a buck regulator. One way is to keep using VBIAS pin and connect extra HV regulator and the other one is to connect external power to VREG instead of using VBIAS pin.

Option #1: Using VBIAS:
For higher VBIAS input ( >36V) or critical environment, connect external power source to VBIAS pin is a good idea. Since internal VBIAS turn over threshold is about 5.6V, using 8V/300mA external regulator is appropriate. Figure 4 demonstrates the connection diagram. Please be aware that the EN pin pull high resistor should be removed or reconfigured if the external regulator PGOOD pin has internal pull high resistor.

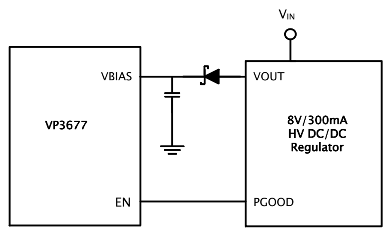



Figure 4. VBIAS External Regulator Connection

If the HV regulator has no PGOOD pin, please refer figure 5 to ensure VBIAS is biased before enabling the VP3677.

## Functional Descriptions (cont.)

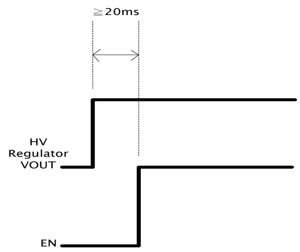



Figure 5. Recommended VOUT/EN on Sequence

Option #2: Using VREG:
If the external MOSFET switches have larger Ciss or multiple MOSFET switches paralleled, it is recommended to connect external power supply to VREG with a blocking diode in series. The concept of such connection is shown in Figure 6.

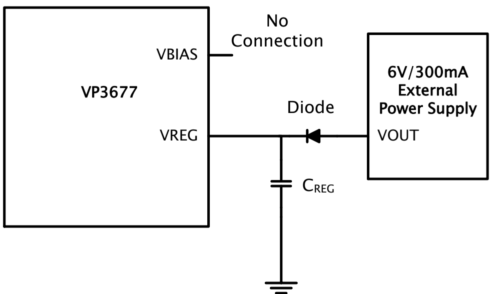



Figure 6. External VREG Supply

Since the nominal voltage of $V_{REG}$ is about 5.3V, external power supply voltage should be approximately 5.5V plus diode V-drop 0.6V. According to these, the output voltage should be regulated at 6V.

With these options and good heating dissipating cooper, the surface temperature of VP3677 would be reduced dramatically.

### Power Good Indicator

PGOOD terminal is pulled high when the voltage at the FB pin is within range of -9%~+10% of the nominal $V_{REF}$ voltage. Otherwise the PGOOD is pulled low. Since the PGOOD is open drain output, it is needed to add pull-up resistor and the pull down strength of the internal MOSFET is about 5.4mA. Since the MOSFET is low voltage device, do not connect the pull-up resistor to 5.5V or higher.

### Slope Compensation

The VP3677 performs a slope compensation based on the current sense signal monitored across the CS and CSG pins with the composition of the $V_{IN}$, $V_{OUT}$ and SLOPE pin signals. The result is compared to the COMP error voltage by PWM modulator.

The current mode controllers require slope compensation for stable current loop operation. In peak current mode the duty is 50% or above and below 50% in valley current mode. Use a capacitor to connect between SLOPE pin and AGND to fine tune optimal slope for various $V_{IN}$ and $V_{OUT}$ combination.

### Loop Compensation

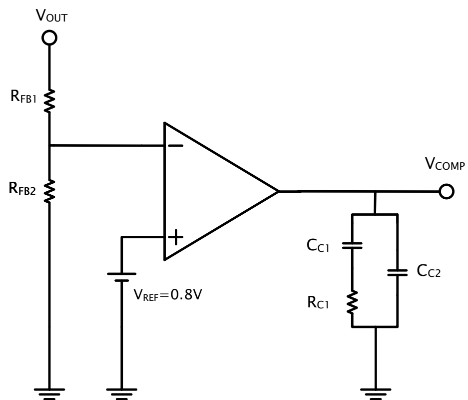



Figure 7. Error Amplifier Compensation Network

## Functional Descriptions (cont.)

Figure 7 shows the internal loop compensation structure. The trans-conductance amplifier output range is from 0.3V to 3V. The COMP pin output range will limit the possible $V_{IN}$ and output current. Type II PI compensation is formed with $R_{C1}$-$C_{C1}$ to AGND in parallel with another pole compensator $C_{C2}$.

The VP3677 will operate in buck, boost and buck-boost mode and the compensation is separated into two considerations. In buck mode, the bottom value of COMP dominates the maximum possible $V_{IN}$ for which the controller can regulate output voltage at no load. Equation 7 shows how to calculate $V_{COMP}$ as function of $V_{IN}$ at no load in PWM operating.

(7)

$$V_{COMP(BUCK)} = 1.6V - A_{CS} \cdot R_{SENSE} \cdot \frac{V_{OUT}}{2 \cdot L1 \cdot F_{SW}} \cdot (1 - D_{BUCK}) - \frac{2\mu S \cdot (V_{IN} - V_{OUT}) + 6\mu A}{C_{SLOPE} \cdot F_{SW}} \cdot (1 - D_{BUCK})$$

Where $D_{BUCK}$ is given by equation 8.

$$D_{BUCK} = \frac{V_{OUT}}{V_{IN}}$$

(8)

To increase the maximum $V_{IN}$ range of buck operation, try to change appropriate frequency, larger inductor, higher $C_{SLOPE}$, smaller sense resistor.

In boost mode, the minimum possible $V_{IN}$ for which the converter can regulate the output at full load is the top value of $V_{COMP}$. Equation 9 shows how to calculate $V_{COMP}$ as function of $V_{IN}$ at full load in PWM operating.

(9)

$$V_{COMP(BOOST)} = 1.6V + A_{CS} \cdot R_{SENSE} \cdot \left( I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}} + \frac{V_{IN}}{2 \cdot L1 \cdot F_{SW}} \cdot D_{BOOST} \right) + \frac{2\mu S \cdot (V_{OUT} - V_{IN}) + 5\mu A}{C_{SLOPE} \cdot F_{SW}} \cdot D_{BOOST}$$

Where $D_{BUCK}$ is given by equation 10.

$$D_{BOOST} = 1 - \frac{V_{IN}}{V_{OUT}}$$

(10)

From equation 9, a larger $L_1$, higher $C_{SLOPE}$, smaller $R_{SENSE}$ and higher frequency could enlarge the $V_{IN}$ range of boost operation.

### Gate Drivers

The VP3677 is a full bridge controller and it contains 4 NMOSFET gate drivers. The buck half bridge drive pins are HSDRV1 and LSDRV1 as well as the boost half bridge drive pins are HSDRV2 and LSDRV2. Each gate driver is capable of sinking 2A and sourcing 1.5A peak current.

The low side gate drivers LSDRV1 and LSDRV2 are biased from $V_{REG}$ and the high side gate drivers HSDRV1 and HSDRV2 are driven from boot-strap capacitors. The boot capacitors are charged and boosted through external schottky diodes connected to VREG terminal. Avoids to use the diodes with greater forward conduction voltage $V_F$ because the high-side gate drives bias will be greatly reduced below than 5V.

### Thermal Protection

The thermal protection circuit monitors the junction temperature and turns off the VP3677 when junction temperature exceeds temperature trip point. When the protection occurs, the soft-start capacitor will be discharged and the gate drivers shut down immediately. The controller will resume switching after soft-start progress when the junction temperature is below then the thermal shutdown hysteresis value.

## Application Information

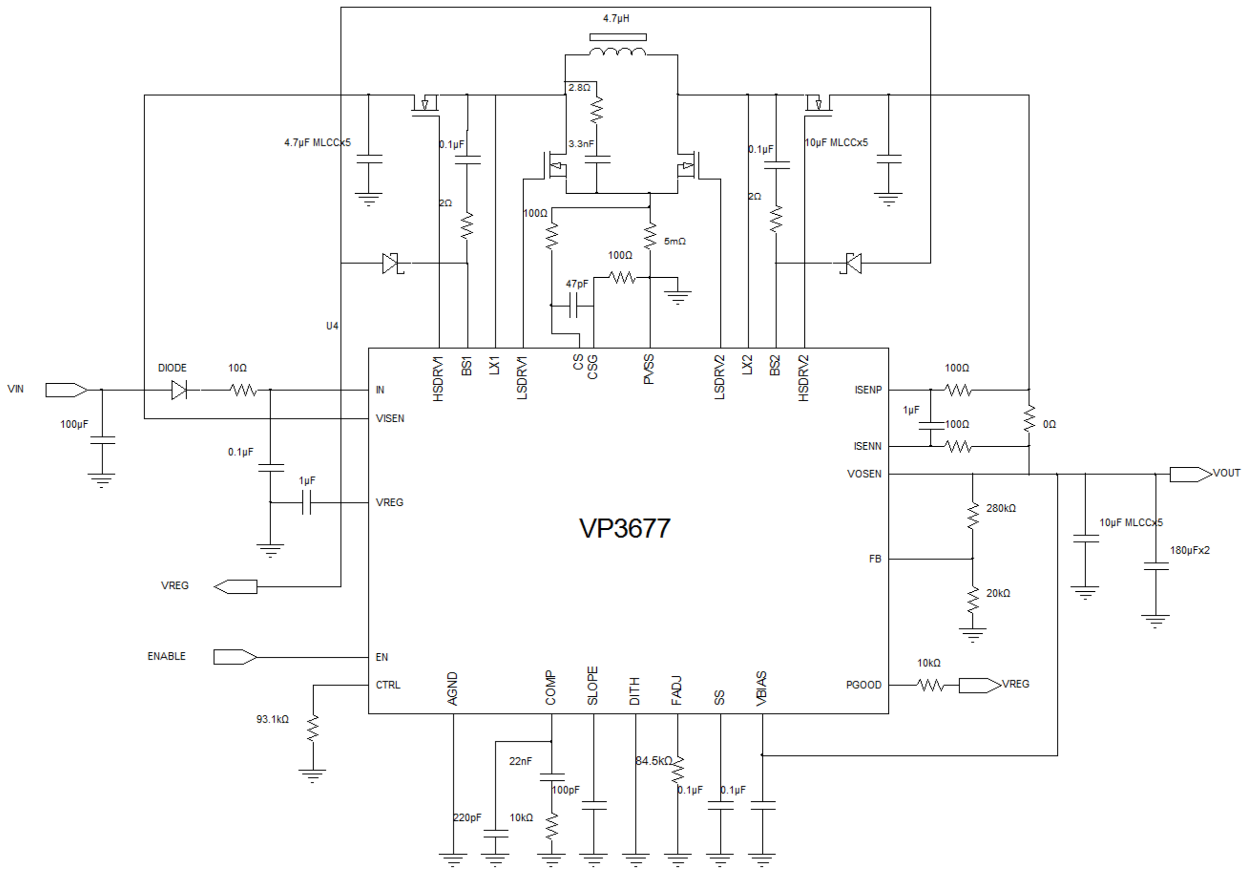



Figure 8. VP3677 Typical Application

| SPECIFICATION ITEM | RATING |
|---|---|
| Input Voltage Range | 9V~48V |
| Output | 12V |
| Load Current | 6A maximum |
| Switching Frequency | 300kHz |
| Protection Scheme | Hiccup |

Table 3. VP3677 Typical Application Specification

## Typical Characteristics

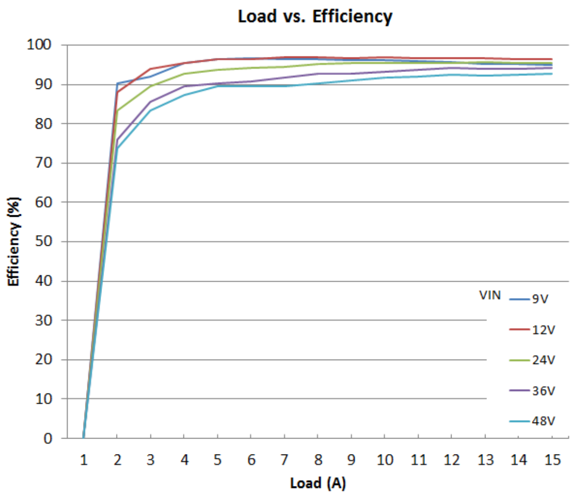



Figure 9. Load vs. Efficiency

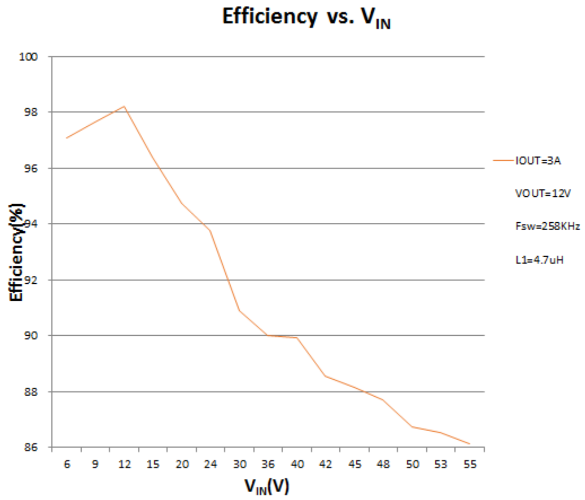
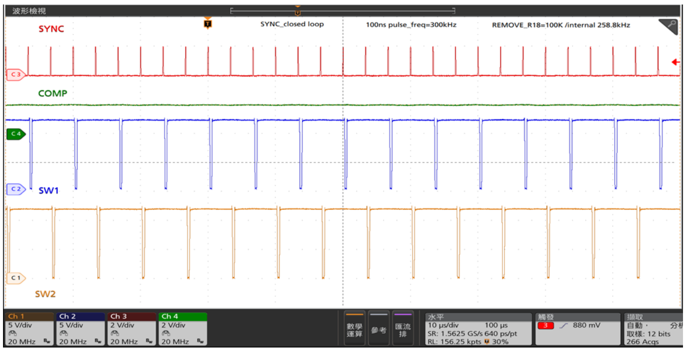



Figure 10. Efficiency ($V_{IN}$)




VIN=12 V VOUT=12 V $C_{SYNC}$=1nF

Figure 11. Clock Sync (100ns pulse/600kHz)

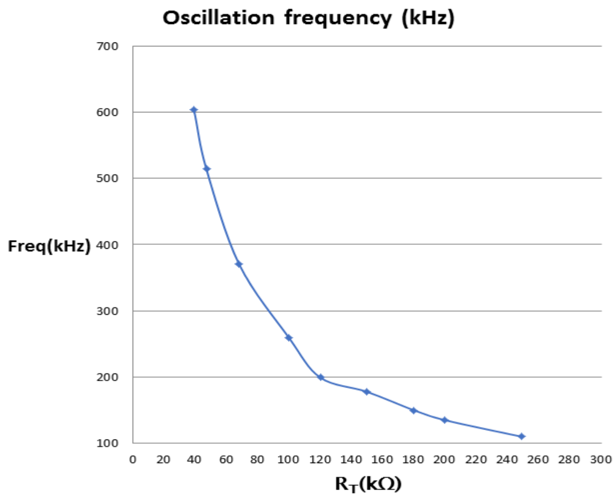
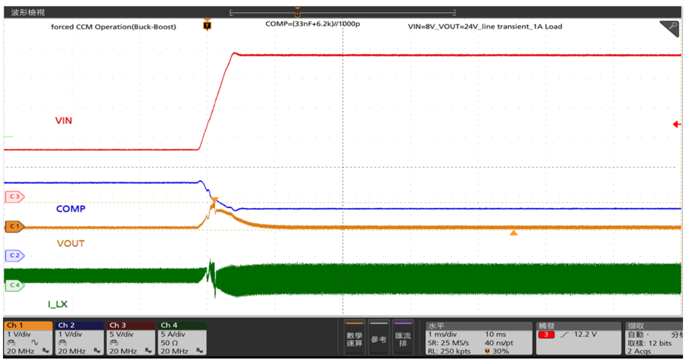
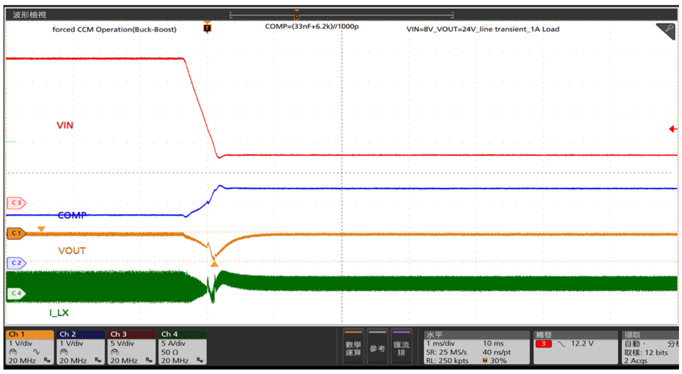



Figure 12. Frequency vs. $R_T$




VIN=8 V to 24 V VOUT=12 V $I_{OUT}$=1A

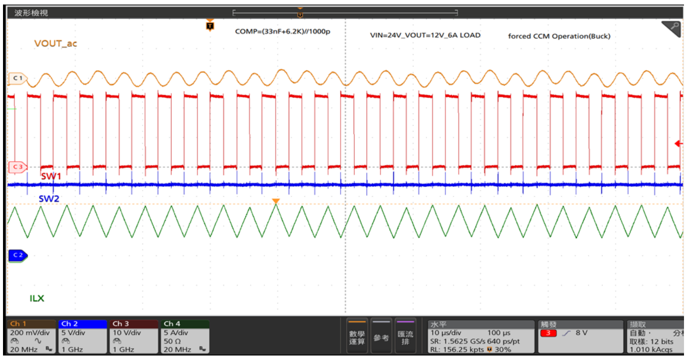
Figure 13. Line Transient




VIN=24V to 8 V VOUT=12 V $I_{OUT}$=1A

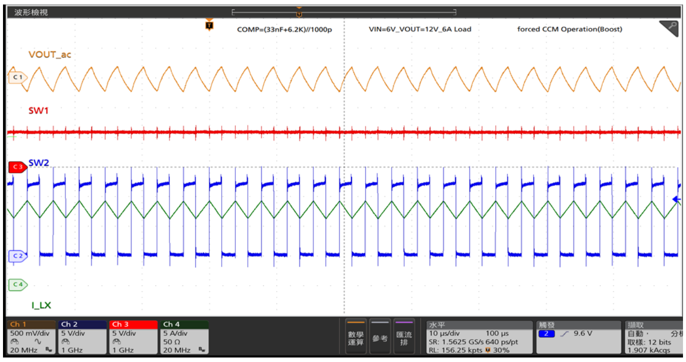
Figure 14. Line Transient

## Typical Characteristics (cont.)



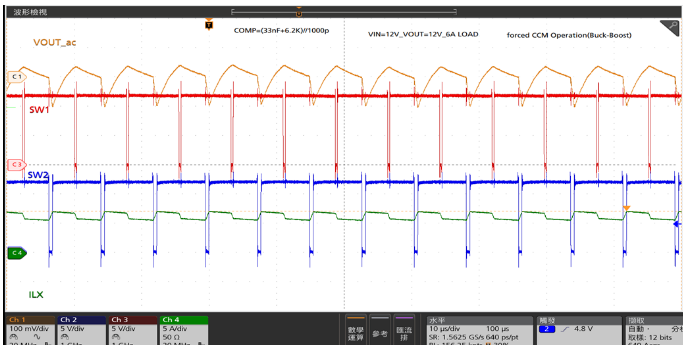

VOUT=12 V VIN=24 V Load = 6A

Figure 15. Forced CCM Operation (Buck)



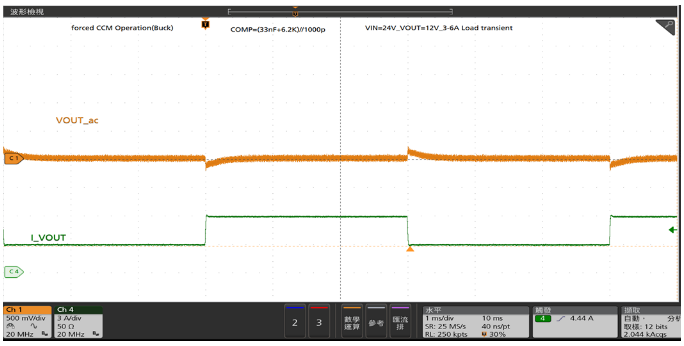

VOUT=24 V VIN=12 V Load = 6A

Figure 16. Forced CCM Operation (Boost)



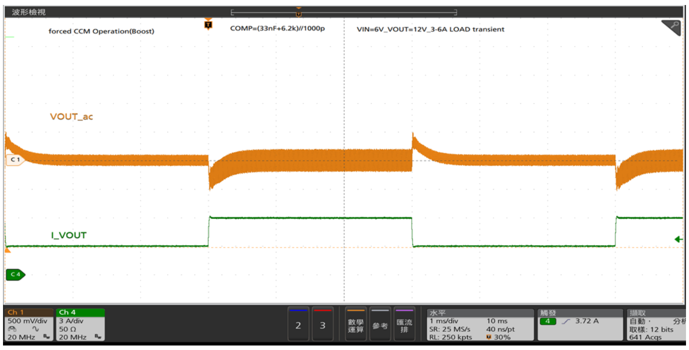

VOUT=12 V VIN=12 V Load = 6A

Figure 17. Forced CCM Operation (Buck-Boost)



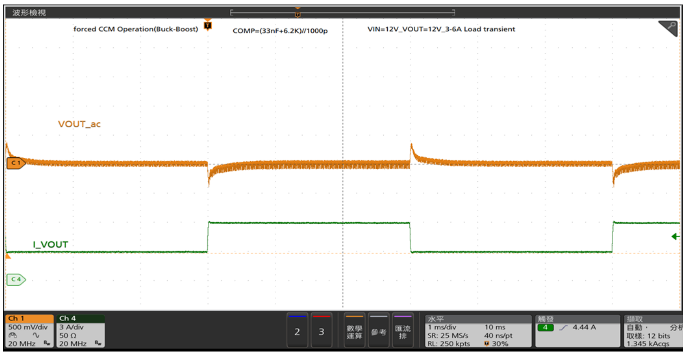

VIN=24 V VOUT=12 V Load 3A to 6A

Figure 18. Load Step (Buck)




VIN=6 V VOUT=12 V Load 3A to 6A

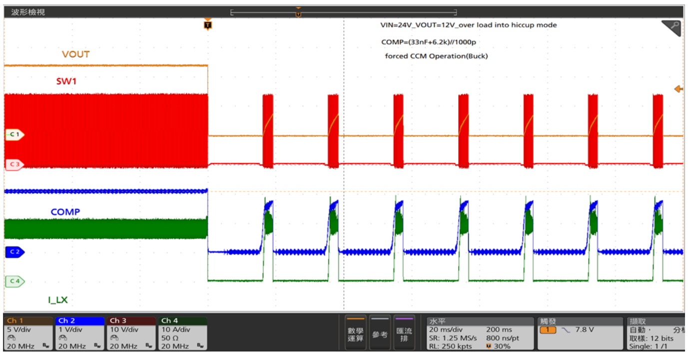
Figure 19. Load Step (Boost)




VIN=12 V VOUT=12 V Load 3A to 6A

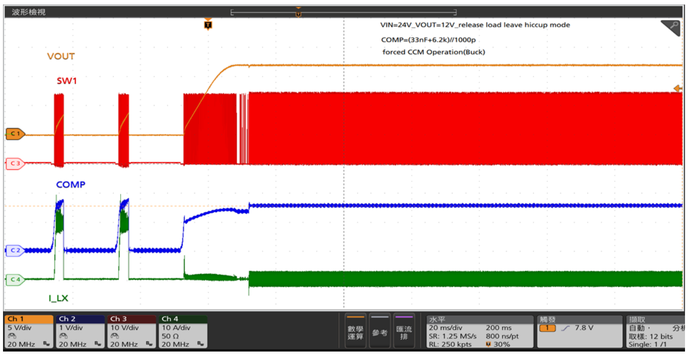
Figure 20. Load Step (Buck-Boost)

## Typical Characteristics (cont.)



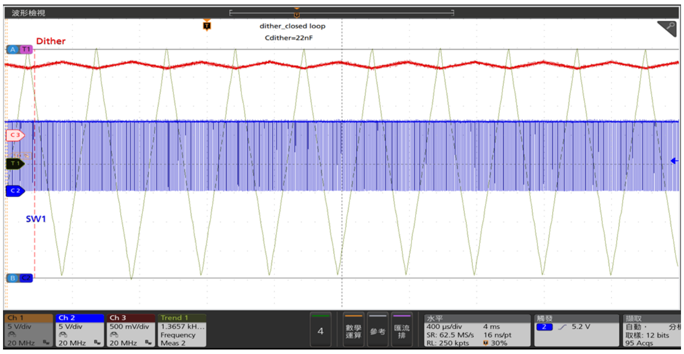

VIN=24 V VOUT=12 V

Figure 21. Entering Hiccup Mode



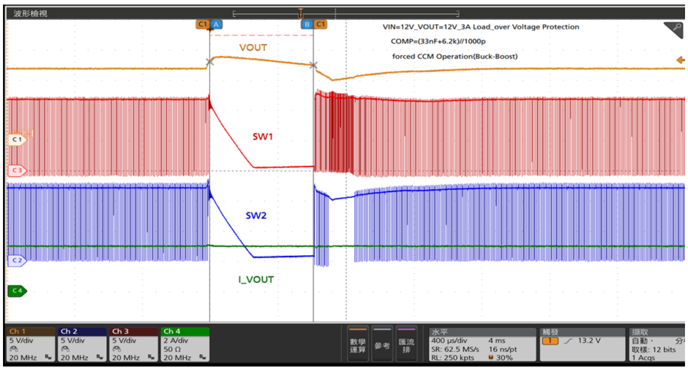

VIN=24 V VOUT=12 V

Figure 22. Exiting Hiccup Mode




VOUT=12 V VIN=12 V $C_{DITH}$=22nF

Figure 23. PWM Dithering

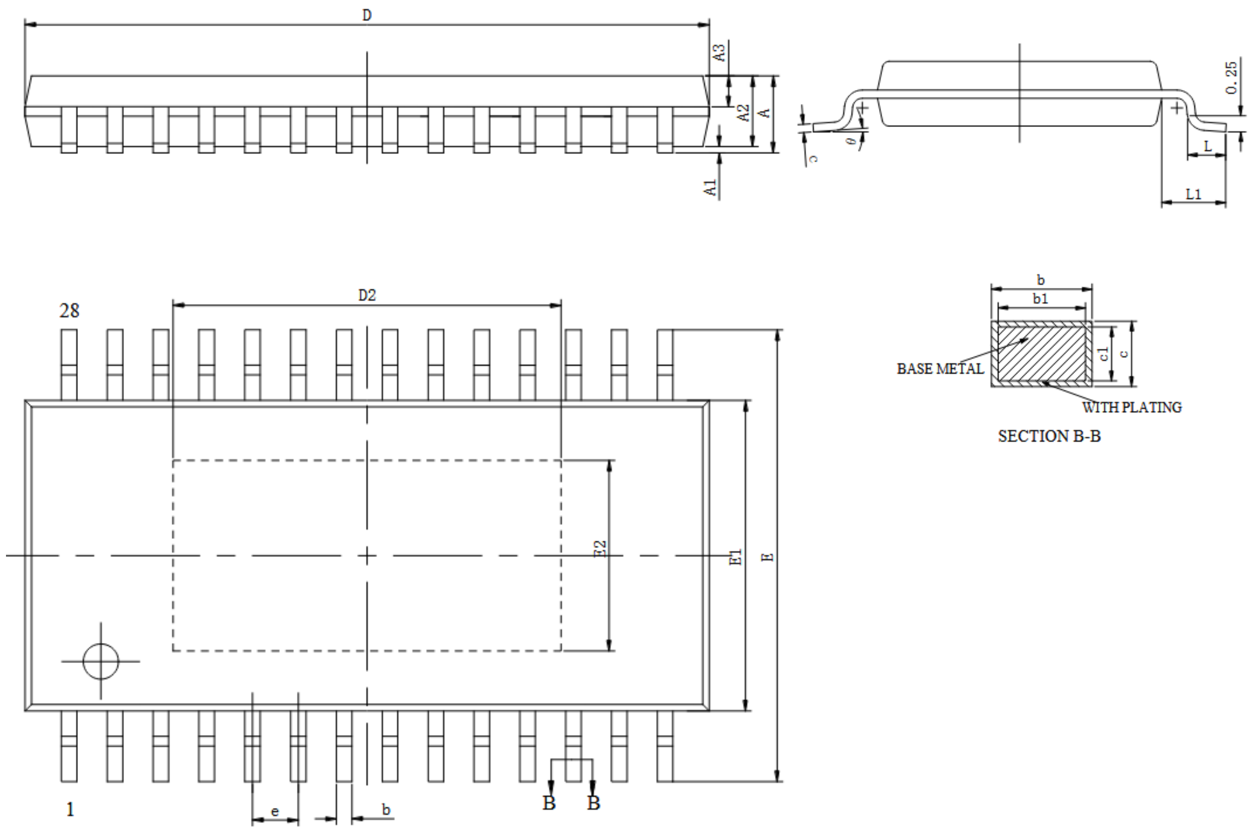



VOUT=12 V VIN=12 V $I_{LOAD}$= 3A

Figure 24. OVP Protection

## Package Information

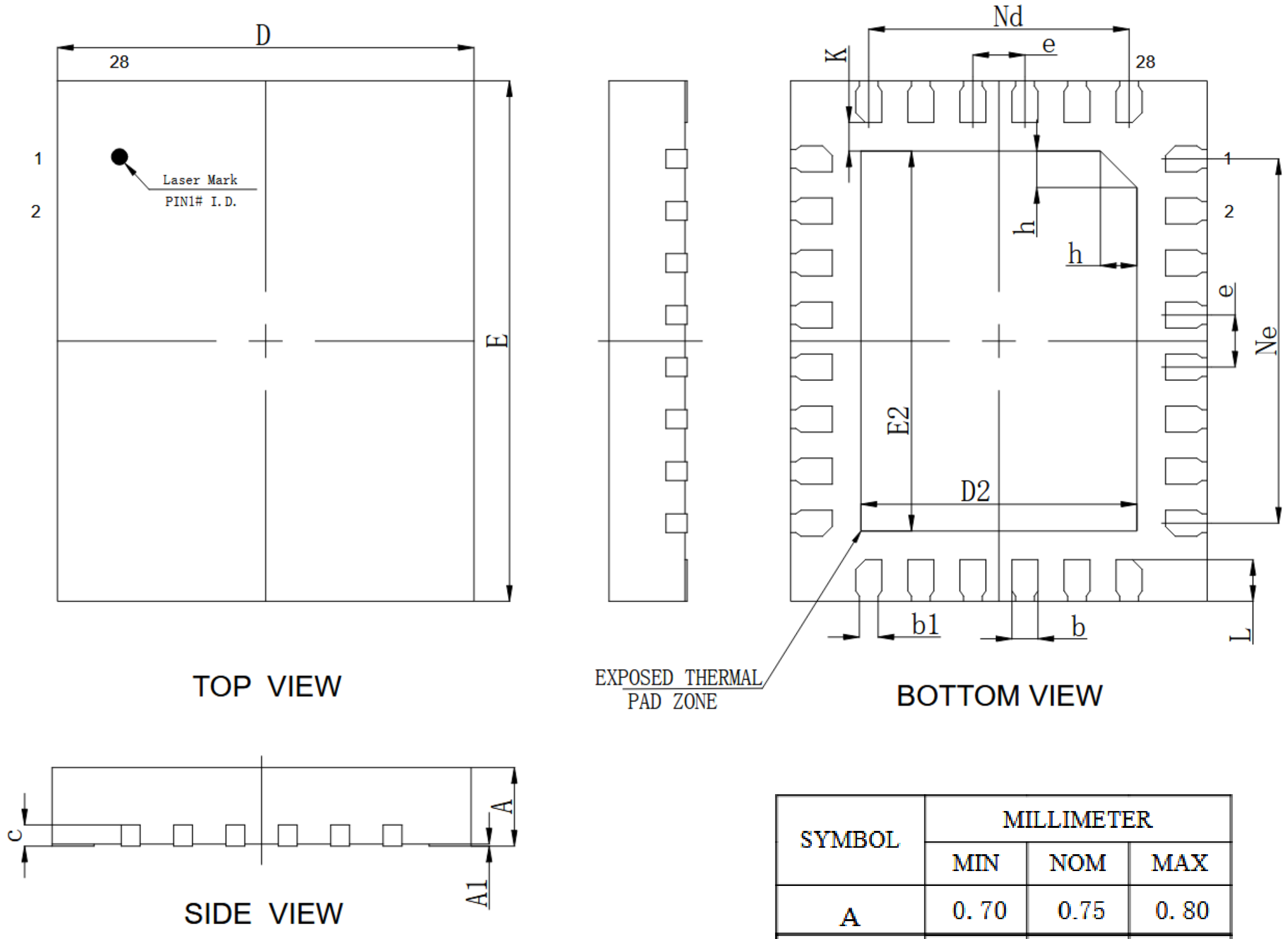
### TSSOP-28EP




| SYMBOL | Millimeter | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | | | 1.2 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.8 | | 1 |
| A3 | 0.39 | 0.44 | 0.49 |
| b | 0.2 | | 0.28 |
| b1 | 0.19 | 0.22 | 0.25 |
| c | 0.13 | | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 9.6 | 9.7 | 9.8 |
| D2 | 4.83REF | | |
| E | 6.2 | 6.4 | 6.6 |
| E1 | 4.3 | 4.4 | 4.5 |
| E2 | 2.70REF | | |
| e | 0.65BSC | | |
| L | 0.45 | 0.6 | 0.75 |
| L1 | 1.00REF | | |
| θ | 0 | | 8 |

## Package Information (cont.)

### QFN28 4x5




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0. 70 | 0.75 | 0. 80 |
| A1 | 0 | 0.02 | 0. 05 |
| b | 0. 20 | 0.25 | 0. 30 |
| b1 | 0.18REF | | |
| c | 0.20REF | | |
| D | 3. 90 | 4. 00 | 4. 10 |
| D2 | 2. 60 | 2. 65 | 2. 70 |
| e | 0. 50BSC | | |
| Ne | 3. 50BSC | | |
| Nd | 2. 50BSC | | |
| E | 4. 90 | 5. 00 | 5. 10 |
| E2 | 3. 60 | 3. 65 | 3. 70 |
| L | 0. 35 | 0. 40 | 0. 45 |
| K | 0. 275REF | | |
| h | 0. 30 | 0. 35 | 0. 40 |

## Ordering Information

VP3677□□□

- 28: Pin Count
- G: Green
- TS: TSSOP with Exposed Pad
  QN: QFN 4x5

| Part No. | Q`ty/Reel |
|---|---|
| VP3677TSG28 | 4,000 |
| VP3677QNG28 | 2,500 |

## Contact Information

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