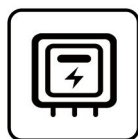


TDSiEMIC

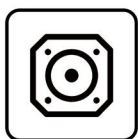
拓 電 半 導 體

自主封測 品質把控 售後保障

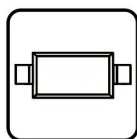
WEB | WWW.TDSEMIC.COM



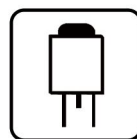
電源管理



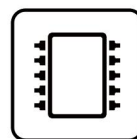
顯示驅動



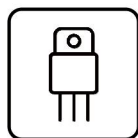
二三極管



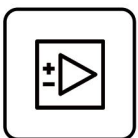
LDO穩壓器



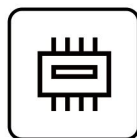
觸摸芯片



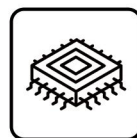
MOS管



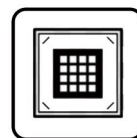
運算放大器



存儲芯片



MCU



串口通信

SN74LS595DR-TD

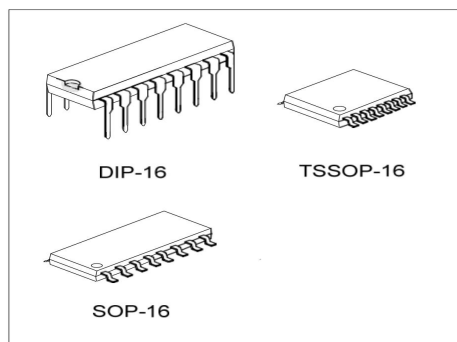
產品規格說明書

1. DESCRIPTION

The 74LS595 contains an 8-bit register with asynchronous reset input and an 8-bit latch with output. The Serial Data Input (SER) will shift into the internal shift register during every LOW-to-HIGH transition on the Shift Clock. The latch will latch the 8-bit data from the shift register during the LOW-to-HIGH transition on the Latch Clock. The shift register also provides a serial output.

2. FEATURES

- Operation Voltage Range: 2 ~ 6V
- High Noise Immunity
- Output Compatibility with CMOS and TTL
- Specified from -40 ~ +125°C
- Package option: DIP-16, SOP-16 and TSSOP-16
- Latch-up performance ≤ 250 mA
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 2023 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 2022 exceeds 2000 V



3. ORDERING INFORMATION

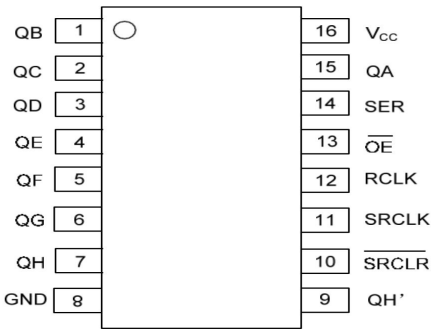
● Tube

Part Number	Marking code	Package	Packing	Pcs/Tube	Pcs/Box
74LS595	74LS595	DIP-16	Tube	25	1250

● Tape Reel

Part Number	Marking code	Package	Packing	Pcs/Reel	Pcs/ Box
74LS595	74LS595	SOP-16	Tape Reel	2.5k	50K
74LS595	74LS595	TSSOP-16	Tape Reel	5K	80K

4. PIN CONFIGURATION

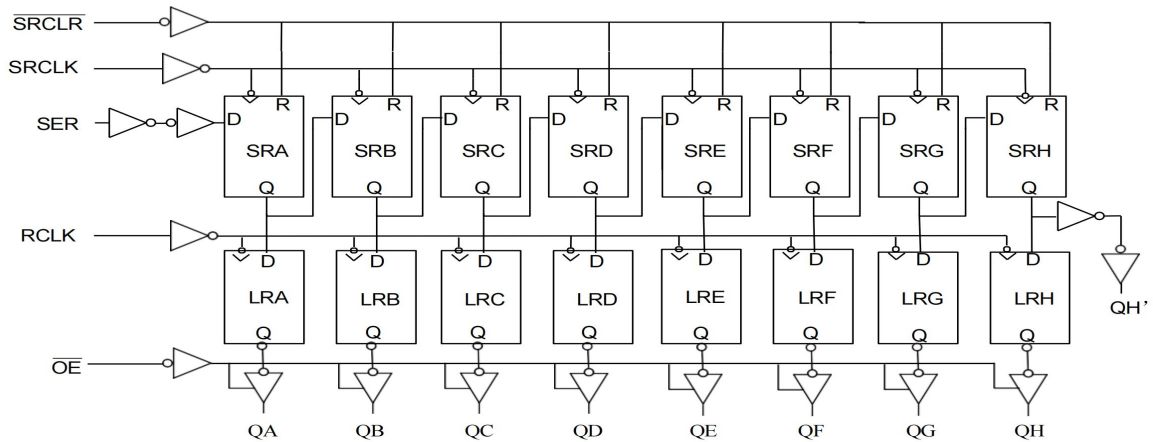


5. FUNCTION TABLE

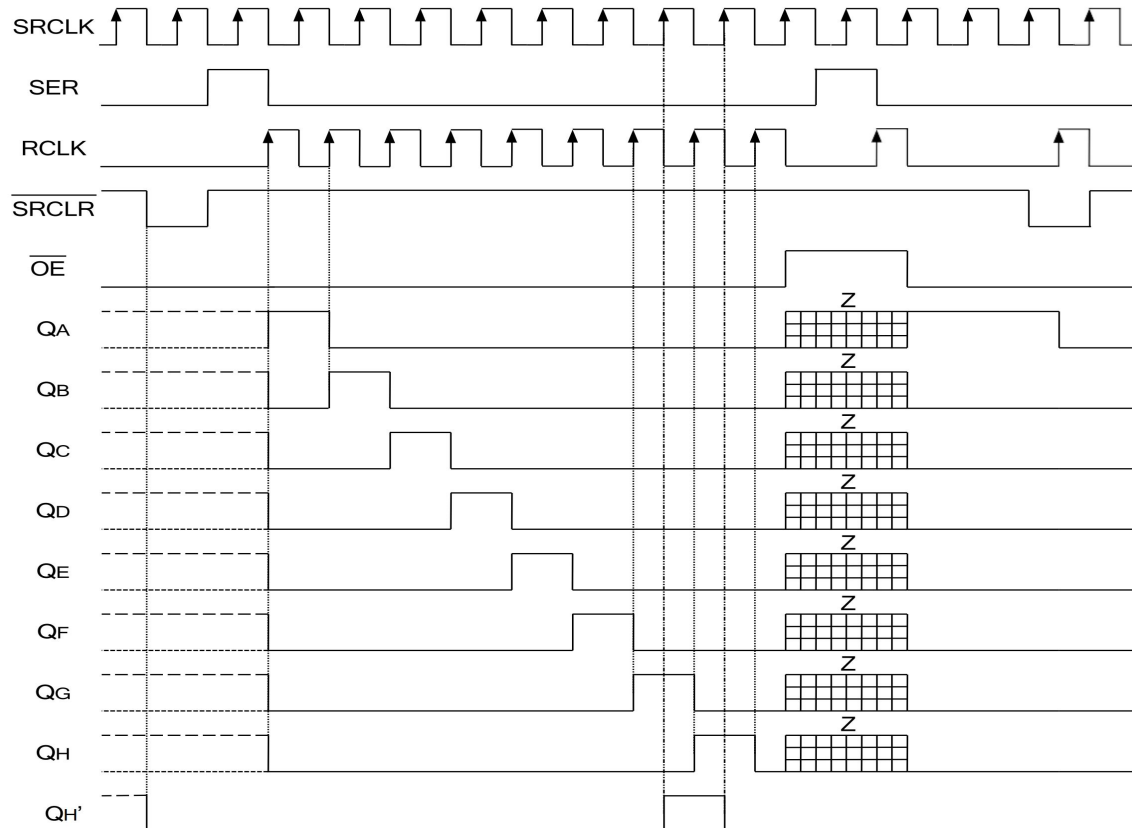
FUNCTION	INPUTS					OUTPUTS	
	SRCLK	RCLK	$\overline{OE}$	$\overline{SRCLR}$	SER	QH'	Qn'
A Low-Level on $\overline{SRCLR}$ only affects the shift registers.	X	X	L	L	X	L	NC
Empty shift register loaded into storage register.	X	↑	L	L	X	L	L
Shift register clear. Parallel outputs in high-impedance OFF-state	X	X	H	L	X	L	Z
Logic high level shifted into the first shift register. Contents of all shift register stages shifted through, e.g. previous state of stage G(internal QG') appears on the serial output(QH').	↑	X	L	H	H	QG'	NC
Contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages.	X	↑	L	H	X	NC	Qn'
Contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages.	↑	↑		H	X	QG'	Qn'

Note: H : HIGH voltage level.
L : LOW voltage level.
X : Don't care.
Z : High impedance OFF-state.
NC: No change.
↑ : Low-to-High transition.
↓ : High-to-Low transition.

6. LOGIC DIAGRAM



7. TIMING DIAGRAM



8. ABSOLUTE MAXIMUM RATING (Note 1)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	-0.5~7.0	V
Input Clamp Current ($V_{IN} < 0$ or $V_{IN} > V_{CC}$)		I_{IK} (Note 2)	±20	mA
Output Clamp Current ($V_{OUT} < 0$ or $V_{OUT} > V_{CC}$)		I_{OK} (Note 2)	±20	mA
Output Current		I_{OUT}	±35	mA
V_{CC} or GND Current		I_{CC}	±75	mA
Power Dissipation	DIP-16	P_D	750	mW
	SOP-16		500	mW
	SOP-16N		550	mW
	SSOP-16		450	mW
	SSOP-16N TSSOP-16			
Storage Temperature		T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. RECOMMENDED OPERATING COMDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}	2	-	6	V
Input Voltage		V_{IN}	0	-	V_{CC}	V
Output Voltage		V_{OUT}	0	-	V_{CC}	V
Operating Temperature		T_A	-40	-	+125	°C
Input Transition Rise or Fall Time	$V_{CC}=2V$	t_R / t_F	-	-	100	ns
	$V_{CC}=4.5V$		-	-	20	ns
	$V_{CC}=6V$		-	-	20	ns

10. ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-Level Input Voltage	V _{IH}	V _{CC} =2V	1.5	-	-	1.5	-	-	V
		V _{CC} =3V	2.1	-	-	2.1	-	-	V
		V _{CC} =4.5V	3.15	-	-	3.15	-	-	V
		V _{CC} =6V	4.2	-	-	4.2	-	-	V
Low-Level Input Voltage	V _{IL}	V _{CC} =2V	-	-	0.5	-	-	0.5	V
		V _{CC} =3V	-	-	0.9	-	-	0.9	V
		V _{CC} =4.5V	-	-	1.35	-	-	1.35	V
		V _{CC} =6V	-	-	1.8	-	-	1.8	V
High-Level Output Voltage, QA-QH	V _{OH}	V _{CC} =2V, I _{OH} =-20μA	1.9	2.0	-	1.9	-	-	V
		V _{CC} =4.5V, I _{OH} =-20μA	4.4	4.5	-	4.4	-	-	V
		V _{CC} =6V, I _{OH} =-20μA	5.9	6.0	-	5.9	-	-	V
		V _{CC} =3V, I _{OH} =-2.4mA	2.48	-	-	2.3	-	-	V
		V _{CC} =4.5V, I _{OH} =-6mA	3.98	-	-	3.7	-	-	V
		V _{CC} =6V, I _{OH} =-7.8mA	5.48	-	-	5.2	-	-	V
Low-Level Output Voltage, QA-QH	V _{OL}	V _{CC} =2V, I _{OL} =20μA	-	0.002	0.1	-	-	0.1	V
		V _{CC} =4.5V, I _{OL} =20μA	-	0.001	0.1	-	-	0.1	V
		V _{CC} =6V, I _{OL} =20μA	-	0.001	0.1	-	-	0.1	V
		V _{CC} =3V, I _{OL} =2.4mA	-	-	0.26	-	-	0.4	V
		V _{CC} =4.5V, I _{OL} =6mA	-	-	0.26	-	-	0.4	V
		V _{CC} =6V, I _{OL} =7.8mA	-	-	0.26	-	-	0.4	V
High-Level Output Voltage, QH'	V _{OH}	V _{CC} =2V, I _{OH} =-20μA	1.9	2.0	-	1.9	-	-	V
		V _{CC} =4.5V, I _{OH} =-20μA	4.4	4.5	-	4.4	-	-	V
		V _{CC} =6V, I _{OH} =-20μA	5.9	6.0	-	5.9	-	-	V
		V _{CC} =3V, I _{OH} =-2.4mA	2.48	-	-	2.3	-	-	V
		V _{CC} =4.5V, I _{OH} =-4mA	3.98	-	-	3.7	-	-	V
		V _{CC} =6V, I _{OH} =-5.2mA	5.48	-	-	5.2	-	-	V
Low-Level Output Voltage, QH'	V _{OL}	V _{CC} =2V, I _{OL} =20μA	-	0.002	0.1	-	-	0.1	V
		V _{CC} =4.5V, I _{OL} =20μA	-	0.001	0.1	-	-	0.1	V
		V _{CC} =6V, I _{OL} =20μA	-	0.001	0.1	-	-	0.1	V
		V _{CC} =3V, I _{OL} =2.4mA	-	-	0.26	-	-	0.4	V
		V _{CC} =4.5V, I _{OL} =4mA	-	-	0.26	-	-	0.4	V
		V _{CC} =6V, I _{OL} =5.2mA	-	-	0.26	-	-	0.4	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} =6V, V _{IN} = V _{CC} or GND	-	-	±0.1	-	-	±1	μA
Output Off-State Current	I _{OZ}	V _{CC} =6V V _{OUT} =V _{CC} or GND	-	-	±0.5	-	-	±10	μA
Quiescent Supply Current	I _{CC}	V _{CC} =6V V _{IN} = V _{CC} or GND, I _{OUT} =0	-	-	4	-	-	160	μA

11. DYNAMIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Clock Pulse Frequency	f _{max}	C _L =50pF	V _{CC} =2V	6	26	-	4	-	MHz
			V _{CC} =4.5V	30	38	-	20	-	MHz
			V _{CC} =6V	35	42	-	24	-	MHz
Propagation Delay From Input (SRCLK) to Output (Q _H ')		C _L =50pF	V _{CC} =2V	-	210	500	-	-	ns
			V _{CC} =4.5V	-	70	175	-	-	ns
			V _{CC} =6V	-	50	150	-	-	ns
Propagation Delay From Input (RCLK) to Output (Q _A -Q _H)	t _{PD}	C _L =50pF	V _{CC} =2V	-	50	140	-	-	ns
			V _{CC} =4.5V	-	17	28	-	-	ns
			V _{CC} =6V	-	14	24	-	-	ns
		C _L =150pF	V _{CC} =2V	-	60	200	-	-	ns
			V _{CC} =4.5V	-	22	40	-	-	ns
			V _{CC} =6V	-	19	34	-	-	ns
Propagation Delay From Input (SRCLR) to Output (Q _H ')	t _{PHL}	C _L =50pF	V _{CC} =2V	-	210	500	-	-	ns
			V _{CC} =4.5V	-	70	175	-	-	ns
			V _{CC} =6V	-	50	150	-	-	ns
Propagation Delay From Input ($\overline{OE}$) to Output (Q _A -Q _H)	t _{en}	C _L =50pF	V _{CC} =2V	-	40	135	-	-	ns
			V _{CC} =4.5V	-	15	27	-	-	ns
			V _{CC} =6V	-	13	23	-	-	ns
		C _L =150pF	V _{CC} =2V	-	70	200	-	-	ns
			V _{CC} =4.5V	-	23	40	-	-	ns
			V _{CC} =6V	-	19	34	-	-	ns
Propagation Delay From Input ($\overline{OE}$) to Output (Q _A -Q _H)	t _{dis}	C _L =50pF	V _{CC} =2V	-	41	150	-	-	ns
			V _{CC} =4.5V	-	15	30	-	-	ns
			V _{CC} =6V	-	12	26	-	-	ns
Output Transition Time (Q _A -Q _H)	t _t	C _L =50pF	V _{CC} =2V	-	28	60	-	-	ns
			V _{CC} =4.5V	-	8	12	-	-	ns
			V _{CC} =6V	-	6	10	-	-	ns
		C _L =150pF	V _{CC} =2V	-	45	210	-	-	ns
			V _{CC} =4.5V	-	17	42	-	-	ns
			V _{CC} =6V	-	13	36	-	-	ns
Output Transition Time (Q _H ')		C _L =50pF	V _{CC} =2V	-	28	75	-	-	ns
			V _{CC} =4.5V	-	8	15	-	-	ns
			V _{CC} =6V	-	6	13	-	-	ns

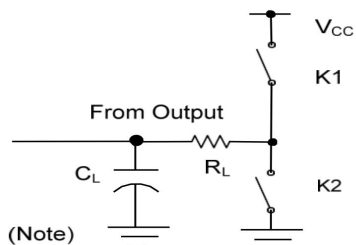
12. TIMING REQUIREMENTS

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40°C~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Pulse Duration, SRCLK or RCLK High or Low	t _w	V _{CC} =2V	80	-	-	110	-	-	ns
		V _{CC} =4.5V	16	-	-	22	-	-	ns
		V _{CC} =6V	14	-	-	19	-	-	ns
V _{CC} =2V		80	-	-	110	-	-	ns	
V _{CC} =4.5V		16	-	-	22	-	-	ns	
V _{CC} =6V		14	-	-	19	-	-	ns	
Pulse Duration, $\overline{\text{SRCLR}}$ Low	t _{su}	V _{CC} =2V	100	-	-	125	-	-	ns
		V _{CC} =4.5V	20	-	-	25	-	-	ns
		V _{CC} =6V	17	-	-	21	-	-	ns
V _{CC} =2V		75	-	-	94	-	-	ns	
V _{CC} =4.5V		15	-	-	19	-	-	ns	
V _{CC} =6V		13	-	-	16	-	-	ns	
V _{CC} =2V		50	-	-	65	-	-	ns	
V _{CC} =4.5V		10	-	-	13	-	-	ns	
V _{CC} =6V		9	-	-	11	-	-	ns	
V _{CC} =2V		50	-	-	60	-	-	ns	
V _{CC} =4.5V		10	-	-	12	-	-	ns	
V _{CC} =6V		9	-	-	11	-	-	ns	
Setup Time, $\overline{\text{SRCLR}}$ High (inactive) Before SRCLK↑	t _h	V _{CC} =2V	3	-	-	3	-	-	ns
		V _{CC} =4.5V	3	-	-	3	-	-	ns
		V _{CC} =6V	3	-	-	3	-	-	ns

13. OPERATING CHARACTERISTIC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C _{IN}	V _{CC} =6V, V _{IN} =V _{CC} or GND	-	-	10	pF
Power Dissipation Capacitance	C _{PD}	No load	-	400	-	pF

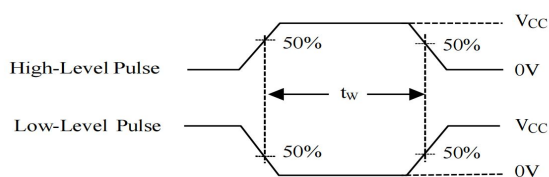
14. TEST CIRCUIT AND WAVEFORMS



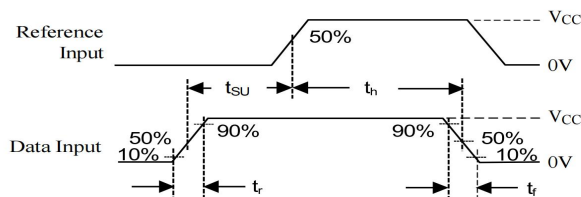
Note: C_L includes probe and jig capacitance. $C_L=50\text{pF}$ or 150pF , $R_L=1\text{K}\Omega$

TEST	K1	K2
t_{PLH}/t_{PHL}	Open	Open
t_{PHZ}/t_{PZH}	Open	Close
t_{PLZ}/t_{PZL}	Close	Open

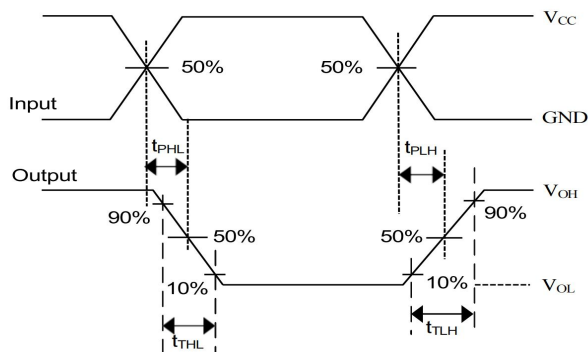
t_{PD} is the same as t_{PHL} and t_{PLH} .
 t_{en} is the same as t_{PZL} and t_{PZH} .
 t_{dis} is the same as t_{PLZ} and t_{PHZ} .



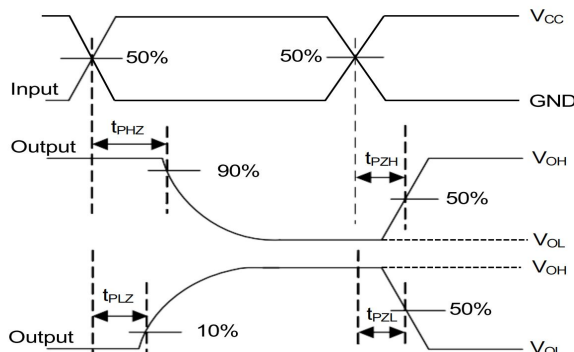
Voltage Waveforms, Pulse Duration



Voltage Waveforms



Voltage Waveforms Propagation Delays

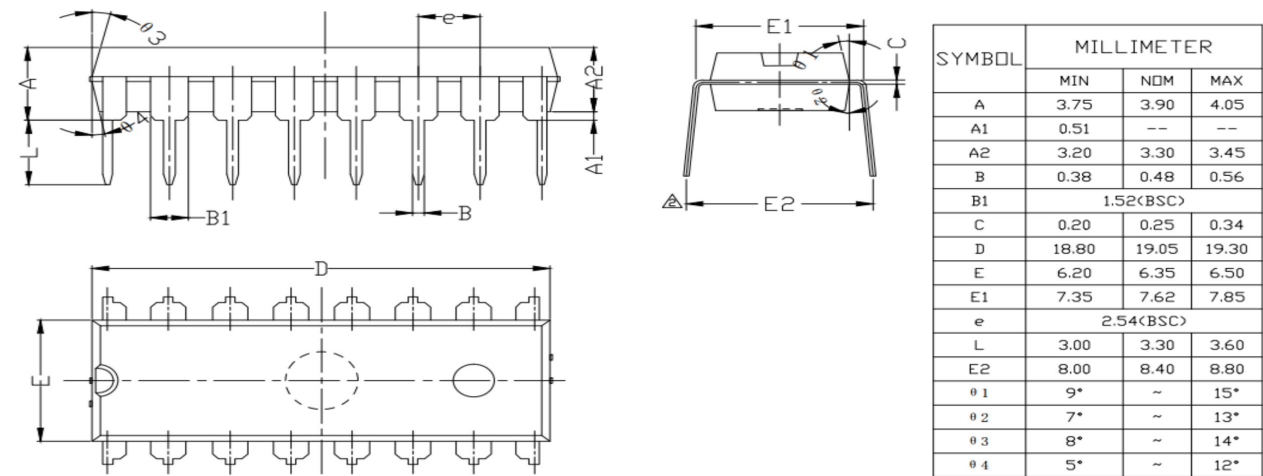


Voltage Waveforms Propagation Delays

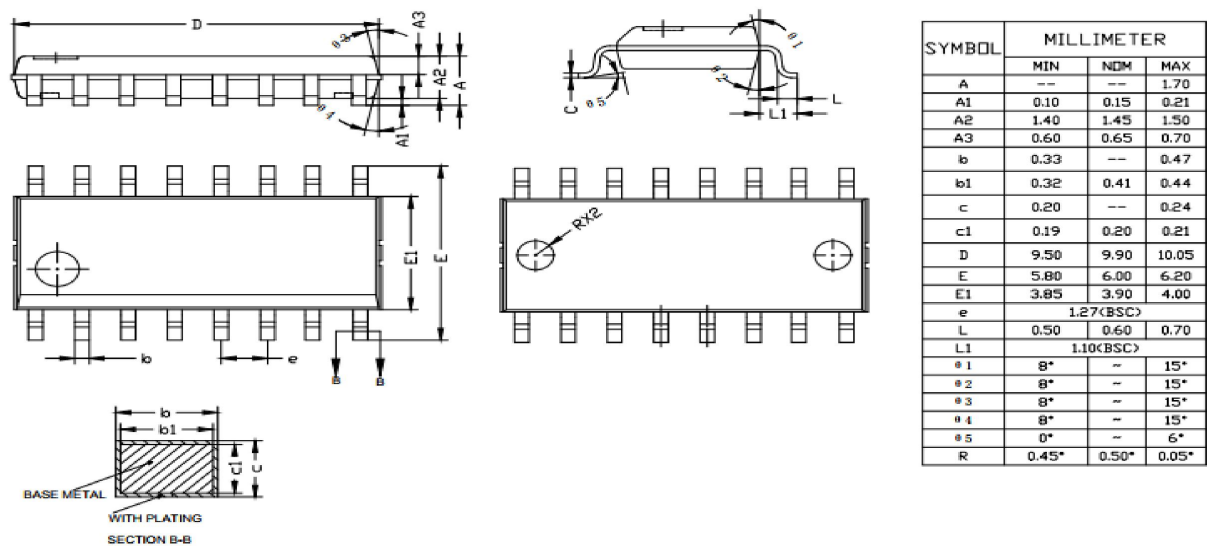
Note: All input pulses are supplied by generators having the following characteristics: $P_{RR} \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_r \leq 3\text{ns}$, $t_f \leq 3\text{ns}$.

15. PACKAGE INFORMATION

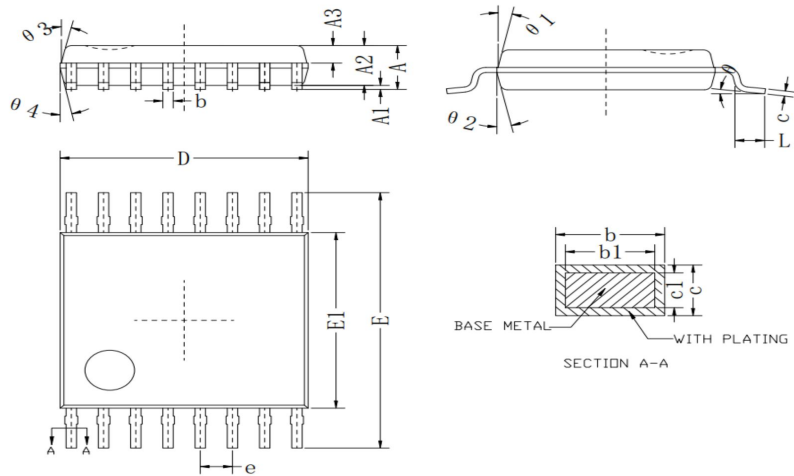
DIP16 package information



SOP16 package information



TSSOP16 package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.20
A1	0.05	0.10	0.15
A2	0.80	1.00	1.05
A3	0.38	0.43	0.48
b	0.19	--	0.29
b1	0.16	0.22	0.26
c	0.13	--	0.15
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 (BSC)		
L	0.45	0.60	0.75
θ	0°	~	8°
θ_1	10°	~	14°
θ_2	10°	~	14°
θ_3	10°	~	14°
θ_4	10°	~	14°