

HMC544AETR-HX GaAs MMIC T/R SWITCH,DC - 4 GHz

Description

The HMC544AETR-HX is a cost-effective SPDT switch housed in a 6-lead SOT-23 package, designed for transmit-receive applications that demand exceptionally low insertion loss at medium power levels. These devices are capable of controlling signals from DC to 4.0 GHz and are particularly well-suited for applications at frequencies of 450, 900, 1900, 2300, and 2700 MHz with an insertion loss of less than 0.5 dB. This GaAs PHEMT design delivers outstanding linearity performance, featuring a +36 dBm compression point at the 1dB level and a +60 dBm third-order intercept point under +3 volt bias conditions. When in the "Off" state, RF1 and RF2 exhibit reflective open characteristics. The integrated on-chip circuitry enables positive control operation while consuming very low DC current.

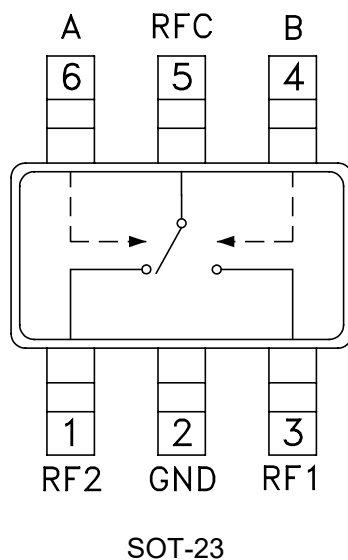
Features

- ★ High Input IP3: +60 dBm
- ★ High Input P1dB: +39 dBm
- ★ Very Low Insertion Loss: 0.2 dB @ 1.0 GHz
- ★ Positive Control: 0/+3V to 0/+5V Compact SOT-23 SMT Package

Applications

- ★ Cellular/PCS/3G Infrastructure
- ★ Basestations & Repeaters
- ★ WLAN, WiMAX and WiBro
- ★ Microwave and Fixed Wireless Radios

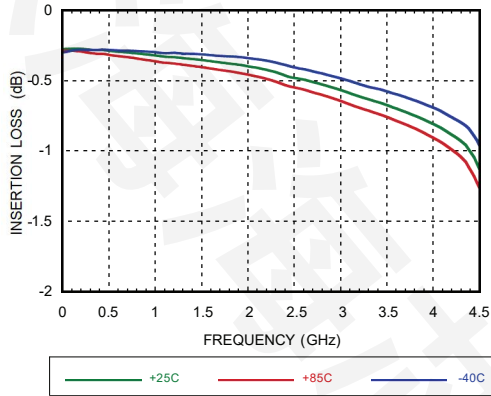
Functional Diagram



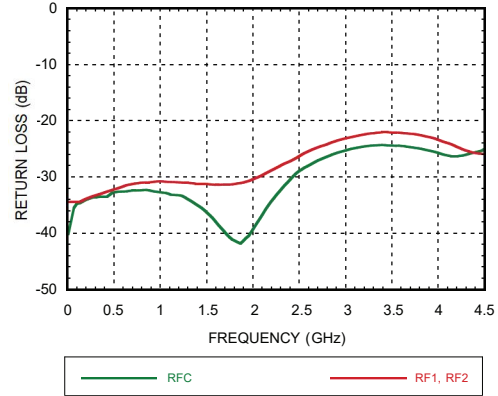
Electrical Specifications, $T_A = +25^\circ\text{C}$, $V_{ctl} = 0/+3\text{ Vdc}$, 50 Ohm System

Parameter	Frequency	Min	Typ	Max	Units
Insertion Loss	DC - 1.0 GHz		0.25	0.5	dB
	DC - 2.5 GHz		0.4	0.7	dB
	DC - 3.0 GHz		0.5	0.8	dB
	DC - 4 GHz		0.7	1.0	dB
Isolation	DC - 1.0 GHz	18	23		dB
	DC - 2.5 GHz	11	16		dB
	DC - 3.0 GHz	9	14		dB
	DC - 4 GHz	8	12		dB
Return Loss	DC - 4 GHz		28		dB
Input Power for 1 dB Compression	0/+5V Control 0/+3V Control	36 33	39		dBm
			35		dBm
Input Third Order Intercept (Two-Tone Input Power = +13 dBm Each Tone)	0.3 - 4.0 GHz		60		dBm
Switching Characteristics	DC - 4 GHz		30		ns
			50		ns

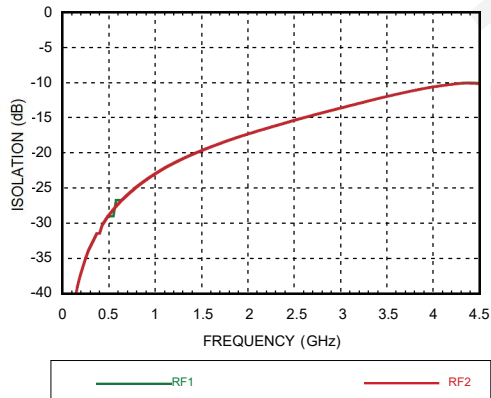
Insertion Loss



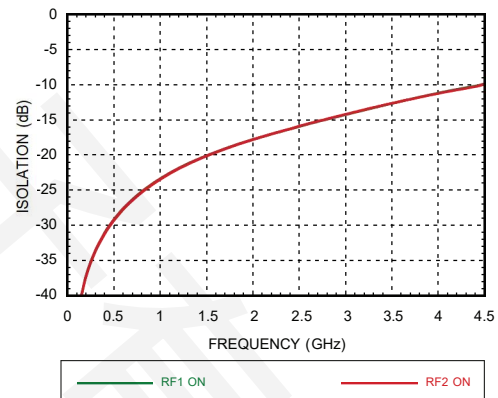
Return Loss



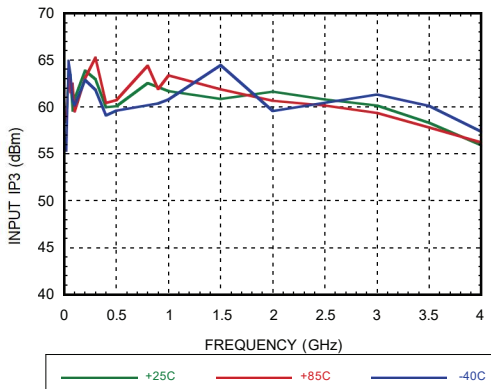
Isolation Between Ports RFC & RF1 / RF2



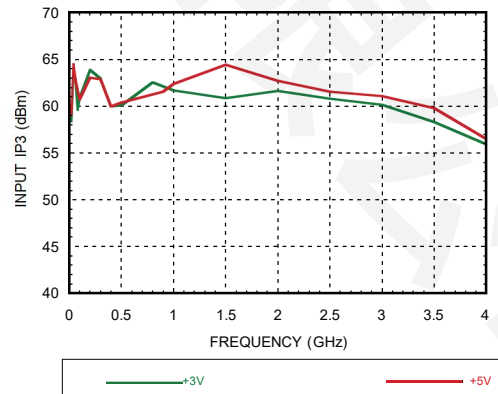
Isolation Between Ports RF1 & RF2



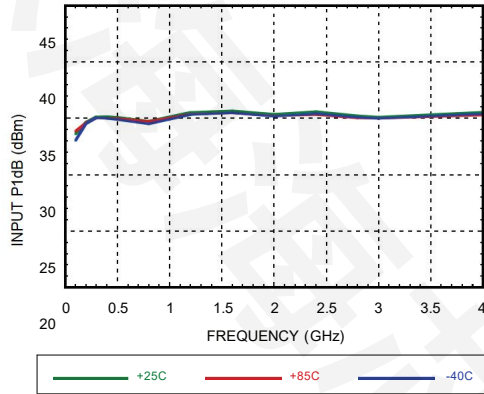
Input IP3 vs. Temperature, Vctl = 0/+3V



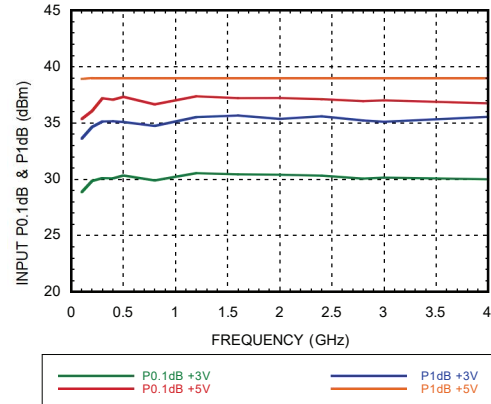
Input IP3 vs. Vctl



Input P1dB vs. Temperature, Vctl = 0/+3V



Compression vs. Vctl



Truth Table

Control Input		Signal Path	
A	B	RFC to RF1	RFC to RF2
Low	High	On	Off
High	Low	Off	On

Control Voltages

State	Bias Condition
Low	0 to 0.2 Vdc @ 1 μ A Typical
High	+3 Vdc @ 0.5 μ A Typical to +5 Vdc @ 1 μ A Typical (± 0.2 Vdc)

Absolute Maximum Ratings

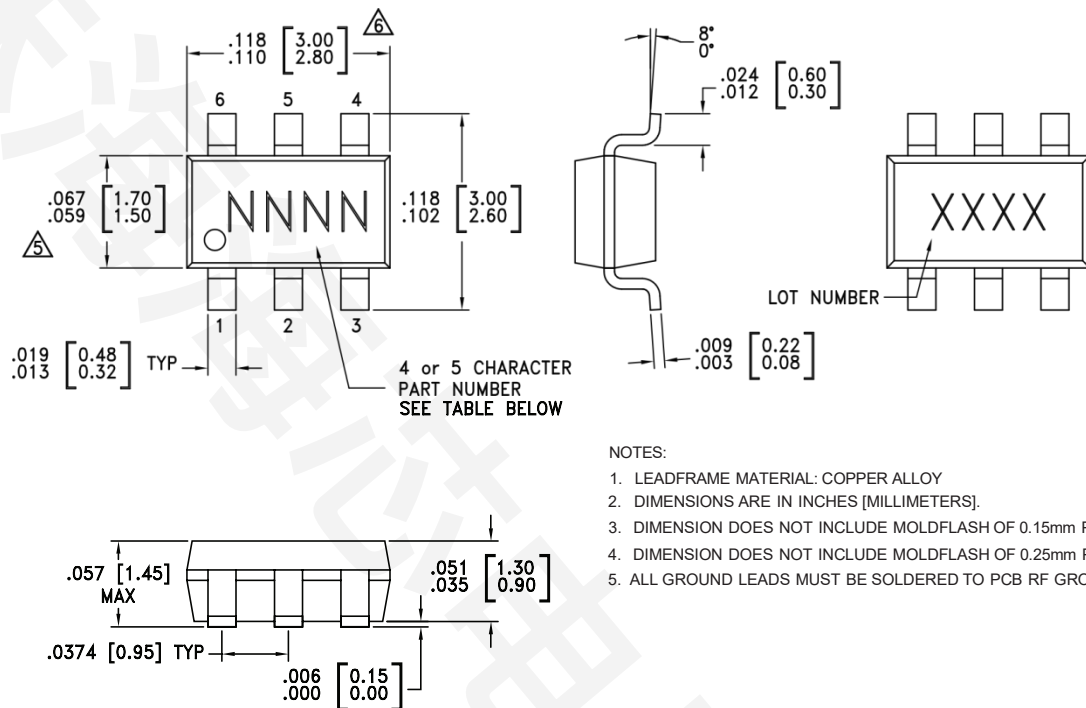
RF Input Power (Vctl = 0/+5V)	+39 dBm
Control Voltage Range (A & B)	-0.2 to +12 Vdc
Hot Switch Power Level (Vctl = 0/+5V)	+39 dBm
Channel Temperature	150 °C
Continuous Pdiss (T= 85 °C) (derate 8.85 mW/ °C above 85°C)	0.574 W
Thermal Resistance	113.3 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1B

DC blocks are required at ports RFC, RF1 and RF2.



Electrostatic sensitive equipment should follow the operation

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
4. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
5. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.

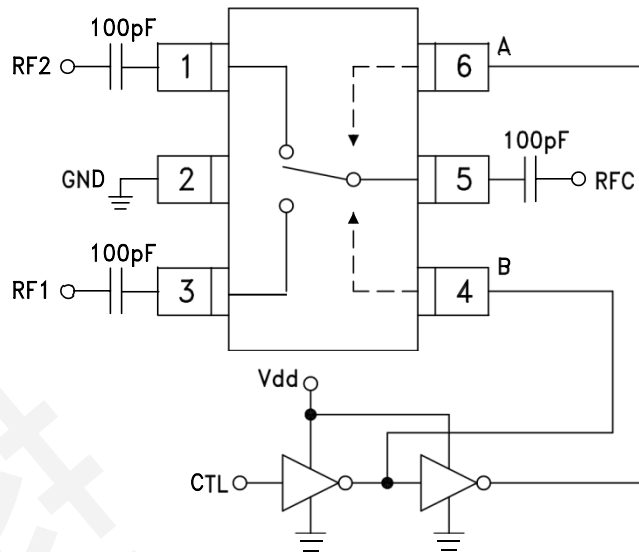
Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating
HMC544AETR-HX	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1

[1] Max peak reflow temperature of 235 °C

[2] Max peak reflow temperature of 260 °C

Typical Application Circuit



Notes:

1. Set logic gate Vdd = +3V to +5V and use HCT series logic to provide a TTL driver interface.
2. Control inputs A/B can be driven directly with CMOS logic (HC) with Vdd of +3V to +5V applied to the CMOS logic gates.
3. DC Blocking capacitors are required for each RF port as shown. Capacitor value determines lowest frequency of operation.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3, 5	RF2, RF1, RFC	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required.	
2	GND	This pin must be connected to RF/DC ground.	
4	B	See truth and control voltage tables.	
6	A	See truth and control voltage tables.	

List of Materials for Evaluation PCB

Item	Description
J1 - J3	PCB Mount SMA RF Connector
J4 - J6	DC Pin
C1 - C2	330 pF capacitor, 0402 Pkg.
R1 - R2	1 KOhm resistor, 0402 Pkg.
U1	HMC544AETR-HX SPDT Switch
PCB [2]	600-00382-00-1 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 Ohm impedance and the package ground leads should be connected directly to the ground plane similar to that shown above.