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TPDTC115EM3T5G

Digital Transistor(NPN)

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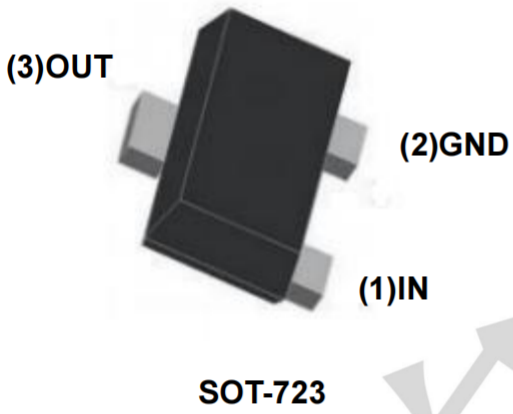
Product Sum ary

- VCC = 50V
- IC = 100mA
- R1 = 100kΩ
- R2 = 100kΩ

Features

- Built-in bias resistors
- making device design easy
- almost completely eliminating parasitic effects

Circuit diagram and pin information



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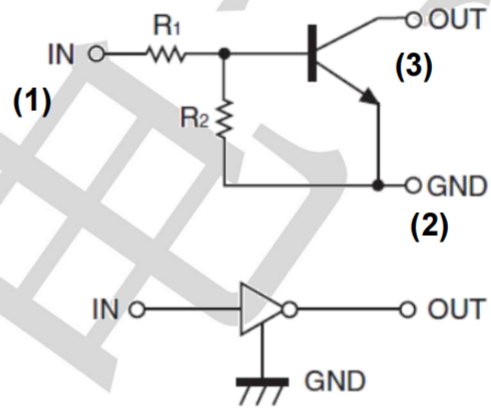

Absolute Maximum Ratings

(Ta=25°C unless otherwise specified)

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	VCC	50	V
Input Voltage	VIN	-10~40V	V
Output Current	I_O	100	mA
Collector current	IC	100	mA
Power Total Dissipation @ T_A=25ºC	P_D	100	mW
Maximum Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	TSTG	-55 to +150	°C

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Electrical Characteristics

(TA=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	$V_{I(off)}$	V_{CC}=5V,I_O=100μA	0.5	--	--	V
	$V_{I(on)}$	V_O=0.3V ,I_O=10mA	--	--	3	V
Output voltage	$V_{O(on)}$	I_O/I_I=10mA/0.5mA	--	0.1	0.3	V
Input current	I_I	V_I=5V	--	--	0.88	mA
Output current	$I_{O(off)}$	V_{CC}=50V,V_I=0	--	--	0.5	μA
DC current gain	G_I	V_O=5V,I_O=5mA	82	--	--	--
Input resistance	R_1		70	100	130	kΩ
Resistance ratio	R_2/R_1		0.8	1.0	1.2	--
Transition frequency	f_T	V_O=10V ,I_O=5mA,f=100MHz	--	250	--	MHz

Note:

1.Characteristics of built-in transistor

2.Each terminal mounted on a reference land

Typical Performance Characteristics(TA=25°C)

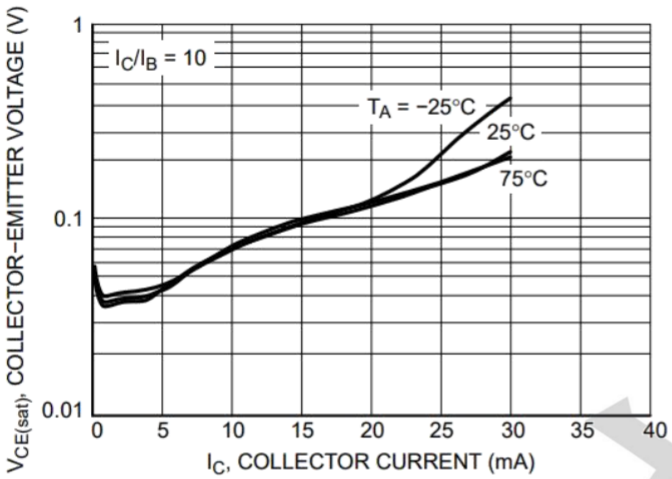

Figure 2. $V_{CE(sat)}$ versus I_C

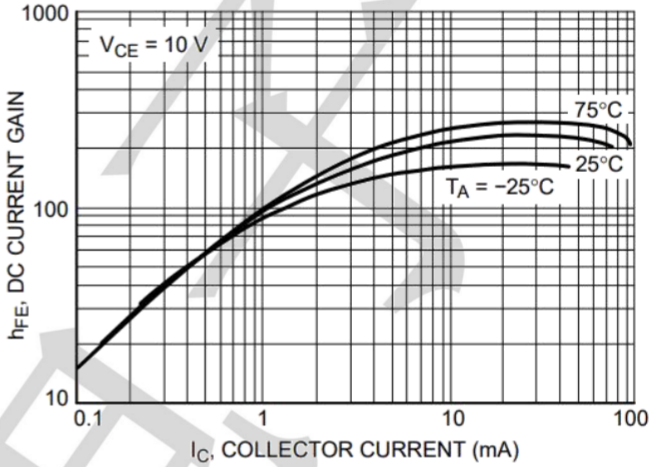

Figure 3. DC Current Gain

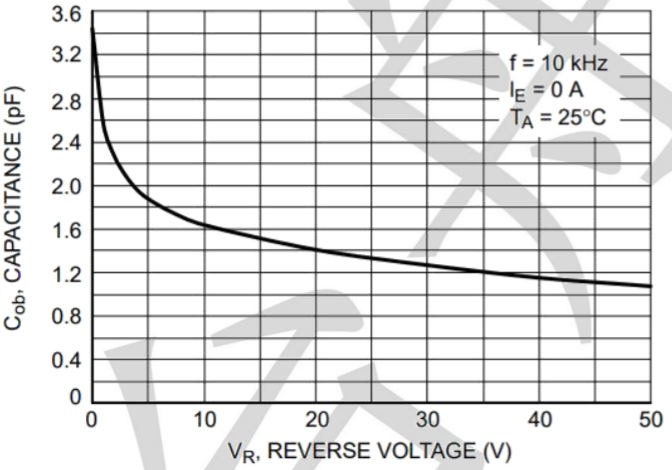

Figure 4. Output Capacitance

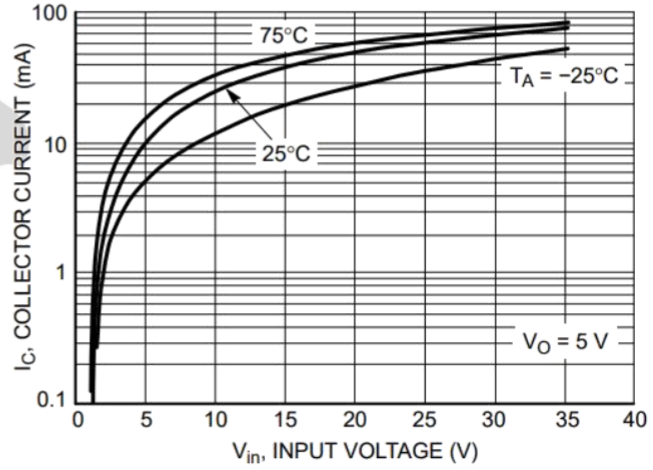

Figure 5. Output Current versus Input Voltage

Package Outline Dimensions (unit: mm)

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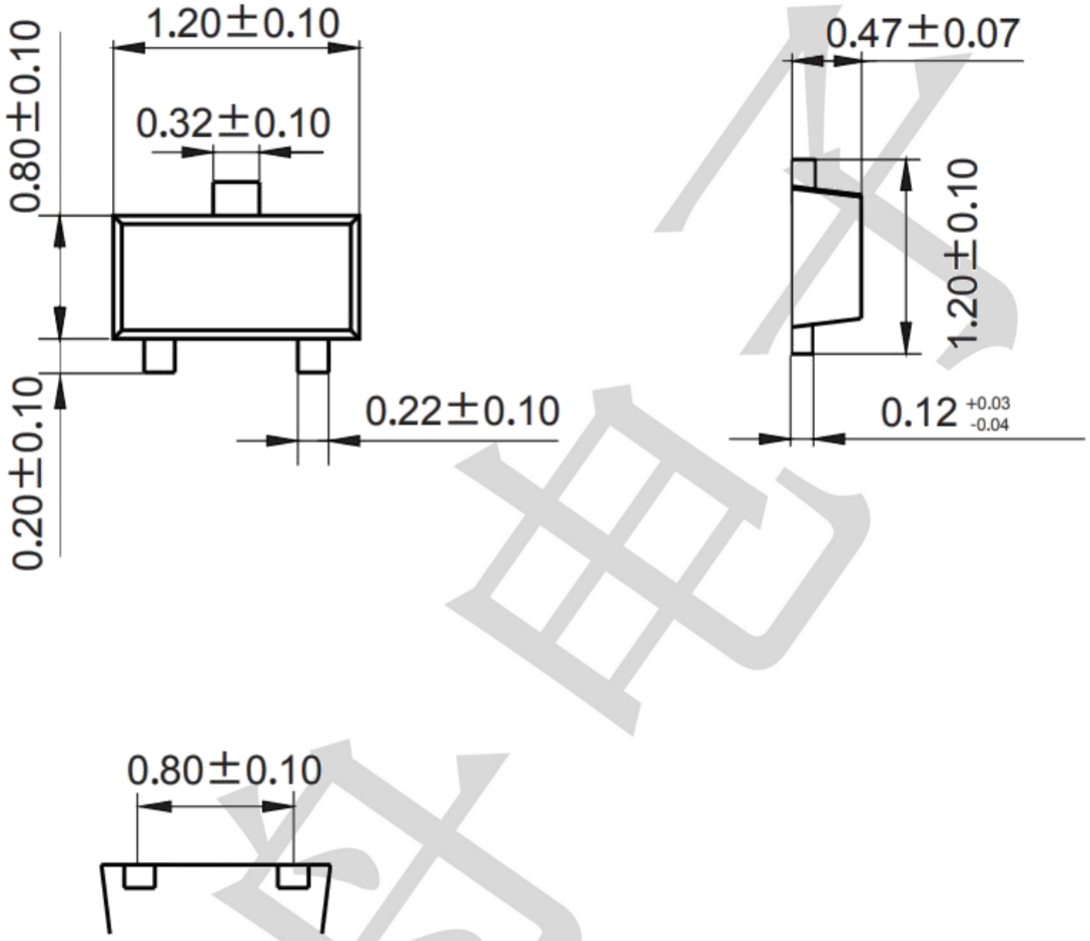

Mounting Pad Layout (unit: mm)